PAL32VX10/A

24-Pin Versatile with XOR Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Increased logic power**
  - Up to 32 inputs and 10 outputs
- **Dual independent feedback paths allow buried state registers or input registers**
- **Programmable flip-flops allow J-K, S-R, T or D types for efficient use of product terms**
- **10 input/output macrocells for flexibility**
- **Programmable registered or combinatorial outputs**
- **Individual user-programmable output polarity**
- **Global register asynchronous/synchronous preset/reset**
- **Automatic register preset on power up**
- **Preloadable output registers for testability**
- **Varied product term distribution**
  - Up to 16 product terms per output
- **300-mil SKINNYDIP® or PLCC packages**
- **Pin-compatible superset of PAL22V10**

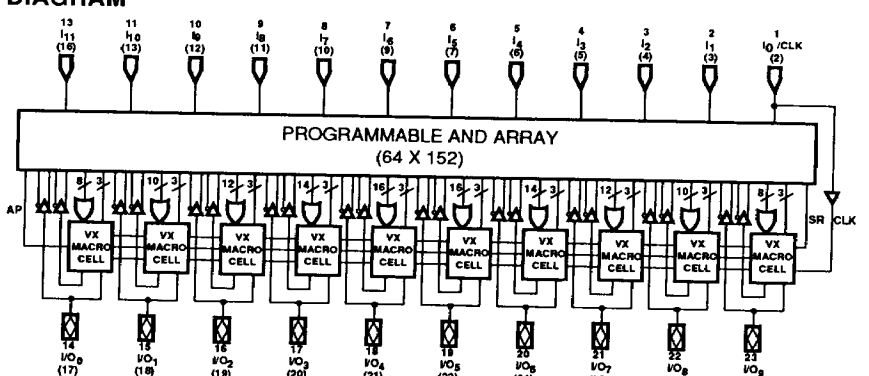
GENERAL DESCRIPTION

The PAL32VX10/A is a high-density Programmable Array Logic (PAL®) device which implements a sum-of-products transfer function via a user-programmable AND logic array and a fixed OR logic array. Featured are ten highly flexible input/output macrocells which are user-configurable for combinatorial or registered operation. Each flip-flop can be programmed to be either a J-K, S-R, T, or D-type for optimal design of state machines and other synchronous logic. In addition, a unique dual feedback architecture allows I/O capability for each macrocell in both combinatorial and registered configurations. This can be achieved even when register feedback is present, and allows implementation of buried flip-flops while preserving the external macrocell input. The PAL32VX10/A is supplied in a space-saving 300-mil-wide dual in-line package offering a powerful, space-saving alternative to SSI/MSI logic devices, while providing the advantage of instant prototyping. Security fuses defeat readout after programming and make proprietary designs difficult to copy.

The PAL32VX10/A is fabricated using Advanced Micro Devices' advanced oxide-isolated bipolar process for high speed and low power. TiW fuse links provide high reliability and programming yields. Preloadable output registers facilitate functional testing.

The PAL32VX10/A can be programmed on standard PAL device programmers, fitted with appropriate programming modules and configuration software. Design development is supported by AMD's PALASM® software as well as by other programmable logic CAD tools available from third-party vendors.

BLOCK DIAGRAM



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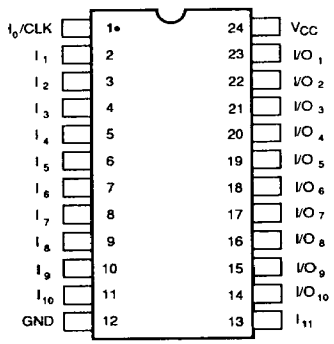
CONNECTION DIAGRAMS

Top View

SKINNYDIP



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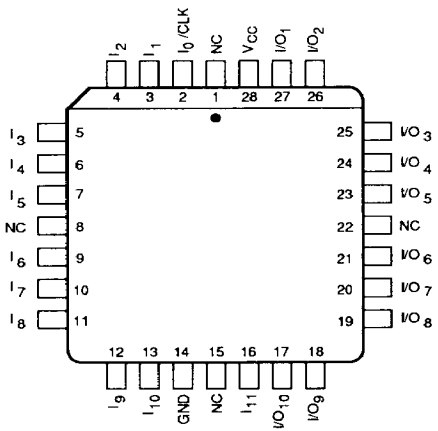
PLCC



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Note:
Pin 1 is marked for orientation.

PIN DESIGNATIONS

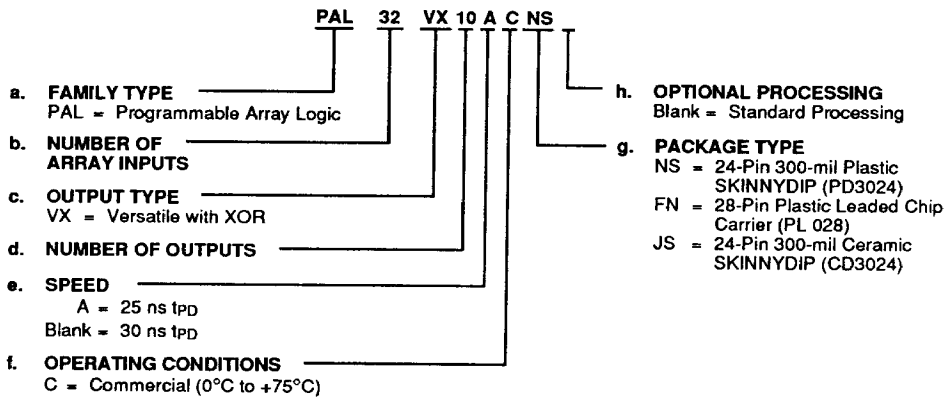
CLK	Clock
GND	Ground
I	Input
I/O	Input/Output
NC	No Connect
V_{CC}	Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. Family Type
b. Number of Array Inputs
c. Output Type
d. Number of Outputs
e. Speed
f. Operating Conditions
g. Package Type
h. Optional Processing



Valid Combinations	
PAL32VX10	CNS, CFN, CJS
PAL32VX10A	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with MMI logo.

FUNCTIONAL DESCRIPTION

The PAL32VX10/A has twelve dedicated input lines and ten programmable I/O macrocells. Pin 1 serves either as an array input or as a clock for all flip-flops. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. The fuse matrix implements a programmable AND logic array, which drives a fixed OR logic array.

The high level of flexibility built into each macrocell, shown in Figure 1, allows the PAL32VX10/A to implement over thirty different architecture options. Each macrocell can be individually programmed to implement a variety of combinatorial or registered logic functions.

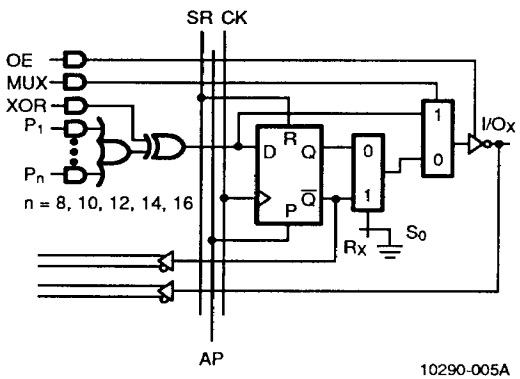


Figure 1. PAL32VX10/A Macrocell

Dual Output Feedback

Dual feedback paths associated with each macrocell provide independent feedback paths directly into the array from both the flip-flop output and the output pin. Unlike other devices which have a single feedback path, the PAL32VX10/A allows each output to have full I/O capability when configured as either a combinatorial output or a registered output, even if register feedback to the array is used. Thus registers can be loaded from their outputs.

If a macrocell is configured as a dedicated input, by disabling the three-state output buffer, the dual feedback architecture allows use of the associated register as an input register or as a "buried" state register, avoiding waste of the flip-flop, as shown in Figure 2.

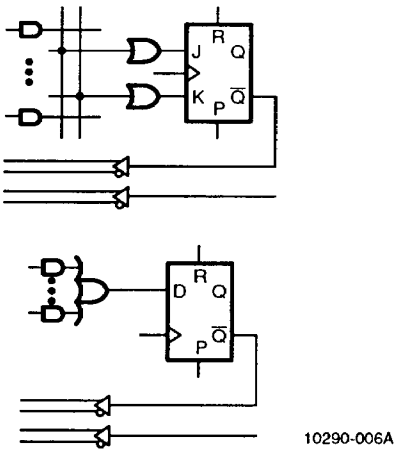


Figure 2. Buried Flip-Flops With Dedicated Inputs

Programmable Flip-flops

Each output macrocell contains a unique programmable flip-flop consisting of a basic D-type flip-flop driven by an XOR gate. This allows the user to choose the optimal flip-flop for the design, since either J-K, S-R, or T-type flip-flops can be synthesized from such a structure without wasting product terms.

As indicated in the macrocell logic diagram, one input of the XOR gate is connected to a single product term, while the second input is connected to the output of the OR logic array. The XOR gate output feeds the input of the D flip-flop. The way in which the XOR gate is used to synthesize the different flip-flop types is described in detail below.

D Flip-Flop. The D flip-flop option is implemented directly. In this configuration, the XOR gate on the input of the flip-flop can be used to program the logic polarity of the transfer function.

J-K Flip-Flop. The J-K flip-flop option can be easily synthesized with a more sophisticated manipulation of the XOR gate inputs and the D flip-flop output.

The transfer function of a J-K flip-flop can be mapped in the Karnaugh map of Figure 3, where Q+ represents the next state of the flip-flop:

J	K	Q=0	Q=1	Q+
0	0	0	(1)	(HOLD)
0	1	0	0	(RESET)
1	1	(1)	0	(TOGGLE)
1	0	(1)	(1)	(SET)

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Figure 3. J-K Flip-Flop Transfer Function

Dropping the (+) for simplicity, the equivalent Boolean expression for Q+ is:

$$Q = \overline{K}*Q + J*\overline{Q}$$

In general, J and K can be sum-of-product expressions which are provided in the PAL architecture only in active-high form. Thus, a direct implementation of $\overline{K}$ expressions must invoke a DeMorgan transformation, which can use excessive product terms. This can be avoided by rewriting the equation for Q without inversion on the J or K inputs.

The XOR gate can be used to construct a logically equivalent expression without any inversions on the J or K inputs. The rewritten Boolean expression is:

$$Q = Q :+: (J*\overline{Q} + K*Q)$$

To check that these expressions are logically equivalent, change the XOR to its equivalent sum-of-products form (remember $A :+: B = A*\overline{B} + \overline{A}*B$) and reduce (using DeMorgan's theorem):

$$Q = Q*\overline{(J*\overline{Q} + K*Q)} + \overline{Q}*(J*\overline{Q} + K*Q)$$

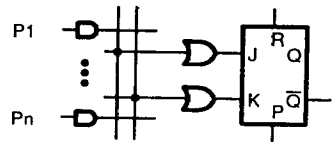
$$Q = Q*((\overline{J} + Q)*(\overline{K} + \overline{Q})) + \overline{Q}*J*\overline{Q} + \overline{Q}*K*Q$$

$$Q = Q*(\overline{J}*\overline{K} + \overline{J}*\overline{Q} + Q*\overline{K} + Q*\overline{Q}) + J*\overline{Q}$$

$$Q = \overline{J}*\overline{K}*Q + \overline{K}*Q + J*\overline{Q}$$

which simplifies to $Q = \overline{K}*Q + J*\overline{Q}$

Since J and K are, in general, sums of products, J and K in either expression can be substituted with (J1 + J2 + ... + Jm) and (K1 + K2 + ... + Kn-m), where n is the total number of product terms associated with a given output macrocell. Thus, the total n-product term resource is shared between the J and K control inputs (Figure 4). Note that all J terms will contain $\overline{Q}$ and all K terms will contain Q.



n = 8, 10, 12, 14, 16

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Figure 4. J-K Flip-Flop Logic Equivalent; J and K Can Also Be Active-Low

The above discussions have assumed that it was most convenient to "group ones" in the Karnaugh map. Sometimes it takes fewer product terms to "group zeros", i.e., implement the inversion of the desired function. The equations shown in Table 1 are equivalent and can be interchanged to optimize product term utilization. This can be readily proved through logic reductions similar to that above.

J and K active high	$Q = Q :+: (J*\overline{Q} + K*Q)$
J active high, K active low	$Q = J*\overline{Q} + \overline{K}*Q$
J active low, K active high	$\overline{Q} = \overline{J}*\overline{Q} + K*Q$
J and K active low	$Q = \overline{Q} :+: (\overline{J}*\overline{Q} + \overline{K}*Q)$

Note:

J = sum of products J1 + J2 + ... + Jm

K = sum of products K1 + K2 + ... + Kn-m

n = total number of available product terms for a given macrocell (8 to 16)

Table 1. J-K Flip-Flop Transfer Functions

S-R Flip-Flop. The S-R flip-flop has a truth table identical to that of the J-K flip-flop, with the exception that the J = K = 1 (toggle) condition is not allowed. The S-R flip-flop implementation is identical to that of the J-K flip-flop, with J-K replaced by S-R, and the S = R = 1 condition avoided.

T Flip-Flop. A T (toggle) flip-flop either holds its state or toggles, depending on the logic state of the T input. The T flip-flop is a subset of the J-K flip-flop and can be considered equivalent to a J-K type with J = K. The general transfer function and its active-low T equivalent are both given in Table 2.

$Q = Q :+: T$
$Q = \overline{Q} :+: \overline{T}$

Note:

T = sum of products T1 + T2 +T3 + ... + Tn

Table 2. J-K Flip-Flop Transfer Functions

Flip-flop Summary

The PAL32VX10/A can synthesize J-K, S-R, T, and D flip-flops, whichever is most convenient for the application, without sacrificing product terms. Additionally, the synthesized equations can use the active-high or active-low forms of the inputs, allowing the designer to minimize product term requirements.

Flip-flop Bypass

Any output in the PAL32VX10/A can be configured to be combinatorial by bypassing the output flip-flop. This is done by setting the output multiplexer to the appropriate state. The multiplexer is controlled by a product term which can be set unconditionally for a permanent combinatorial (all fuses opened, product term high) or registered (all fuses intact, product term low) output configuration, or can be programmed to bypass the output flip-flop "on the fly" allowing signals to be routed directly to output pins under user-specified conditions.

Varied Product Term Distribution

An increased number of product terms has been provided in the PAL32VX10/A over previous generation PAL devices. These terms are distributed among the ten macrocells in a varied manner, ranging from eight to sixteen terms per output. The five output pairs have 8, 10, 12, 14, or 16 product terms available for the OR gate within each macrocell. In addition, each macrocell has one XOR product term and two architecture control product terms.

Programmable I/O

Each macrocell has a three-state output buffer with programmable three-state control. Control is implemented by a single product term, allowing specification of enable/disable functions controlled by any device input or output. Each macrocell can be configured as a dedicated input by disabling the buffer drive capability. When this is done, the associated register can still be used as an input register or buried state register, due to the independent register feedback path.

Programmable Preset and Reset

The ten macrocell flip-flops share common programmable preset and reset control for easy system initialization. The Q outputs of the register will go to the logic LOW state following a LOW-to-HIGH transition on pin 1 (I_0/CLK) when the synchronous reset (SR) product term is asserted. The register will be forced to the logic HIGH state independent of the clock when the asynchronous preset (AP) product term is asserted.

Programmable Polarity

The polarity of each macrocell output can be set active high or active low.

Combinatorial Outputs. The XOR gate provides polarity control for combinatorial outputs, with the single product term to the XOR gate controlling the invert/not invert function. With all fuses intact, there is no inversion through the XOR gate, creating an active-low output. Opening all fuses forces the product term high, inverting data and creating an active-high output.

Registered Outputs. Output polarity for registered outputs can be determined in two ways. For D-type registered outputs, polarity can be set by the XOR gate, as is the case with combinatorial outputs. Using this method to set polarity, preset and reset will not be affected.

Polarity, as observed from the output pin, can also be determined by the flip-flop output multiplexer. Note that this does not affect the polarity of the register feedback signal, but does affect preset and reset. By changing the flip-flop output multiplexer, the preset and reset functions are exchanged relative to the controlling product terms.

With the multiplexer fuse intact, the $\overline{Q}$ output is routed to the output pin, configuring an active-low output. With the multiplexer fuse opened, Q is routed to the output pin and synchronous reset becomes synchronous preset. Similarly, asynchronous reset becomes asynchronous preset.

Polarity options for J-K, S-R, and T flip-flops have been discussed in the section on programmable flip-flops.

Power-up Preset

All flip-flops power up to a logic HIGH for predictable system initialization. Outputs of the PAL32VX10/A will be HIGH or LOW depending on the state of the register output multiplexers.

Register Preload

The register on the PAL32VX10/A can be preloaded to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, thereby making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading in illegal states and observing proper recovery.

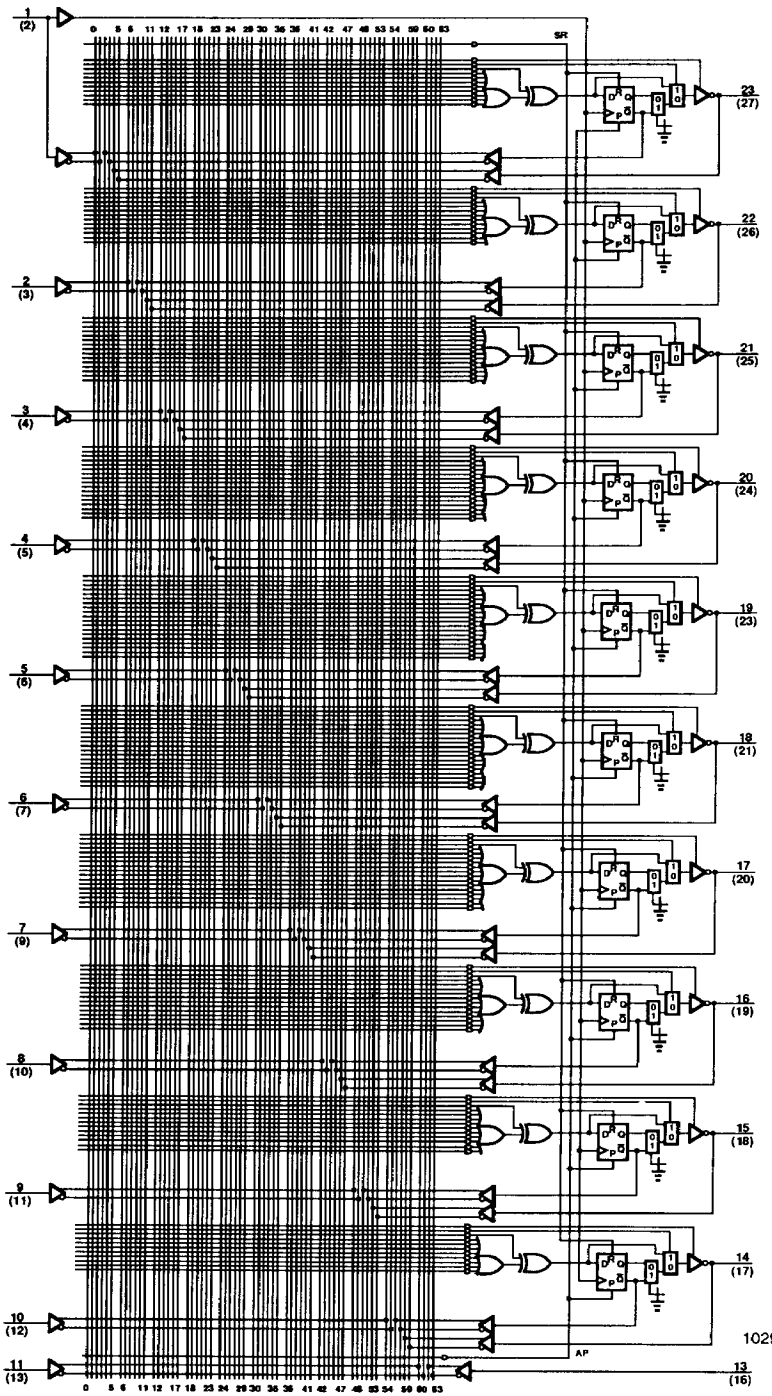
Security Fuse

After programming and verification, a PAL32VX10/A design can be secured by programming the security fuses. Once programmed, these fuses defeat readback of the internal fuse pattern by a device programmer, making proprietary designs very difficult to copy. The array will read as if every fuse is programmed.

Quality and Testability

The PAL32VX10/A offers a very high level of built-in quality. Special on-chip test circuitry provides a means of verifying performance of all AC and DC parameters prior to programming. In addition, these built-in test paths verify complete functionality of each device to provide the highest post-programming functional yields in the industry.

LOGIC DIAGRAM SKINNYDIP (PLCC) Pinouts



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ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–1.5 V to +5.5 V
DC Output or I/O Pin Voltage	5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 2)		25	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		180	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = +25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		11	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

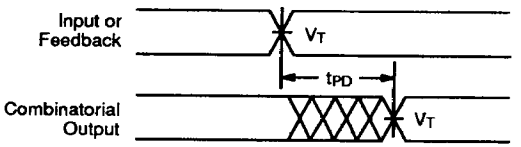
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				A		Std		Unit
					Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Combinatorial Output	Product Terms P_1–P_n				25		30	ns
		Product Term XOR				30		35	
t_S	Setup Time from Input, Feedback, or SP to Clock	Product Terms P_1–P_n, SR			25		30		ns
		Product Term XOR			30		35		
t_H	Hold Time				0		0		ns
t_{CO}	Clock to Output					15		15	ns
t_{AP}	Asynchronous Preset to Registered Output					25		30	ns
t_{APW}	Asynchronous Preset Width				25		30		ns
t_{APR}	Asynchronous Preset Recovery Time				25		30		ns
t_{SRR}	Synchronous Reset Recovery Time				25		30		ns
t_{CR}	Input or Feedback to Registered Output from Combinatorial Configuration (Product Term MUX 1→ 0)					90		90	ns
t_{RC}	Input or Feedback to Combinatorial Output from Registered Configuration (Product Term MUX 0 → 1)					90		90	ns
t_{WL}	Clock Width	LOW			18		20		ns
t_{WH}		HIGH			18		20		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	Product Terms P_1–P_n	25		22.5		MHz
				Product Term XOR	22.2		20		
		No Feedback	$1/(t_{WH} + t_{WL})$		27.7		25		MHz
t_{EA}	Input to Output Enable Using Product Term Control					25		30	ns
t_{ER}	Input to Output Disable Using Product Term Control					25		30	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.

SWITCHING WAVEFORMS



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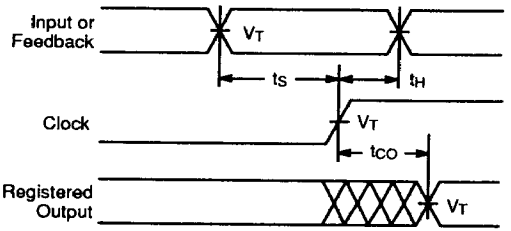
Combinatorial Output



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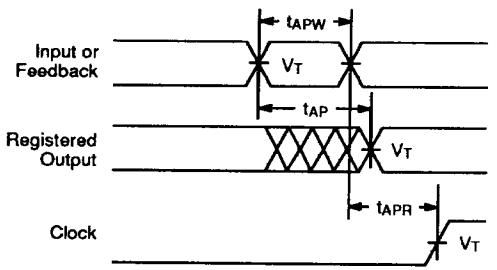
Registered Output



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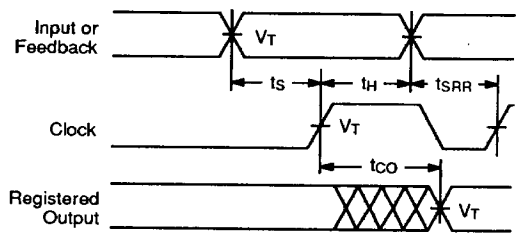
Asynchronous Preset



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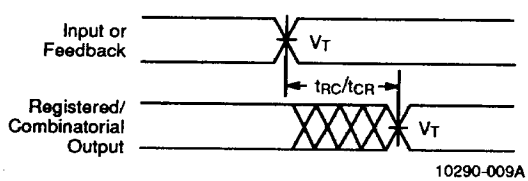
Synchronous Reset



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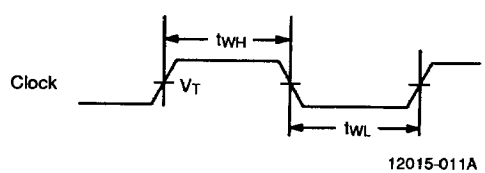
Configuration Change



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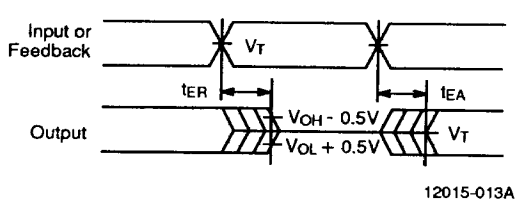
Clock Width



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Input to Output Disable/Enable

Notes:

1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2–5 ns typical.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

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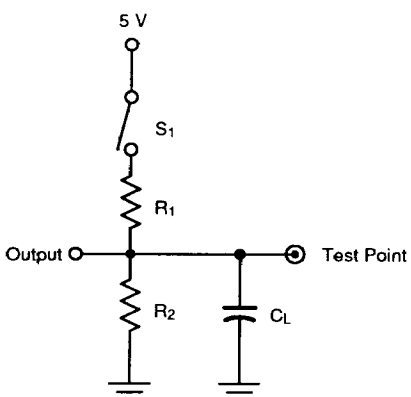
SWITCHING TEST CIRCUIT



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Specification	S_1	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	50 pF	300 Ω	390 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} - 0.5 V L → Z: V_{OL} + 0.5 V

USE OF XOR PRODUCT TERM

The speed of the PAL32VX10/A is specified according to the use of the Exclusive-OR (XOR) product term in the macrocell. Note that the macrocell data input is a function of the two-input XOR gate, whose inputs are the OR of the product terms P_1–P_n and the single additional XOR product term (Figure 5).

The specification for the path through the single XOR product term is 5 ns slower than through the P_1–P_n product terms and the OR gate. As a result, if the single XOR product term is changing, the macrocell data input will not be available until 5 ns later than if only the P_1–P_n product terms were changing.

This difference between paths affects t_{PD}, t_S and f_{MAX} (feedback). As a result, these three parameters are specified both for only the P_1–P_n product terms changing ("Product terms P_1–P_n") and with the single XOR product term changing ("Product term XOR") (See table).

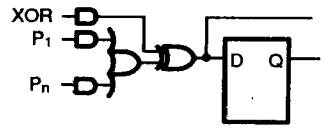
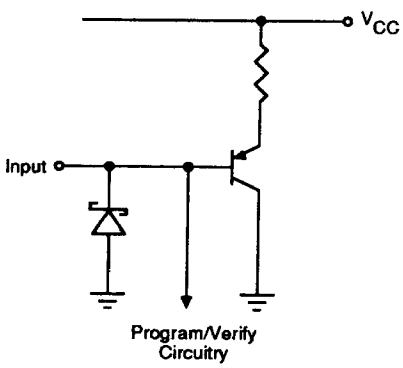


Figure 5. XOR Product Term

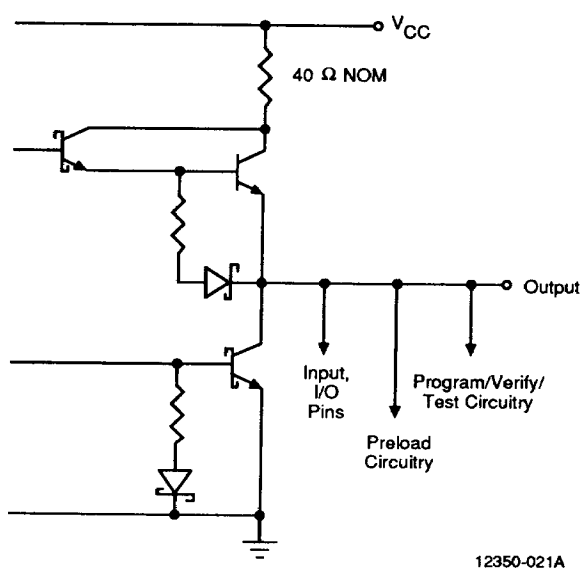
Specification		Explanation
t_{PD}, t_S, f_{MAX} (feedback)	Product Terms P_1–P_n	If only the P_1–P_n product terms are changing (XOR term is not changing)
	Product Term XOR	If XOR term is changing

INPUT/OUTPUT EQUIVALENT SCHEMATICS

Typical Input



Typical Output

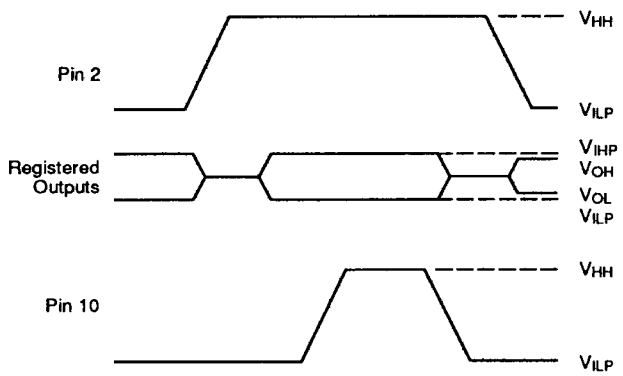


OUTPUT REGISTER PRELOAD

The Preload function allows the register to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure is as follows:

1. Raise V_{CC} to 4.5 V.
2. Disable output registers by setting pin 2 to V_{HH} (12 V).
3. Apply the desired value (V_{ILP}/V_{IHP}) to all registered output pins. Leave combinatorial outputs floating.
4. Pulse pin 10 to V_{HH}, then back to 0 V.
5. Remove V_{ILP}/V_{IHP} from all registered output pins.
6. Remove high voltage from pin 2.
7. Enable output registers per programmed pattern.
8. Verify V_{OL}/V_{OH} at all registered output pins.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
V_{HH}	Super-level input voltage	11	11.5	12	V
V_{ILP}	Low-level input voltage	0	0	0.5	V
V_{IHP}	High-level input voltage	2.4	5.0	5.5	V



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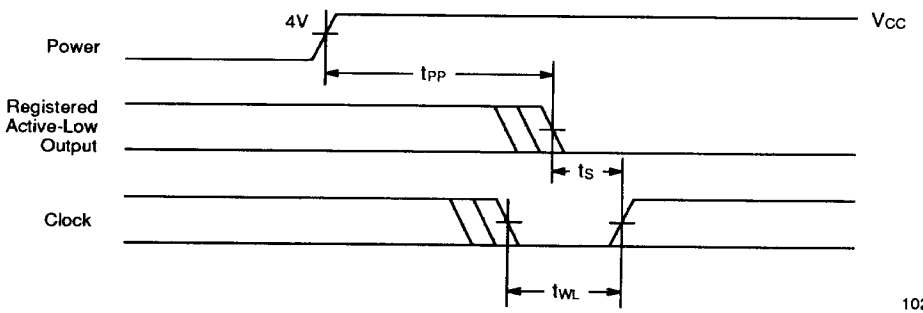
Output Register Preload Waveform

POWER-UP PRESET

The power-up preset feature ensures that all flip-flops will be preset to HIGH after the device has been powered up. The output state will depend on the programmed configuration. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up preset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up preset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following preset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Descriptions	Max.	Unit
t_{PP}	Power-Up Preset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



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Power-Up Preset Waveform