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# SSI 33R3750A
## Preamplifier for
## Magneto Optical Storage

### Advance Information

## DESCRIPTION

The 33R3750A is a custom designed BiCMOS integrated circuit. It contains the servo algebra functions and the channel preamplifier for an optical disk drive system. It is available in a 32-Lead TQFP package.

## FEATURES

### GENERAL

- Power supply range (4.5 to 5.5V)
- Low power operation (250 mW typical @ 5V)
- Small footprint 32-Lead TQFP package

### SERVO

- 1 MHz bandwidth
- Low impedance input buffer with nominal 4X gain

- SUM signal used to detect media defects
- Servo algebra signals used for optical alignment, seeking, focusing, and track following: Alignment Error Signal (AES), Tracking Error Signal (TES), Focus Error Signal (FES)

### CHANNEL

- 40 MHz bandwidth
- Switching time between ROM and MO 100 ns (max)
- Control lines for switching between ROM and MO modes and for gain selection
- Differential ROM/MO signal output

## BLOCK DIAGRAM

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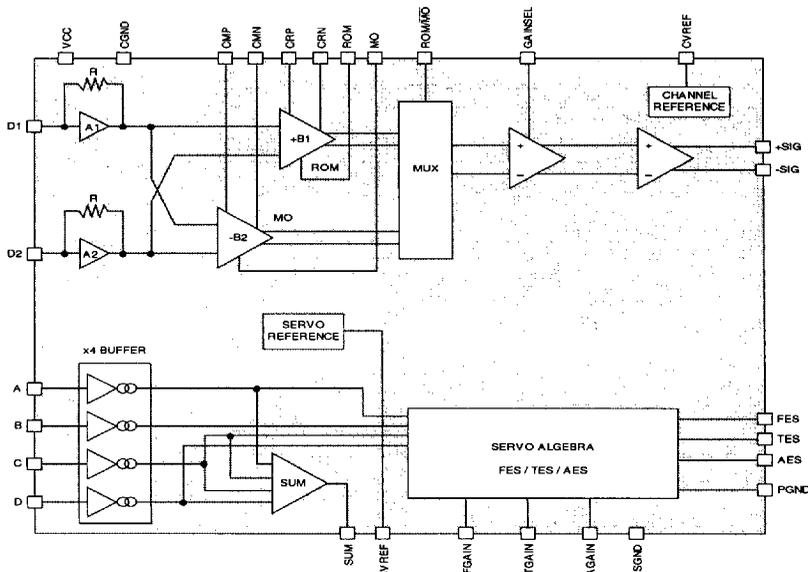
# SSI 33R3750A
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## FUNCTIONAL DESCRIPTION

### SERVO OVERVIEW

The input currents IA, IB, IC, and ID from the quad detector are used to generate the servo FES, TES, SUM, and AES signals. The AES signal is used to align the quad detector during optical head assembly.

### Buffer / Sum / Peak Detect

The Buffer circuit provides a low input impedance to the quad input signals from the photo detectors. It has a minimum bandwidth of 1 MHz and nominal gain of 4X.

The SUM signal represents the summation of IA, IB, IC, and ID with a gain of 4X. It will be used to detect media defects.

### Servo Algebra

The servo algebra signals required for optical alignment, seeking, focusing, and track following are generated from a quad detector, differential amplifiers, summing amplifiers and dividers. The divider is implemented by using logarithm and anti-logarithm circuitries. The servo algebra signals include: Focus Error Signal (FES), Tracking Error Signal (TES), and Alignment Error Signal (AES). These signals are referenced to PGND.

$V_{FES}$ = VCC/2 + FGAIN x[(D-A) / (D+A) + (B-C) / (B+C)]
where FGAIN is the voltage at pin 13

$V_{TES}$ = VCC/2 + 5TGAIN x[(B+C)-(A+D)]/(A+B+C+D)]

$V_{AES}$ = VCC/2 + 5AGAIN x[(A+B)-(C+D)]/(A+B+C+D)]
where TGAIN is the voltage at pin 11, AGAIN is the voltage at pin 19

• PGND ( Common)
Refer to as Psuedo GND = VCC/2 ±3%, and capable of stable operation for CL ≤ .01 μF.

• Svref
Refer to as Servo reference voltage. 1.5V ± 5%

## CHANNEL PREAMPLIFIER OVERVIEW

The channel section provides a minimum of 40 MHz bandwidth.

The MO data signal is generated by two photodetectors (D1 and D2). The photo-currents from D1 and D2 are converted to a voltage by the transimpedance amplifiers A1 and A2.The difference amplifier B2 generates the Magneto Optical signal, Vmo.

Vmo = K1 ( Id1 - Id2)
where K1 = (transimpedance gain, R) (difference amplifier gain) with a value of 48 kΩ nominal.

The reflectivity signal (Vrom) is generated by the sum amplifier B1.

Vrom = K2 x (Id1 + Id2)
where K2 = (transimpedance gain, R)(summing amplifier gain) with a value of 6 kΩ nominal.

The digital I/O line ROM/$\overline{\text{MO}}$ controls the internal analog multiplexer for MO or ROM modes. The select lines ROM and MO control the ROM and MO signals into the multiplexer input respectively. The capacitors C1 and C2 maintain the DC component of the ROM and MO signals when they are disconnected from the multiplexer input (reference Table 2).

The GainSel line can change the overall gain by 3.0 times when asserted low, and the differential output is an open collector stage capable of driving a low impedance flex cable down to 100Ω single ended.

Cvref is the channel reference voltage = 1.5V ± 5%.

Note: A 0.1 μF capacitor at SVREF and CVREF to reduce noise is permitted.

### TABLE 1: Input Contrast

|  | FES | TES | AES |
|---|---|---|---|
| Input Contrast | $\left(\dfrac{D-A}{D+A}\right)+\left(\dfrac{B-C}{B+C}\right)$ | $\dfrac{(B+C)-(A+D)}{A+B+C+D}$ | $\dfrac{(A+B)-(C+D)}{A+B+C+D}$ |

## MODE SELECT OVERVIEW

The following table contains the mode select lines which control the MO and ROM signals:

**TABLE 2:  Mode Select Lines**

| MO | ROM | ROM / $\overline{\text{MO}}$ | MODE |
|----|-----|------------|------|
| 0 | 0 | X | ROM and MO disabled (DC on C1,C2 maintained) |
| 0 | 1 | 1 | ROM enabled (DC on C2 maintained) |
| 1 | 0 | 0 | MO enabled (DC on C1 maintained) |

## PIN DESCRIPTION

### POWER SUPPLY PINS

| NAME | TYPE | DESCRIPTION |
|------|------|-------------|
| VCC | - | +5V Supply |
| SGND | - | Servo Ground (see Note 1) |
| CGND | - | Channel Ground (see Note 1) |

### INPUT PINS

| | | |
|------|------|-------------|
| D1,D2 | I | Data Detector 1,2. Photo detector inputs generating the MO and ROM signals. |
| DA,DB,DC,DD | I | Segments A,B,C,D of the Quad detectors. |
| GainSel | I | Gain Select (TTL). A 1x or 3x (active low) gain may be selected. |
| ROM/$\overline{\text{MO}}$ | I | ROM/$\overline{\text{MO}}$ Selection (TTL). A low level selects the MO signal through the multiplexer, and a high level selects the ROM signal. |
| ROM | I | ROM Transient (TTL). A low level opens the ROM line. |
| MO | I | MO Transient (TTL). A low level opens the MO line. |

Note 1: SGND and CGND are separate grounds on the chip. Both need external ground connections for proper operation.

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## PIN DESCRIPTION (continued)

### OUTPUT PINS

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| SUM | O | Quad Sum Signal. The sum of the IA, IB, IC, and ID inputs. |
| AES | O | Alignment Error Signal. Servo function of the IA, IB, IC, and ID inputs. Referenced to PGND. |
| FES | O | Focus Error Signal. Servo function of the IA, IB, IC, and ID inputs. Referenced to PGND. |
| TES | O | Track Error Signal. Servo function of the IA, IB, IC, and ID inputs. Referenced to PGND. |
| PGND | O | Psuedo Ground. VCC/2 reference for servo. |
| ±Sig | O | Differential Data Outputs. ROM/MO signal output. |
| Cvref | O | Vref for Channel. Channel voltage reference. |

### ANALOG PINS

| TGAIN | - | Tracking Gain. Controls the tracking gain variable in the TES signal. |
|---|---|---|
| FGAIN | - | Focus Gain. Controls the tracking gain variable in the FES signal. |
| AGAIN | - | Alignment Gain. Controls the tracking gain variable in the AES signal. |
| Svref | - | Vref for Servo. Reference for ROM and PKDET outputs. |
| C1 (CRP, CRN) | - | Rom AC Pole Cap. This hold the DC component of the ROM signal during MO operation. |
| C2 (CMP, CMN) | - | MO AC Pole Cap. This hold the DC component of the MO signal during ROM operation. |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS
Operation beyond the maximum ratings may damage the device.

| PARAMETER | RATING |
|---|---|
| Operating Temperature | 0 to 70°C |
| Storage Temperature | -65 to 150°C |
| Junction Operating Temperature | 135°C |
| Operating Supply Voltage | 4.5V (min.), 5V (typ.), 5.5V (max.) |
| Maximum Supply Voltage | 6V |

### RECOMMENDED OPERATING CONDITIONS
Unless otherwise specified, the recommended operating conditions are as follows: $4.5V < Vcc < 5.5V$

| | | |
|---|---|---|
| Ambient Temperature | Ta | $0°C < Ta < 70°C$ |
| Junction Operating Temperature | Tj | $25°C < Tj < 135°C$ |

Currents flowing into the chip are positive. Current maximums are currents with the highest absolute value.

### POWER SUPPLY CURRENT AND POWER DISSIPATION

| PARAMETER | CONDITION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Operating Supply Current | | | 50 | 62 | mA |
| Total Module Power Dissipation at +5V | | | 250 | 340 | mW |

### INPUTS AND OUTPUTS

### TTL COMPATIBLE INPUTS

| | | | | | | |
|---|---|---|---|---|---|---|
| Input low voltage | VIL | 5V, 25°C | 0 | | 0.8 | V |
| Input high voltage | VIH | 5V, 25°C | 2 | | | V |
| Input low current | VIL | VIL = 0.8V | | | -0.4 | mA |
| Input high current | VIH | VIH = 2.4V | | | 100 | µA |

### BUFFER CIRCUIT SPECIFICATIONS

| | | | | | |
|---|---|---|---|---|---|
| Quad Input | IAQ, IBQ, ICQ, IDQ | 0.3 | 1.6 | 40.0 | µA |
| Current Gain to Output | IAb, IBb, ICb, IDb | | 4 | | X |
| Gain Tracking from each Input | | | 2 | | % |
| Bandwidth | Cin = 10 pF | 1 | | | MHz |

### SUM SIGNAL SPECIFICATIONS

| | | | | | |
|---|---|---|---|---|---|
| Input from Buffer | IAb, IBb, ICb, IDb | 1.2 | 6.4 | 160 | µA |
| Bandwidth | | 1 | | | MHz |
| Current Gain from Quad Input to Sum | | | 4 | | X |

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## ELECTRICAL SPECIFICATIONS (continued)

### SERVO ALGEBRA SPECIFICATIONS

| | | | | | |
|---|---|---|---|---|---|
| Psuedo Ground Level | ≤10 nF capacitance<br>$I_L$ ≤ 5 mA<br>Measured in % of supply voltage | 47 | 50 | 53 | % |
| Svref (Servo Reference Voltage) | $I_L$ ≤ 1.5 mA | 1.425 | 1.5 | 1.575 | V |

### FES SPECIFICATIONS (see Notes 2, 3 & 4)

| | | | | | |
|---|---|---|---|---|---|
| Bandwidth | 0.3 µA Quad Input (-3 dB) | 100 | | | kHz |
| Algebra Error          Linearity | DC to 100 kHz | -3 | 0 | 3 | % |
| Offset | Reference to PGND | | | | |
| | measured at 0.5 µA | -50 | 0 | 50 | mV |
| | measured at 5 µA | -50 | 0 | 50 | mV |
| Thermal Drift | | -0.1 | 0.0 | 0.1 | mV/°C |
| Output Voltage Diff.<br>pk - pk | Input contrast ±1.0<br>FGain setting = 0.50V | | 1.0 | | Vp-p |

### TES SPECIFICATIONS (see Notes 2, 3 & 4)

| | | | | | |
|---|---|---|---|---|---|
| Bandwidth | 0.3 µA Quad Input (-3 dB) | 1 | | | MHz |
| Algebra Error          Linearity | DC to 100 kHz | -3 | 0 | 3 | % |
| Offset<br>pk - pk | Reference to PGND | | | | |
| | measured at 0.5 µA | -50 | 0 | 50 | mV |
| | measured at 5 µA | -50 | 0 | 50 | mV |
| Thermal Drift | | -0.1 | 0 | +0.1 | mV/°C |
| Output Voltage Diff. | Input contrast ±0.25<br>TGain setting = 0.40V | | 1.0 | | Vp-p |

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## AES SPECIFICATIONS (see Notes 2, 3 & 4)

| PARAMETER | CONDITION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Bandwidth | 0.3 µA Quad Input (-3 dB) | 1 | | | MHz |
| Algebra Error          Linearity | DC to 100 kHz | -3 | 0 | 3 | % |
| Offset | Reference to PGND | | | | |
| | measured at 0.5 µA | -50 | 0 | 50 | mV |
| | measured at 5 µA | -50 | 0 | 50 | mV |
| Thermal Drift | | -0.1 | 0.0 | 0.1 | mV/°C |
| Output Voltage Diff. pk - pk | Input contrast ±0.25 TGain setting = 0.40V | | 1.0 | | Vp-p |

Note 2: FES, TES, and AES provide an output of 1 Vp-p at 1 MHz without any slew rate distortion. The loading characteristic is CL = 30 pF and RL = 10 kΩ.

Note 3: All outputs have a minimum drive capability of 1 mA.

Note 4: Limits on Gain inputs: 0V ≤ V(FGAIN, TGAIN, AGAIN) ≤ 0.6V.

## CHANNEL SPECIFICATIONS

| | | | | | |
|---|---|---|---|---|---|
| Overall Bandwidth | Cin = 4 pF, CL = 15 pF RL = 100Ω per side | 40 | | | MHz |
| Equiv. Input Noise Current (MO) | Cin = 4 pF, 20 MHz BW | | 2.5 | 3 | pA/√Hz |
| Equiv. Input Noise Current (ROM) | Cin = 4 pF, 20 MHz BW | | 5.5 | 6.3 | pA/√Hz |
| Overall MO Gain | Unity Gain Select | 40.8 | 48 | 55.2 | kΩ |
| Overall ROM Gain | Unity Gain Select | 5.1 | 6 | 6.9 | kΩ |
| DC Photocurrent Input (Id1 or Id2) | | 1.8 | | 30 | µA |
| AC Input Signal for ROM (per detector) | | 1.5 | | 15 | µA |
| MO Signal Input (Id1-Id2) | | 0.3 | | 5 | µA |
| CMRR of Diff. Amp. | 20 MHz BW | 25 | 30 | | dB |
| MO/ROM Output Range | 20 MHz BW, < 3% THD | 5 | 6 | | mA p-p |
| Output AC Load/Side | | | 100 | | Ω |
| Volt. Droop of C1,C2 (C1 = C2 = 0.2 µF) | | | | 5 | µV/µs |
| Gain Mismatch of Transimpedance Amps | | | | 2 | % |
| MO to ROM Gain Ratio | | 7.6 | 8 | 8.4 | Ω/Ω |
| Amplitude Response Ripple | 20 MHz BW | -0.5 | 0.0 | 0.5 | dB |

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## CHANNEL SPECIFICATIONS (continued)

| PARAMETER | CONDITION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Phase Response Ripple | 20 MHz BW | -2 | 0 | 2 | ° |
| Switching Time | ROM/$\overline{MO}$, ROM, MO | | | 100 | ns |
| Gain Ratio for GainSel | | | 3 | | X |
| Cross Talk from ROM to MO path at 10 MHz | | 35 | | | dB |
| AC poles for C1 = C2 | Max cap size = 0.7 μF | | 200 | 400 | Hz |
| DC Bias at Detector Out | D1 and D2 | | 0.7 | 0.9 | V |
| PSRR | Over 10 MHz | 35 | 40 | | dB |

Note: The above specifications are for the operating voltage and temperature range unless otherwise stated.
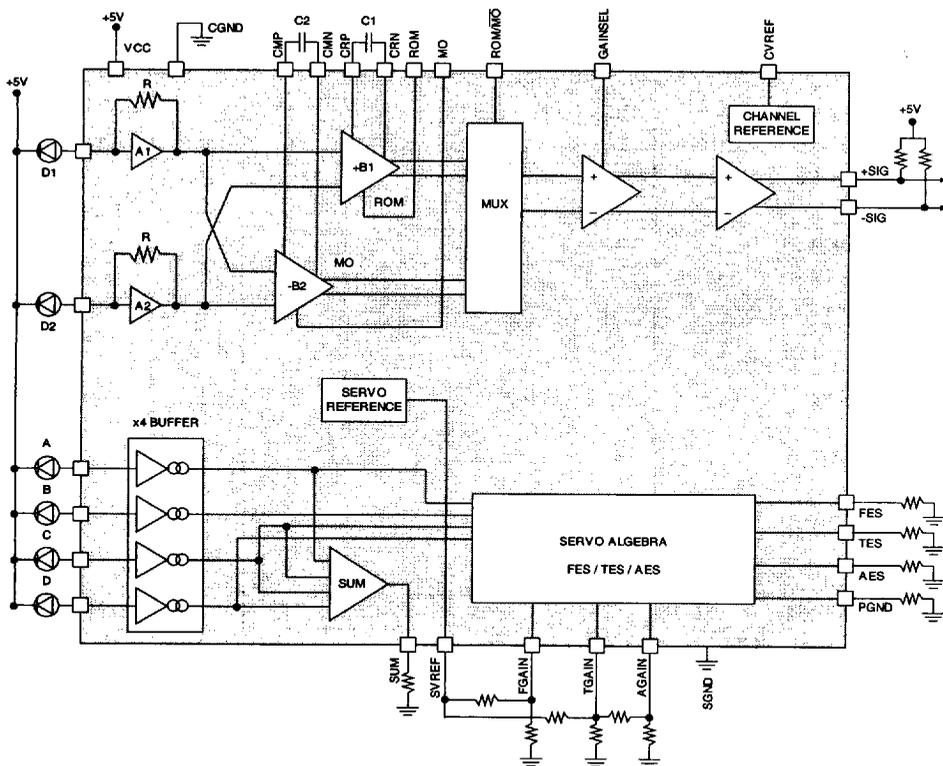


**FIGURE 1: Applications Diagram**

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## PACKAGE PIN DESIGNATIONS
(Top View)

Pin designations (32-Lead TQFP):

Top row (pins 32–25): CRN (32), CRP (31), ROM (30), MO (29), CMP (28), CMN (27), ROM/MO (26), CVREF (25)

Left side:
- 1 — CGND
- 2 — D2
- 3 — D1
- 4 — A
- 5 — B
- 6 — C
- 7 — D
- 8 — SGND

Right side:
- 24 — GAINSEL
- 23 — SIG+
- 22 — SIG-
- 21 — NC
- 20 — NC
- 19 — A GAIN
- 18 — NC
- 17 — FES

Bottom row (pins 9–16): VCC (9), SUM (10), TGAIN (11), SVREF (12), FGAIN (13), PGND (14), AES (15), TES (16)
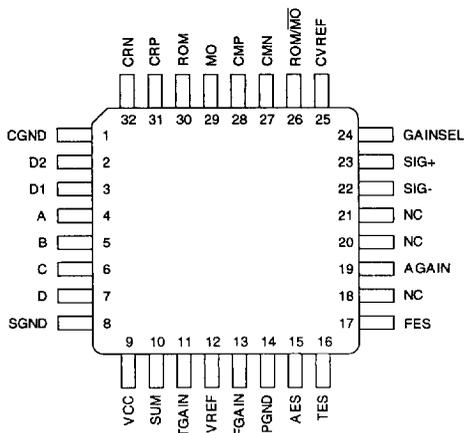
**32-Lead TQFP**

CAUTION: Use handling procedures necessary for a static sensitive component.

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