REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																								
SHEET																								
REV																								
SHEET	22	23	24	25	26	27	28	29																

REV STATUS OF SHEETS	REV																						
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE: 91-08-16

REVISION LEVEL:

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS EE PROGRAMMABLE READ ONLY MEMORY 256 X 16 MONOLITHIC SILICON

SIZE	CAGE CODE	5962-91549
A	67268	

SHEET 1

DESC FORM 193
SEP 87

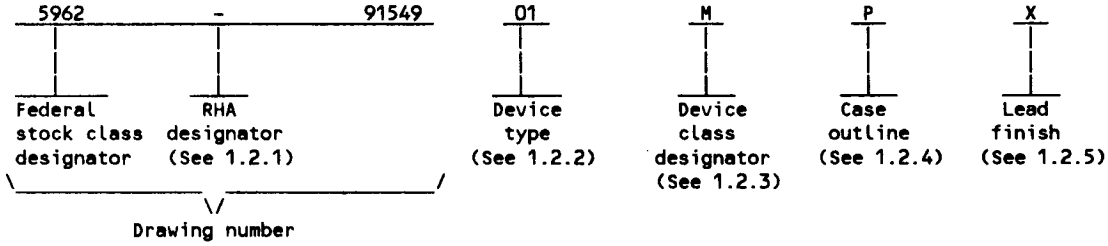
* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E256

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	93CS66	4096-Bit serial electrically erasable programmable memory

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). For device classes M, B, and S, case outline(s) shall meet the requirements in appendix C of MIL-M-38510 and as listed below. For device classes Q and V, case outline(s) shall meet the requirements of MIL-I-38535, appendix C of MIL-M-38510, and as listed below.

Outline letter	Case outline
P	D-4 (8-lead, .405" x .310" x .200") dual-in-line package

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

All input or output voltages with respect to gnd	+6.5 V to -0.3 V
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J) 2/	+150°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-M-38510, appendix C
Thermal resistance, junction-to-ambient (Θ_{JA})	+200°C/W
Power dissipation (P_D)	80 mW
Endurance	10,000 program/erase cycles(minimum)
Data retention	10 years (minimum)

1.4 Recommended operating conditions.

Positive power supply	+4.5 V to +5.5 V
Ambient operating temperature range (T_A)	-55°C to +125°C
Supply voltage (V_{SS})	0.0 V dc
High level input voltage range (V_{IH})	2.0 V dc to V_{CC} + 1.0 V dc
Low level input voltage range (V_{IL})	-0.1 V dc to 0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 3/

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
3/ When a QML source exists, a value shall be provided.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the characterization of LATCH-UP in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Pennsylvania Avenue, N.W., Washington, DC 20006.)

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, Pennsylvania 19103).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Instruction set. The instruction set shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be as specified in 4.4.5e.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-ECS of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 42 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

3.12 Processing of EEPROMs. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.12.1 Conditions of the supplied devices. Devices will be supplied in cleared state (Logic "0's"). No provision will be made for supplying written devices.

3.12.2 Read-write procedures. Correct read-write procedures shall be as specified in 4.6.3.

3.12.3 Verification of state of EEPROMs. When specified, devices shall be verified as either written to the specified pattern or cleared. As a minimum, verification shall consist of performing a read of the entire array to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure and the device shall be removed from the lot or sample.

3.13.4 Power supply sequence of EEPROMs. In order to reduce the probability of inadvertent writes, the following power supply sequences shall be observed:

a. A logic low state shall be applied to $\overline{CS}$ at the same time or before the application of V_{CC}.

b. A logic low state shall be applied to $\overline{CS}$ at the same time or before the removal of V_{CC}.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Delete the sequence specified as 3.1.9 - 3.1.13 (preburn-in electrical parameters through interim postburn-in electrical parameters of method 5004) and substitute lines 1 through 6 of table IIA herein.

b. Prior to burn in, the devices shall be programmed (see 4.6 herein) with a checkerboard pattern or equivalent (manufacturers at their option may employ an equivalent pattern provided it is a topologically true alternating bit pattern). The pattern shall be read before and after burn in. Devices having bits not in the proper state after burn in shall constitute a device failure and shall be included in the PDA calculation and shall be removed from the lot (see 4.2.3 herein).

c. For device class M the burn-in test circuit shall be submitted to DESC-ECS for review with the certificate of compliance. For device classes B and S the burn-in test circuit shall be submitted to the qualifying activity.

(1) Static burn-in for device classes S (method 1015 of MIL-STD-883, test condition A).

(a) All inputs shall be connected to GND. Outputs may be open or connected to 4.5 V minimum. Resistors R1 are optional on both inputs and outputs, and required on outputs connected to V_{CC}±0.5 V. R1 = 220 ohms to 47 kohms. For static II burn-in, reverse all input connections (i.e. V_{SS} to V_{CC}).

(b) V_{CC} = 4.5 V minimum.

(c) Ambient temperature (T_A) shall be +125°C minimum.

(d) Test duration for the static test shall be 48 hours minimum. The 48 hour burn-in shall be broken into two sequences of 24 hours each (Static I and Static II) followed by interim electrical measurements.

(2) Dynamic burn-in for device classes M, B, and S (method 1015 of MIL-STD-883, test condition D or F) using the circuit submitted (see 4.2.1c herein).

d. Interim and final electrical parameters shall be as specified in table IIA herein.

e. For classes S and B devices, post dynamic burn-in electrical parameter measurements may, at the manufacturer's option, be performed separately or included in the final electrical parameter requirements.

f. An endurance test including a data retention bake, per method 1033 of MIL-STD-833, prior to burn in (e.g. may be performed at wafer sort) shall be included as part of the screening procedure, with the following conditions:

(1) Cycling may be chip, block, byte or page at equipment room ambient and shall cycle all bytes a minimum of 10,000 cycles.

(2) After cycling, perform a high temperature unbiased storage 48 hours at 150°C minimum. The storage time may be accelerated by a higher temperature in accordance with the Arrhenius relationship and with the apparent activation energy of .6 eV. The maximum storage temperature shall not exceed 200°C for assembled devices and 300°C for unassembled devices. All devices shall be programmed with a charge opposite the state that the cell would read in its equilibrium state (e.g. worst case pattern, see 3.12.2 herein).

(3) Read the data retention pattern and test using subgroups 1, 7, and 9 (at the manufacturer's option high temperature equivalent subgroups 2, 8A, and 10 or low temperature equivalent subgroups 3, 8B, and 11 may be used in lieu of subgroups 1, 7, and 9) after cycling and bake, but prior to burn in. Devices having bits not in the proper state after storage shall constitute a device failure.

g. After the completion of all screening, the devices shall be erased and verified prior to delivery.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be submitted to DESC-ECS with the certificate of compliance and shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535 and as detailed in table IIB herein.

4.2.3 Percent defective allowable (PDA).

a. The PDA for class S devices shall be 5 percent for static burn-in and 5 percent for dynamic burn-in, based on the exact number of devices submitted to each separate burn-in.

b. The PDA for class B devices shall be in accordance with MIL-M-38510 for dynamic burn-in.

c. Static burn-in I and II failures shall be cumulative for determining PDA.

d. Those devices whose measured characteristics, after burn-in, exceed the specified delta (table IIc) limits or electrical parameter limits specified in table IA, subgroup 1, are defective and shall be removed from the lot. The verified failures divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot and the lot shall be accepted or rejected based on the specifed PDA.

e. The PDA for device classes Q and V shall be in accordance with MIL-I-38535 for dynamic burn-in.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.1.1 Qualification extension for device class B or S. When authorized by the qualifying activity, if a manufacturer qualifies one device type which is identical (i.e., same die), to other device types on this specification, the slower device types may be part I qualified, upon the request of the manufacturer, without any further testing. The faster device types may be part I qualified by performing only group A qualification testing.

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.3 Electrostatic discharge sensitivity inspection. Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015. ESDS testing shall be measured only for initial qualification and after process or design changes which may affect ESDS classification.

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the instruction set table. For device classes B and S, subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. Procedures and circuits shall be submitted to DESC-ECS for class M devices. For classes B and S the procedures and circuits shall be submitted to the qualifying activity. For classes Q and V the procedures and circuits shall be submitted to DESC-ECS and shall be as indicated in the QM plan and will be under the control of the device manufacturer's technical review board (TRB). Testing shall be on all pins, on 5 devices with zero failures. Latch-up test shall be considered destructive.

d. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is fifteen devices with no failures, and all input and output terminals tested.

e. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified, (except device submitted for groups B, C, and D testing).

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{SS} = 0 V; 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Supply current active CMOS level	I_{CC1}	V_{CC} = 5.5 V, V_{SK} = 0, f_{SK} = .5 MHz, V_{CS} = 5 V, V_I = 0 or 5 V	1,2,3	01		2	mA
Supply current active TTL level	I_{CC2}	V_{CC} = 5.5 V, V_{SK} = .8 to 2 V f_{SK} - .5 MHz, V_{CS} = V_{IH}, other V_I = $V_{IH/L}$	1,2,3	01		4	
Supply current CMOS standby	I_{CC3}	V_{CC} = 5.5 V, V_{SK} = 0 to 5 V, f_{SK} = 0 Hz, V_{CS} = 0 V, other V_I = $V_{IH/L}$	1,2,3	01		100	µA
Logical "0" input leakage current	I_{IL}	V_{CC} = 5.5 V, V_I = 0 V	1,2,3	01	-10		
Logical "1" input leakage current	I_{IH}	V_{CC} = 5.5 V, V_I = 5.5 V	1,2,3	01		10	
Logical "0" output leakage current	I_{OLZ}	V_{CC} = 5.5 V, DO TRI-STATE, V_{DO} = 0 V	1,2,3	01	-10		
Logical "1" output leakage current	I_{OHZ}	V_{CC} = 5.5 V, DO TRI-STATE, V_{DO} = 5.3 V	1,2,3	01		10	
Logical "0" input voltage	V_{IL}	V_{CC} = 4.5 V	1,2,3	01	-.1	.8	V
Logical "1" input voltage	V_{IH}	V_{CC} = 5.5 V	1,2,3	01	2	V_{CC}+1	
Logical "0" output voltage	V_{OL1}	V_{CC} = 4.5 V, I_{OL} = 1.8 mA	1,2,3	01		.4	
	V_{OL2}	V_{CC} = 4.5 V, I_{OL} = 10 µA				.2	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{SS} = 0 V; 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Logical "1" output voltage	V_{OH1}	V_{CC} = 4.5 V, I_{OH} = -400 µA	1,2,3	01		2.4	V
		V_{CC} = 4.5 V, I_{OH} = -10 µA				VCC-.2	
Input capacitance	C_I	V_{CC} = 5.5 V, V_{IN} = 2 V, f = 1 MHz 1/	4	01		8	pF
Output capacitance	C_O	V_{CC} = 5.5 V, V_O = 2 V, f = 1 MHz 1/	4	01		10	
		AC Testing 2/					
SK clock frequency	f_{SK}	V_{CC} = 4.5 V 3/	9,10,11	01	0	.5	MHz
SK high time	t_{SKH}	V_{CC} = 4.5 V 3/	9,10,11	01	500		ns
SK low time	t_{SKL}	V_{CC} = 4.5 V 3/	9,10,11	01	500		
CS low time	t_{CS}	V_{CC} = 4.5 V 4/	9,10,11	01	500		
CS setup time	t_{CSS}	V_{CC} = 4.5 V, Relative to SK rising See figure 3	9,10,11	01	100		
DI setup time	t_{DIS}		9,10,11	01	200		
PRE setup time	t_{PRES}		9,10,11	01	100		
PE setup time	t_{PES}		9,10,11	01	100		
CS hold time	t_{CSH}	V_{CC} = 4.5 V Relative to SK falling	9,10,11	01	0		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{SS} = 0 V; 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
DI hold time	t_{DIH}	V_{CC} = 4.5 V, Relative to SK rising See figure 3	9,10,11	01	200		ns
PE hold time	t_{PEH}	V_{CC} = 4.5 V, Relative to CS falling See figure 3	9,10,11	01	500		
PRE hold time	t_{PREH}		9,10,11	01	0		
Output delay to "1"	t_{PD1}	V_{CC} = 4.5 V, Relative to SK rising See figure 3	9,10,11	01		1000	
Output delay to "0"	t_{PD0}		9,10,11	01		1000	
CS to status valid	t_{SV}		9,10,11	01		1000	
CS to DO in tri-state	t_{DF}	V_{CC} = 5.5 V, Relative to CS falling See figure 4	9,10,11	01		1000	
Write cycle time	t_{WP}		9,10,11	01		10	ms

1/ Tested initially and after any design or process changes which may affect this parameter, and therefore guaranteed to the limits specified in table IA.

2/ Tested by application of specified timing signals and conditions.
Equivalent A.C. test conditions:
Output load: See figure 5.
Input rise and fall times <= 10 ns.
Input pulse levels: 0.4 and 2.4 V.
Timing measurement reference levels:
Inputs 1 V. and 2 V.
Outputs 0.8 V. and 2 V.

3/ The SK frequency sepcification is for a minimum 5K clock period of 2 us, therefore in a 5K clock cycle tSKH + tSKL must be greater than or equal to 2 us.

4/ CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

TABLE IB. Single event phenomena (SEP) test limits. 1/ 2/

Device type	Temperature (±10°C)	Memory pattern	V_{CC} = 4.5 V Effective LET no upsets (Mev/(mg/cm^2))	V_{CC} = 4.5 V Maximum device cross section (cm^2) (LET = 3/)	Bias for latchup test V_{CC} = 5.5 V no latchup LET

1/ This table blank, table will be filled in when a qualified vendor exsists.
2/ For SEP test conditions see 4.4.5 herein.
3/ Value to be determined.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table IIA herein.

a. For device class S only steady-state life test circuits shall be conducted using test condition D and the circuit described in 4.2.1c herein, or equivalent as approved by the qualifying activity.

b. For device class S only, end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 5 of group B inspections and shall consist of tests specified in table IIC herein.

c. All devices selected for class S electrical testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing the devices shall be erased and verified, (except devices submitted to group C and D).

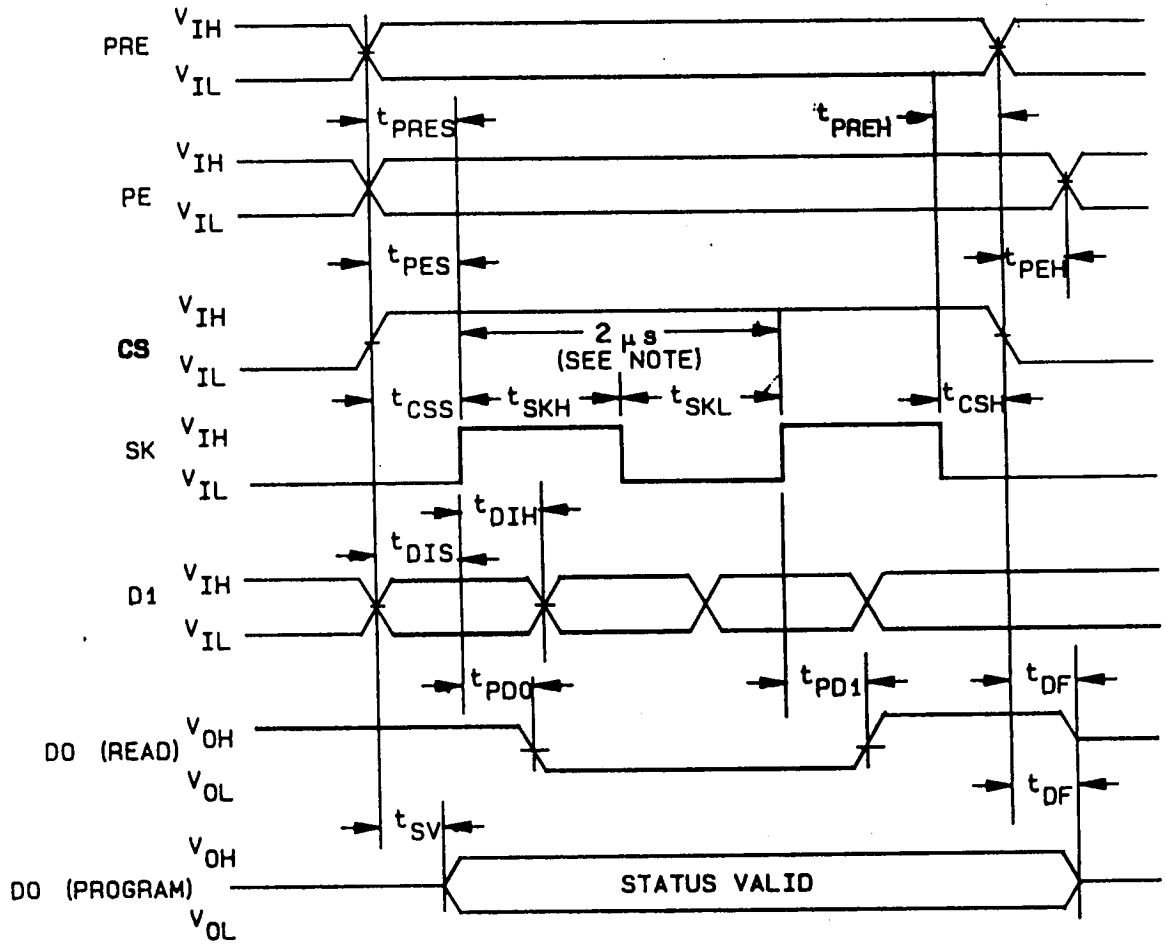
Device type	01
Case outline	P
Terminal number	Terminal symbol
1	CS
2	SK
3	DI
4	DO
5	GND
6	PE
7	PRE
8	V_{CC}

FIGURE 1. Terminal connections.

Instruction	SB	Op Code	Address	Data	PRE	PE	Comments
READ	1	10	A7-A0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXXXX		0	1	Write enable must precede all programming modes
WRITE	1	01	A7-A0	D15-D0	0	1	Writes register if address is unprotected.
WRALL	1	00	01XXXXXX	D15-D0	0	1	Writes all registers. Valid only when Protect Register is cleared.
WDS	1	00	00XXXXXX		0	X	Disables all programming instructions.
PRREAD	1	10	XXXXXXXX		1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXXXX		1	1	Must immediately precede PRCLEAR,PRWRITE, and PRDS instructions.
PRCLEAR	1	11	11111111		1	1	Clears the "protect register" so that no registers are protected from WRITE
PRWRITE	1	01	A7-A0		1	1	Programs address into Protect Register. Thereafter, memory addresses≥ the address in Protect Register are protected from WRITE.
PRDS	1	00	00000000		1	1	One time only instruction after which the address in the Protect Register cannot be altered.

FIGURE 2. Instruction set

Synchronous data timing

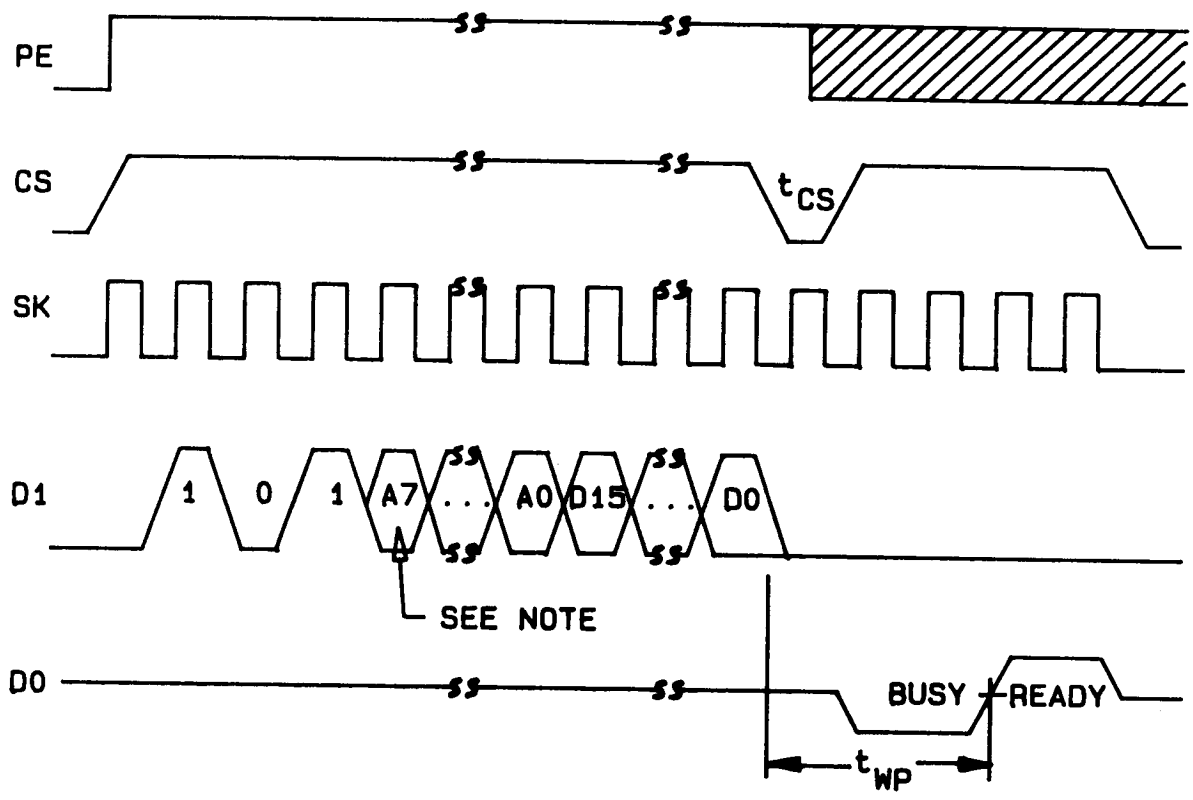


NOTE: This is the minimum SK period.

FIGURE 3. Timing waveform.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-91549
		REVISION LEVEL	SHEET 14

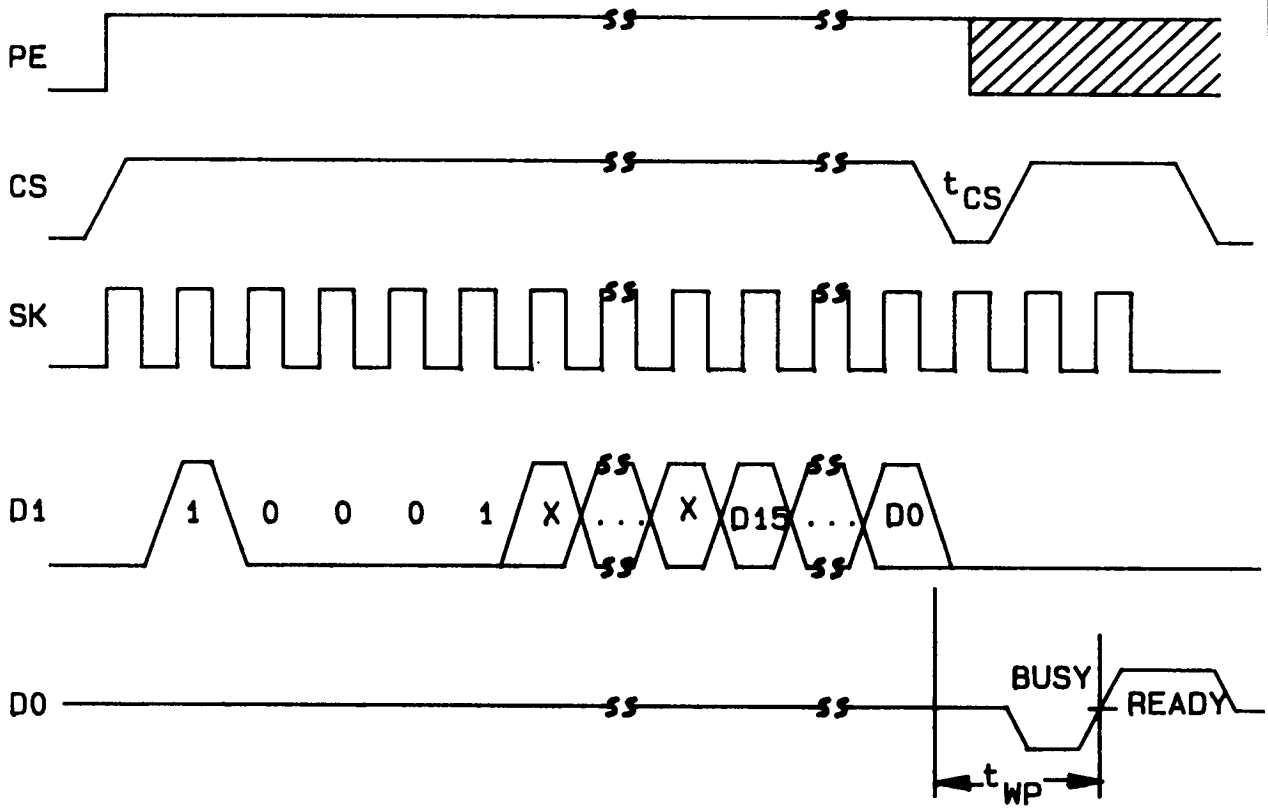
WRITE: PRE = 0
(see note)



NOTE: Address bit A7 becomes a "don't care" for NMC93CS56.

FIGURE 4. Timing diagrams.

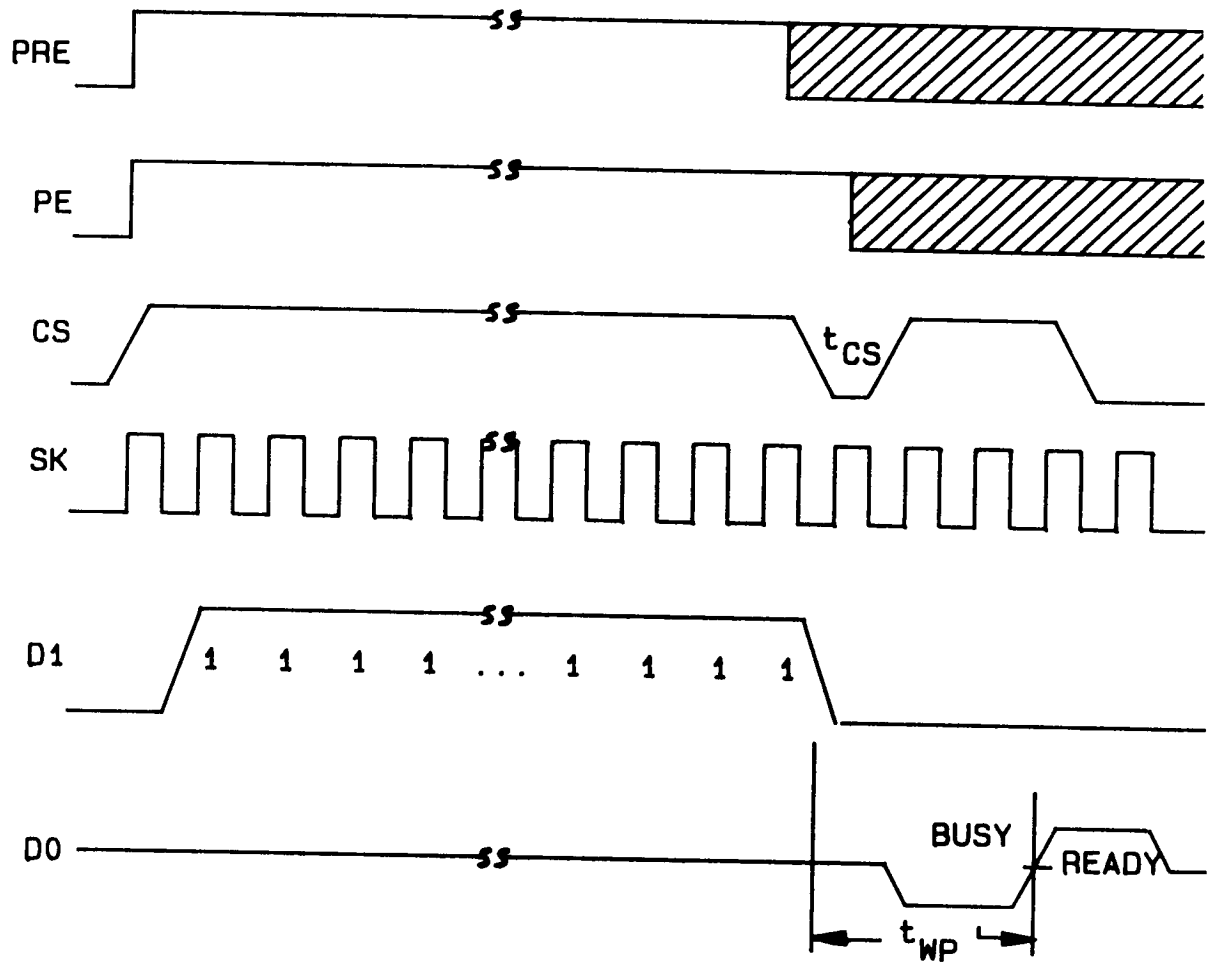
WRALL: PRE = 0
(see note)



NOTE: Protect Register must be cleared.

FIGURE 4. Timing diagrams - Continued.

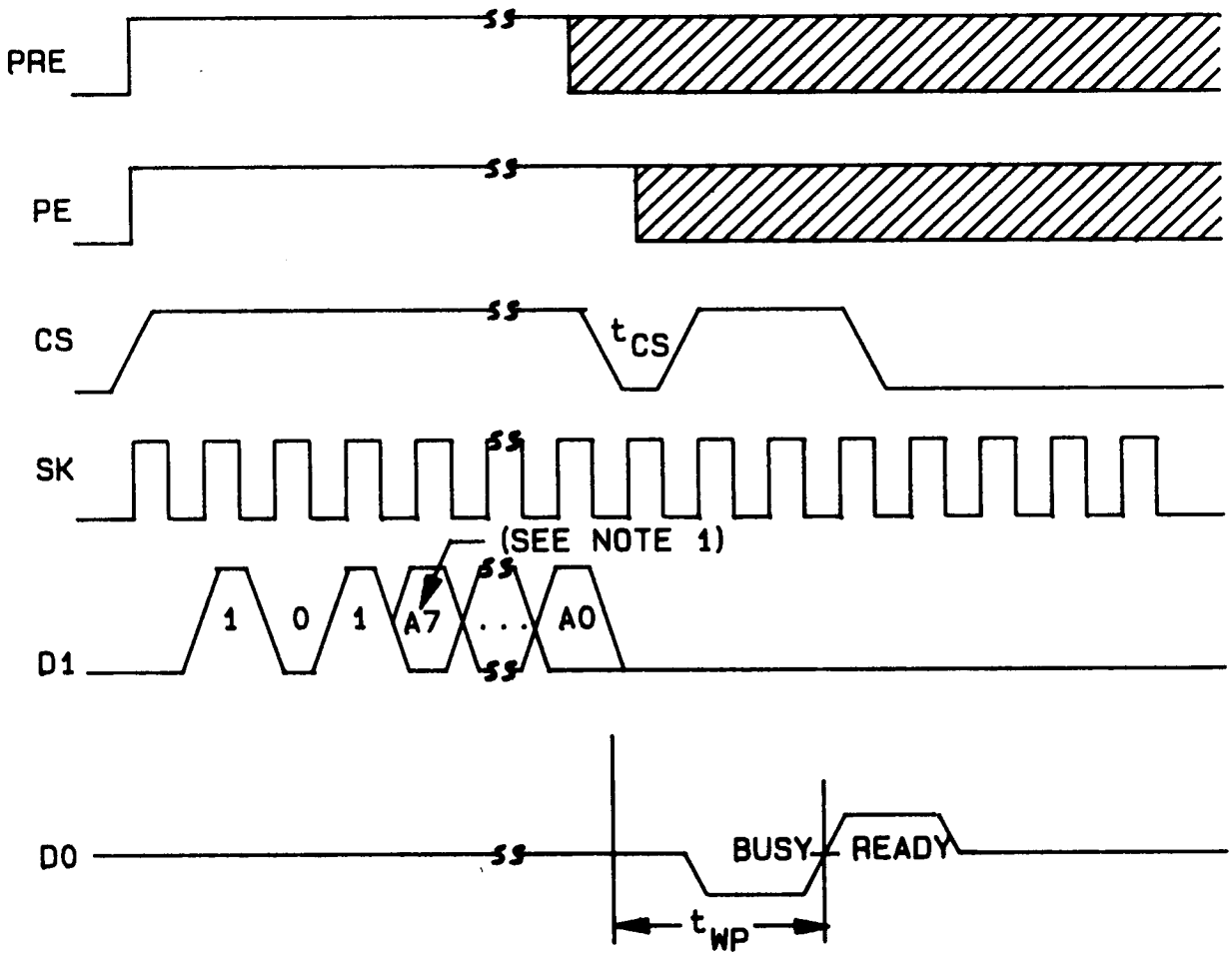
PRCLEAR: (see note)



NOTE: A PREN cycle must immediately precede a PRCLEAR cycle.

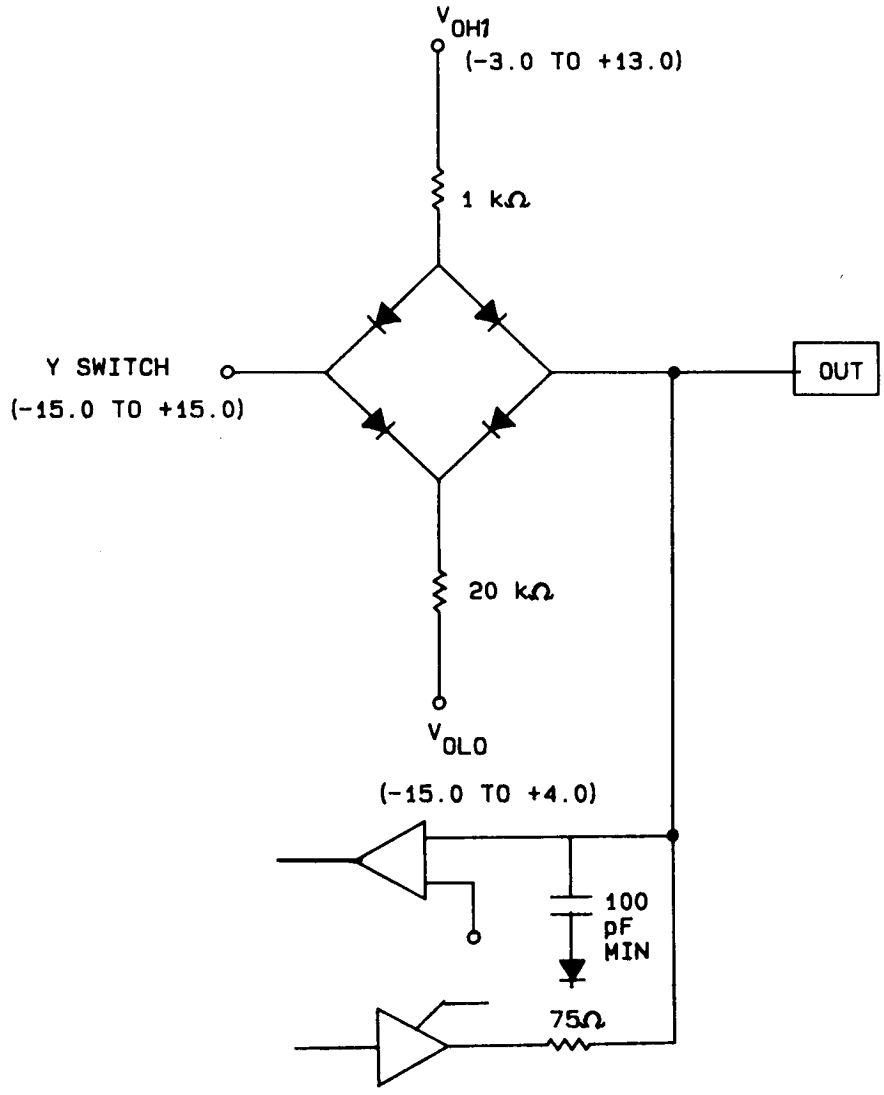
FIGURE 4. Timing diagrams - Continued.

PRWRITE: (see note 2)



NOTES:
1. Address bit A7 becomes a "don't care" for NMC93CS56.
2. Protect Register must be cleared before a PRWRITE cycle. A PREN cycle must immediately precede a PRWRITE cycle.

FIGURE 4. Timing diagrams - Continued.



NOTE: V_{OH1} and V_{OLO} will be adjusted to meet load conditions of table I.

FIGURE 5. Switching load circuit.

Note: When a qualified source exists, a circuit shall be provided and placed on this page.

FIGURE 6. Radiation Hardness bias circuit.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/

Line no.	Test requirements	Subgroups (per method 5005 table I)			Subgroups (per MIL-I-38535, table III)	
		Device class M	Device class B	Device class S	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1,7,9 or 2,8A,10	1,7,9 or 1,2,8A,10	1,7,9 or 2,8A,10	1,7,9 or 1,2,8A,10
2	Static burn-in I & II method 1015	Not required	Not required	Required	Not required	Required
3	Same as line 1			1*,7*Δ		1*,7*Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required	Required	Required
5	Same as line 1			1*,7*Δ		1*,7*Δ
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9, 10,11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9, 10,11
7	Group A test requirements	1,2,3,4**, 7,8A,8B,9, 10,11	1,2,3,4**, 7,8A,8B,9, 10,11	1,2,3,4**, 7,8A,8B,9, 10,11	1,2,3,4**, 7,8A,8B,9, 10,11	1,2,3,4**, 7,8A,8B,9, 10,11
8	Group B end-point electrical parameters			1,2,3,7,8A, 8B,9,10,11 10,11Δ		1,2,3,7, 8A,8B,9, 10,11Δ
9	Group C end-point electrical parameters	2,3,7, 8A,8B	1,2,3,7,8A, 8B,9,10,11 Δ 7/		1,2,3,7,8A, 8B,9,10,11 Δ 7/	
10	Group D end-point electrical parameters	2,3,7, 8A,8B	2,3,7, 8A,8B	2,3,7 8A,8B	2,3,7, 8A,8B	2,3,7, 8A,8B
11	Group E end-point electrical parameters	1,7,9, 8A,8B	1,7,9, 8A,8B	1,7,9 8A,8B	1,7,9, 8A,8B	1,7,9, 8A,8B

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIC) shall be required where specified, and the delta values shall be computed with reference to the previous electrical parameters (see table IIC).
7/ Delta limits required for initial qualification and after any design or process changes.

TABLE IIB. Additional screening for device class V.

Test	MIL-STD-883, test method	Lot requirement
Particle impact noise detection	2020	100%
Internal visual	2010, condition A or approved alternate	100%
Nondestructive bond pull	2023 or approved alternate	100%
Reverse bias burn-in	1015	100%
Burn-in	1015, total of 240 hrs. at +125°C	100%
Radiographic	2012	100%

TABLE IIC. Delta limits at +25°C.

Test 1/	Device types
	All
I_{CC3} standby	±10% of specified value in table IA
I_{OHZ}, I_{OLZ}	±10% of specified value in table IA

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta Δ.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table IIC herein.

4.4.3.1 Additional criteria for device classes M, B, and S.

a. Steady-state life test conditions, method 1005 of MIL-STD-883:

(1) All devices requiring end-point electrical testing shall be programmed with a checkerboard pattern. After completion of all testing, the devices shall be erased and verified (except devices submitted for group D testing).

(2) Test condition D or E. For device class M the test circuit shall be submitted to DESC-ECS for review with the certificate of compliance. For device classes B and S the test circuit shall be submitted to the qualifying activity.

(3) T_A = +125°C, minimum.

(4) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

b. An endurance test, per method 1033 of MIL-STD-883, shall be added to group C1 inspection prior to performing the steady state life test (see paragraph 4.4.3.1a) and extended data retention (paragraph 4.4.3.1c). Cycling may be block, byte or page from devices passing Group A after the completion of the requirements of 4.2 herein. Initially two groups of devices shall be formed, cell 1 and cell 2. The following conditions shall be met:

(1) Cell 1 shall be cycled at -55°C and cell 2 shall be cycled at +125°C for a minimum of 10,000 cycles for device types.

(2) Perform group A subgroups 1,7 and 9 after cycling. Form new cells (cell 3 and cell 4) for steady state life and extended data retention. Cell 3 for steady state life test consists of 1/2 of the devices from cell 1 and 1/2 of the devices from cell 2. Cell 4 for extended data retention consists of the remaining devices from cell 1 and cell 2.

(3) The sample plans for cell 1, cell 2, cell 3 and cell 4 shall individually be the same as for group C, as specified in method 5005 of MIL-STD-883.

c. Extended data retention test shall consist of the following:

(1) All devices shall be programmed with a charge on all memory cells in each device, such that the cell will read opposite the state that the cell would read in its equilibrium state (e.g., worst case pattern).

(2) Unbiased bake for 1000 hours (minimum) at +150°C (minimum). The unbiased bake time may be accelerated by using higher temperature in accordance with the Arrhenius Relationship and with the apparent activation of 0.6eV. The maximum bake temperature shall not exceed +200°C for packaged devices or +300°C for unassembled devices.

(3) Read the pattern after bake and perform end-point electrical tests per table IIA herein for group C.

d. After the completion of all testing, the devices shall be erased and verified prior to delivery.

e. Cell 1, cell 2, cell 3, and cell 4 must individually pass the specified sample plan.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The steady-state life test circuit shall be submitted to DESC-ECS with the certificate of compliance and shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535. After the completion of all testing, the devices shall be erased and verified prior to delivery.

4.4.4 Group D inspection. For group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisiton document.

a. RHA tests for device classes B and S for levels M, D, R, and H or for device class M for levels M and D shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table IA herein. RHA samples need not be tested at -55°C or +125°C prior to total dose irradiation.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. The samples shall pass the specified group A electrical parameters for subgroups specified in table IIA herein.

d. The devices shall be subjected to radiation hardness assurance tests as specified in MIL-M-38510, (device classes M, B, and S) and MIL-I-38535, (device classes Q and V) for the RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = 25°C ±5°C, after exposure.

e. Prior to and during, total dose irradiation, the devices shall be biased to the worst case conditions established during characterization, (see figure 6) herein.

f. Single Event Phenomena (SEP) testing, shall be performed on all class S and V devices, and shall be optional on all classes M, B, and Q devices. SEP testing shall be performed at initial qualification and after any design or process changes which may affect the upset or latchup characteristics of the device. Test four devices with zero failures. ASTM standard F1192-88 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

(1) The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°).

(2) The fluence shall be ≥ 10^7 ions/cm^2.

(3) The flux shall be between 10^2 and 10^5 ion/cm^2/s. The cross section shall be verified to be flux independent by measuring the cross section at two flux rates which differ by at least an order of magnitude.

(4) The particle range shall be ≥ 20 microns in silicon.

(5) The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

(6) Bias conditions shall be V_{CC} = 4.5 V dc for the upset measurements and V_{CC} = 5.5 V dc for the latchup measurements.

(7) For SEP test limits see table IB herein.

g. For device classes M, B, and S subgroups 1 and 2 of table V method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

h. When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

(1) RHA delta limits.

(2) RHA upset levels.

(3) Test conditions (SEP).

(4) Number of upsets (SEP).

(5) Number of transients.

(6) Occurence of latchup.

4.5 Delta measurements for device classes B, S, Q, and V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIC.

4.6 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows:

4.6.1 Voltages and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

4.6.2 Life test, burn-in, cool down and electrical test procedure. When devices are measured at +25°C following application of the steady state life or burn-in test condition, all devices shall be cooled to +35°C or within 10°C of the power stable condition prior to removal of bias voltages/signals. Any electrical tests required shall first be performed at -55°C or +25°C prior to any required tests at +125°C.

4.6.3 Writing Procedure.

4.6.3.1 Read (READ). The Read (READ) instructions outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit output string. Output data changes are initiated by a low to high transition of the SK clock. In the NONVOLATILE SHIFT-REGISTER mode of operation, the memory automatically cycles to the next register after each 16 data bits are clocked out. The dummy-bit is supressed in this mode and a continuous string of data is obtained.

4.6.3.2 Write Enable (WNE). When VCC is applied to the part, it powers up in the Write Disable (WDS) state. Therefore, all programming modes must be preceded by a Write Enable (WEN) instruction. Once a Write Enable instruction is excecuted programming remains enabled until a Write Disable (WDS) instruction is excecuted or VCC is removed from the part.

4.6.3.3 Write (WRITE). The Write (WRITE) instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. The PE pin MUST be held "high" while loading the WRITE instruction, however, after loading the WRITE instruction the PE pin becomes a "don't care". The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (CS). DO = logical 0 indicates that programming is still in progress. DO = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

4.6.3.4 Write All (WRALL). The Write All (WRALL) instruction is valid only when the "protect register" has been cleared by exceuting a PRCLEAR instruction. The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. Like the WRITE instruction, the PE pin MUST be held "high" while loading the WRALL instruction, however, after loading the WRITE instruction the PE pin becomes a "don't care". As in the WRITE mode the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (tCS).

4.6.3.5 Write Disable (WDS). To protect against accidental data distrub, the Write Disable (WDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

4.6.3.6 Protect Register Read (PRREAD). The Protect Register Read (PRREAD) instruction outputs the address stored in the "protect register" on the DO pin. The PRE pin MUST be held "high" while loading the instruction. Following the PRREAD instruction the 8-bit address stored in the Protect Register is transferred to the serial out shift register. As in the READ mode, a dummy bit (logical 0) precedes the 8-bit address string.

4.6.3.7 Protect Register Enable (PREN). The Protect Register Enable (PREN) instruction is used to enable the PRCLEAR, PRWRITE, and PRDS modes. Before the PREN mode can be entered, the part must be in the Write Enable (WEN) mode. Both the PRE and PE pins MUST be held "high" while loading the instruction. Note that a PREN instruction must IMMEDIATELY precede a PRCLEAR, PRWRITE, or PRDS instruction.

4.6.3.8 Protect Register Clear (PRCLEAR). The Protect Register Clear (PRCLEAR) instruction clears the address stored in the Protect Register and, therefore, enables ALL registers for the WRITE and WRALL instruction. The PRE and PE pins MUST be held "high' while loading the instruction, however, after loading the PRCLEAR instruction the PRE and PE pins become "don't care". Note that a PREN instruction must IMMEDIATELY precede a PRCLEAR instruction.

4.6.3.9 Protect Register Write (PRWRITE). The Protect Register Write (PRWRITE) instruction is used to write into the Protect Register the address of the first register to be protected. After the PRWRITE instruction is executed, all memory registers whose addresses are greater than or equal to the address specified in the Protect Register are protected from the WRITE operation. Note that before executing a PRWRITE instruction the Protect Register must first be cleared by executing a PRCLEAR operation and that the PRE and PE pins MUST be held "high" while loading the instruction, however, after loading the PRWRITE instruction, the PRE and PE pins become "don't care". Note that a PREN instruction must IMMEDIATELY precede a PRWRITE instruction.

4.6.3.10 Protect Register Disable (PRDS). The Protect Register Disable (PRDS) instruction is a ONE TIME ONLY instruction which renders the Protect Register unalterable in the future. Therefore, the specified registers become PERMANENTLY protected against data changes. As in the PRWRITE instruction the PRE and PE pins MUST be held "high" while loading the instruction, and after loading the PRDS instruction the PRE and PE pins become "don't care". Note that a PREN instruction must IMMEDIATELY precede a PRDS instruction.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandantory.)

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

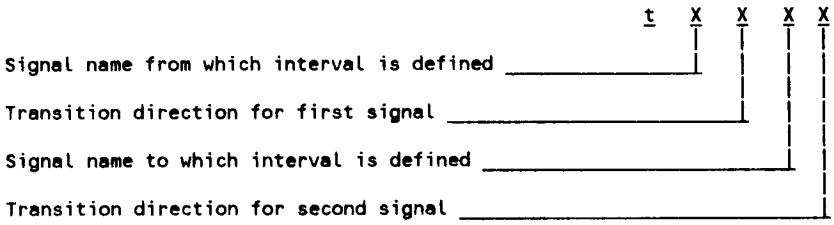
6.4 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

C_{IN} C_{OUT}	Input and bidirectional output, terminal-to-GND capacitance.
GND	Ground zero voltage potential.
I_{CC}	Supply current.
I_{IL}	Input current low
I_{IH}	Input current high
T_C	Case temperature.
T_A	Ambient temperature
V_{CC}	Positive supply voltage.
V_H	Output enable and Write enable voltage during chip erase
O/V	Latch-up over-voltage

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.2 Timing parameter abbreviations. All timing abbreviations use lower case characters with upper case character subscripts. The initial character is always "t" and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal specify the signal name and the signal transition. Thus the format is:



a. Signal definitions:

A = Address
D = Data in
Q = Data out
W = Write enable
E = Chip enable
O = Output enable

b. Transition definitions:

H = Transition to high
L = Transition to low
V = Transition to valid
X = Transition to invalid or don't care
Z = Transition to off (high impedance)

6.5.3 Waveforms.

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-ECS and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS.