

1.1 Scope.

This specification covers the detail requirements for two monolithic CMOS analog switches, each consisting of four independent single-pole single-throw switches and latched digital inputs with a WR signal for microprocessor interfacing. They differ only in that the digital control logic is inverted.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
-1	ADG221T(X)/883B
-2	ADG222T(X)/883B

NOTE

¹To complete the part number substitute the package identifier as shown in paragraph 1.2.3.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-16	16-Pin Cerdip
E	E-20A	20-Terminal LCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$)

V+ to V-	44V
V+ to GND	25V
V- to GND	-25V
Analog Inputs	
Voltage at S, D	V- to V+
Continuous Current, S or D	30mA
Pulsed Current S or D	
1ms Duration, 10% Duty Cycle	70mA
Digital Inputs	
Voltages at IN, WR	V- -2V to V+ +2V or 20mA, Whichever Occurs First
Power Dissipation (Package)	
Up to +75°C	900mW/°C
Derates above +75°C by	12mW/°C
Operating Temperature	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C
Junction Temperature (T_J)	+175°C

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C/W}$ for Q-16 and E-20A
 $\theta_{JA} = 120^\circ\text{C/W}$ for Q-16 and E-20A

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Table 1.

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Test Condition ¹ /Comments	Units
Switch "ON" Resistance	R_{DS}	- 1, 2	145	90	145	$V_{IN} = 0.8V$ for - 1 Device and 2.4V for - 2 Device; $V_D \pm 10V$, $I_S = \mp 1.0mA$ (See Figure 1)	Ω max
		- 1, 2	200	200	200	$V = +10V$, $V = -10V$; $V_D = \pm 7.5V$; $V_{IN} = 0.8V$ for - 1 Device and 2.4V for - 2 Device; $I_S = +10.0mA$ (See Figure 1)	Ω max
Source "OFF" Leakage Current	$I_S(OFF)$	- 1, 2	100	1	100	$V_D = \pm 14V$, $V_S = \mp 14V$; $V_{IN} = 2.4V$ for - 1 Device and 0.8V for - 2 Device, (See Figure 2)	$\pm nA$ max
Drain "OFF" Leakage Current	$I_D(OFF)$	- 1, 2	100	1	100	$V_D = \pm 14V$, $V_S = \mp 14V$; $V_{IN} = 2.4V$ for - 1 Device and 0.8V for - 2 Device, (See Figure 3)	$\pm nA$ max
Channel "ON" Leakage Current	$I_D(ON)$	- 1, 2	200	1	200	$V_D = \pm 14V$, All Other Digital Inputs = 0.8V for - 1 Device and 2.4V for - 2 Device (See Figure 4)	$\pm nA$ max
Digital Input High Voltage	V_{INH}	- 1, 2	2.4	2.4	2.4		V min
Digital Input Low Voltage	V_{INL}	- 1, 2	0.8	0.8	0.8		V max
High Level Input Current	I_{INH}	- 1, 2	1.0	0.5	1.0	$V_{IN} = 15V$; All Other Digital Inputs = 0.8V (See Figure 5)	$\pm \mu A$ max
Low Level Input Current	I_{INL}	- 1, 2	1.0	0.5	1.0	$V_{IN} = 0.8V$; All Other Digital Inputs = 2.4V (See Figure 5)	$\pm \mu A$ max
Supply Current	$+I_{CC}$	- 1, 2	2.0	1.5	2.0	$V_{IN} = 0V$ or 5V For All Digital Inputs $S1 \dots S4 = D1 \dots D4 =$ Open Circuit (See Figure 6)	mA max
	$-I_{CC}$	- 1, 2	2.0	1.5	2.0	$V_{IN} = 0V$ or 5.0V For All Digital Inputs $S1 \dots S4 = D1 \dots D4 =$ Open Circuit (See Figure 6)	mA max
Subgroup 9: $T_A = +25^\circ C$ Write Pulse Width Digital Input Setup Time Digital Input Hold Time Turn "ON" Time Turn "OFF" Time	t_{WR} t_{DS} t_{HS} $t_{(ON)}$ $t_{(OFF)}$	- 1, 2 - 1, 2 - 1, 2 - 1, 2 - 1, 2	100 100 20 600 500			(See Paragraph 5.0) (See Paragraph 5.0) (See Paragraph 5.0) $C_L = 100pF$, $R_L = 1k$ (See Figure 7) $C_L = 100pF$, $R_L = 1k$ (See Figure 7)	ns min ns min ns min ns max ns max
Subgroup 10: $T_A = +125^\circ C$ Write Pulse Width Digital Input Setup Time Digital Input Hold Time Turn "ON" Time Turn "OFF" Time	t_{WR} t_{DS} t_{HS} $t_{(ON)}$ $t_{(OFF)}$	- 1, 2 - 1, 2 - 1, 2 - 1, 2 - 1, 2	120 120 20 800 650			(See Paragraph 5.0) (See Paragraph 5.0) (See Paragraph 5.0) $C_L = 100pF$, $R_L = 1k$ (See Figure 7) $C_L = 100pF$, $R_L = 1k$ (See Figure 7)	ns min ns min ns min ns max ns max
Subgroup 11: $T_A = -55^\circ C$ Write Pulse Width Digital Input Setup Time Digital Input Hold Time Turn "ON" Time Turn "OFF" Time	t_{WR} t_{DS} t_{HS} $t_{(ON)}$ $t_{(OFF)}$	- 1, 2 - 1, 2 - 1, 2 - 1, 2 - 1, 2	120 120 20 600 500			(See Paragraph 5.0) (See Paragraph 5.0) (See Paragraph 5.0) $C_L = 100pF$, $R_L = 1k$ (See Figure 7) $C_L = 100pF$, $R_L = 1k$ (See Figure 7)	ns min ns min ns min ns max ns max
Subgroup 12: $T_A = +25^\circ C$ Off Isolation	V_{ISO}	- 1, 2	60			$f = 200kHz$ $V_{GEN} = 1V_{P-P}$; $R_L = 1k$ (See Figure 8)	dB min
Subgroup 13: $T_A = +25^\circ C$ Crosstalk between Channels	V_{CT}	- 1, 2	60			$f = 200kHz$ $V_{GEN} = 1V_{P-P}$; $R_L = 1k$ (See Figure 9)	dB min
Subgroup 14: $T_A = +25^\circ C$ Charge Transfer Error	V_{CTE}	- 1, 2	10			(See Figure 10)	$\pm mV$ max
Capacitance: Address	C_A	- 1, 2	15			$T_A = +25^\circ C$; $GND = 0V$; $f = 1MHz$; $V_{IN} = 0V$	pF max
Capacitance: Input Switch	C_{IS}	- 1, 2	15			$T_A = +25^\circ C$; $GND = 0V$; $f = 1MHz$; $V_{IN} = 5V$	pF max
Capacitance: Output Switch	C_{DS}	- 1, 2	20			$T_A = +25^\circ C$; $GND = 0V$; $f = 1MHz$; $V_{IN} = 5V$	pF max

NOTE

¹Unless otherwise noted $V = +15V$; $V = -15V$.

Table 2. Electrical Test Requirements

MIL-STD-883 Test Requirements	Subgroups (See Table 1)
Interim Electrical Parameters (Pre-Burn-In) Method 5004	1
Final Electrical Parameters, Method 5004	1*, 2, 3, 9
Group A Electrical Parameters, Method 5005	1, 2, 3, 9, 10, 11
Group C End Point Electrical Parameters, Method 5005	1, 10, 11 and Table 3 Delta Limits

*Indicates P.D.A. applies to Subgroup 1.

Table 3.

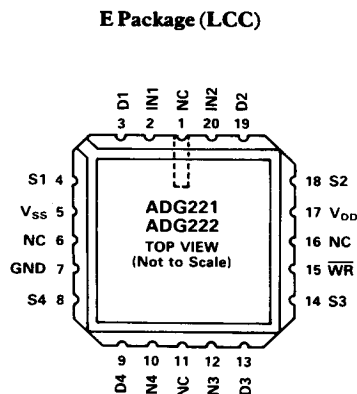
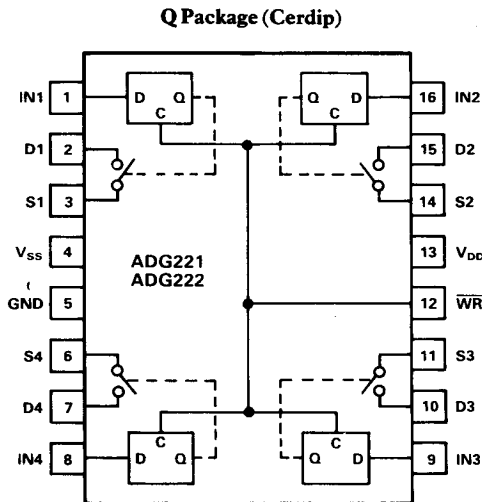
Parameters ²	Delta Limits at +25°C ¹ Device Types	
	1	2
R _{DS}	15Ω	15Ω
I _D (ON)	1nA	1nA

NOTES

¹Each test applies to every switch in the package.

²Each of the above parameters shall be recorded before and after the required burn-in and life-tests to determine deltas (Δ).

3.2.1 Functional Block Diagram and Terminal Assignments.



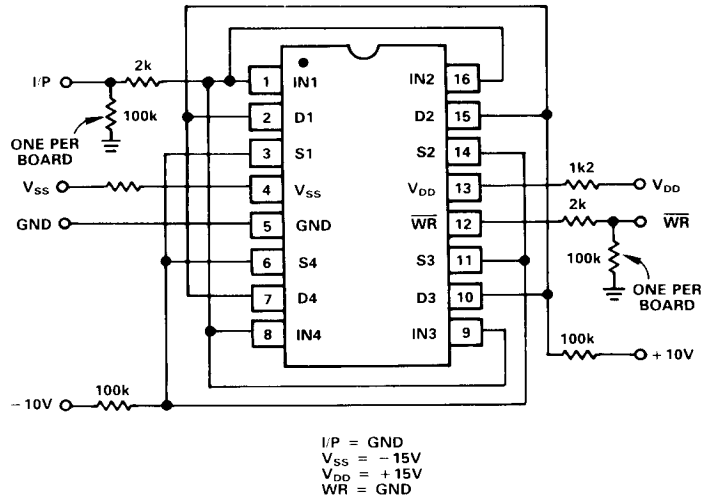
3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (82).

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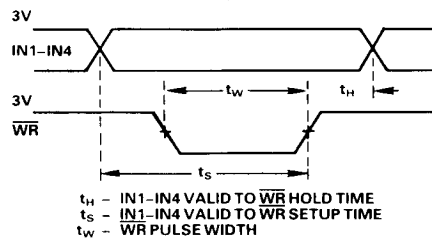
4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



5.0 Timing and Control Sequence

The diagram below shows the timing sequence for latching the switch digital inputs (IN1-IN4). The latches are level sensitive and, therefore, while $\overline{WR}$ is held low the latches are transparent and the switches respond to the digital inputs. The digital inputs are latched on the rising edge of $\overline{WR}$.



Timing and Control Sequence

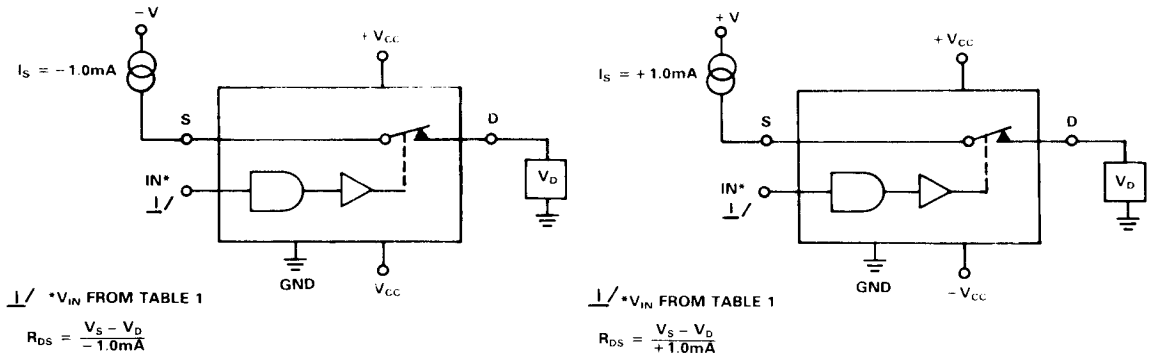


Figure 1. R_{DS} Test Circuits

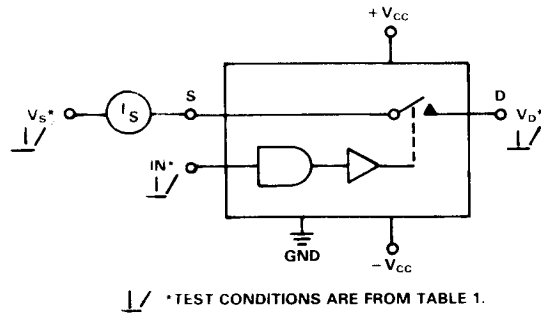


Figure 2. I_S (OFF) Test Circuit

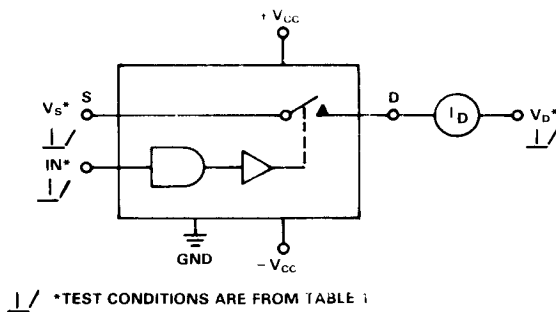


Figure 3. I_D (OFF) Test Circuit

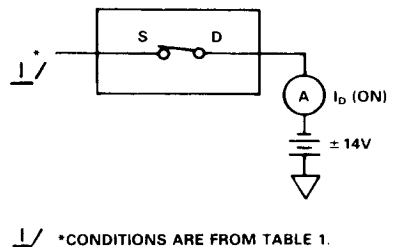
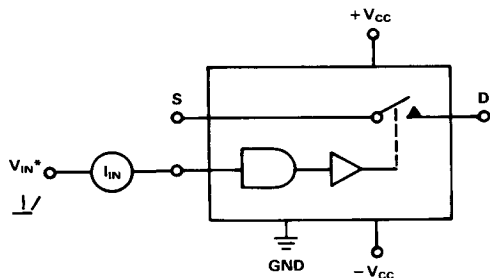


Figure 4. I_D (ON) Test Circuit



1/ *CONDITIONS ARE FROM TABLE 1.

Figure 5. I_{INL} , I_{INH} Test Circuit

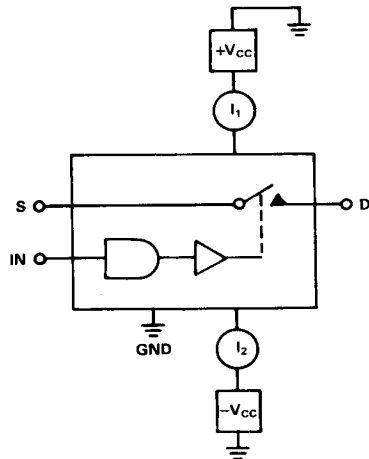


Figure 6. $\pm I_{CC}$ Test Circuit

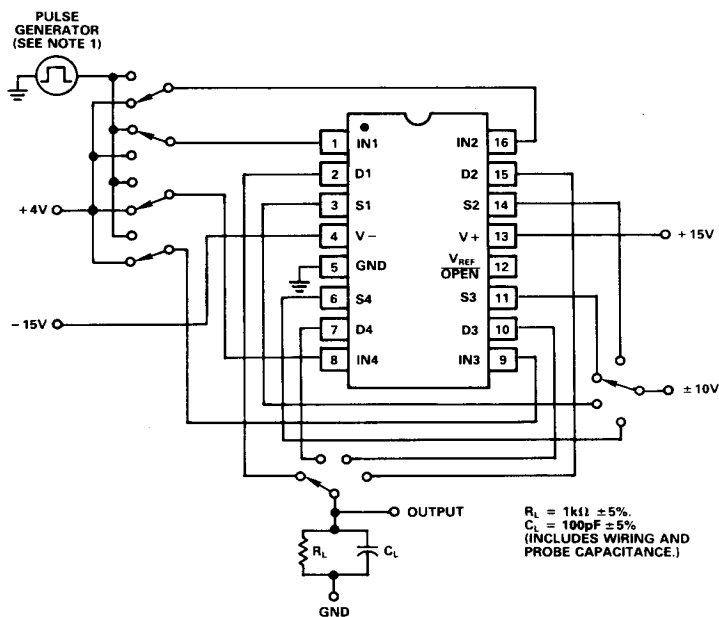
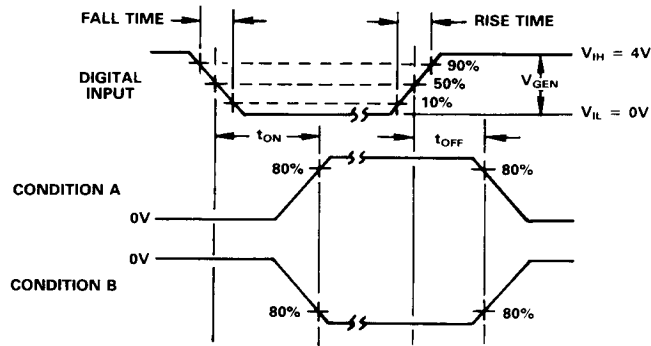
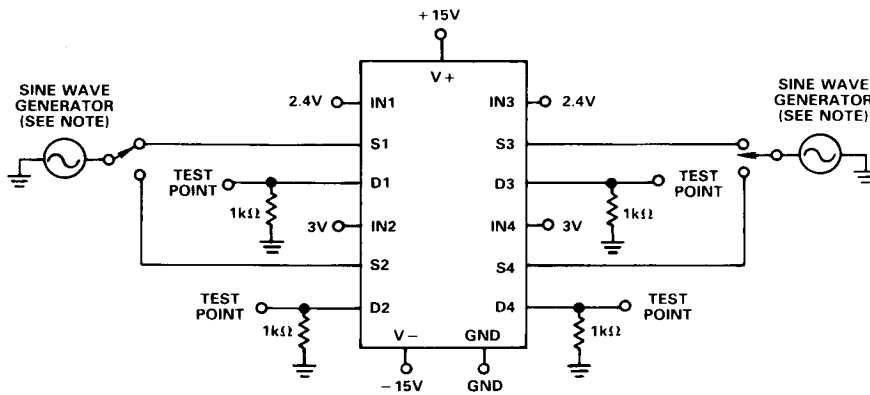


Figure 7a. Switching Time Circuits



NOTE
RISE TIME AND FALL TIME $\leq 20\text{ns}$.

Figure 7b. Switching Time Waveforms



NOTE
THE SINE WAVE GENERATOR HAS THE FOLLOWING CHARACTERISTICS:
 $V_{\text{GEN}} = 1\text{V p-p}$, FREQUENCY = 200kHz

Figure 8. Off Isolation Test Circuits

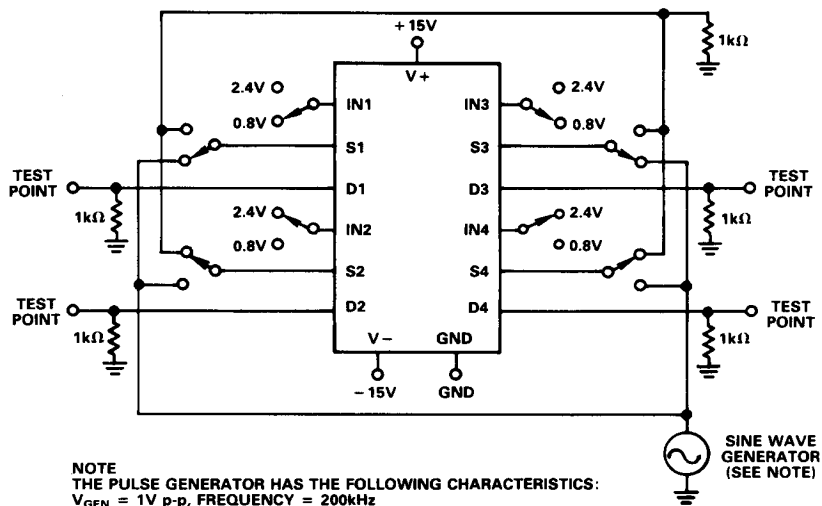


Figure 9. Crosstalk Test Circuit

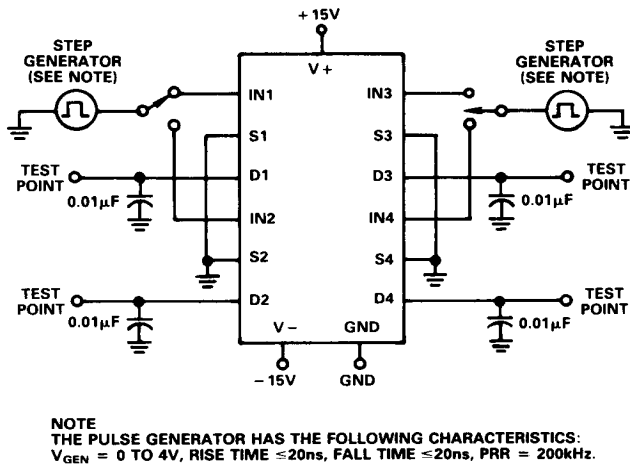


Figure 10. Charge Transfer Error Test Circuits