Data Sheet
May 1996

microelectronics group

Lucent Technologies
Bell Labs Innovations

ALA401/402 Semicustom Linear Array

Features

- High-speed CBIC process: 250 MHz NPN and PNP
- High breakdown (BV_{CEO} 33 V)
- Optional on-chip ESD protection
- Two-level metal
- Electrically trimmable resistor meltback links
- Quick design turnaround (typically 4 to 5 weeks)
- Proven reliability

Applications

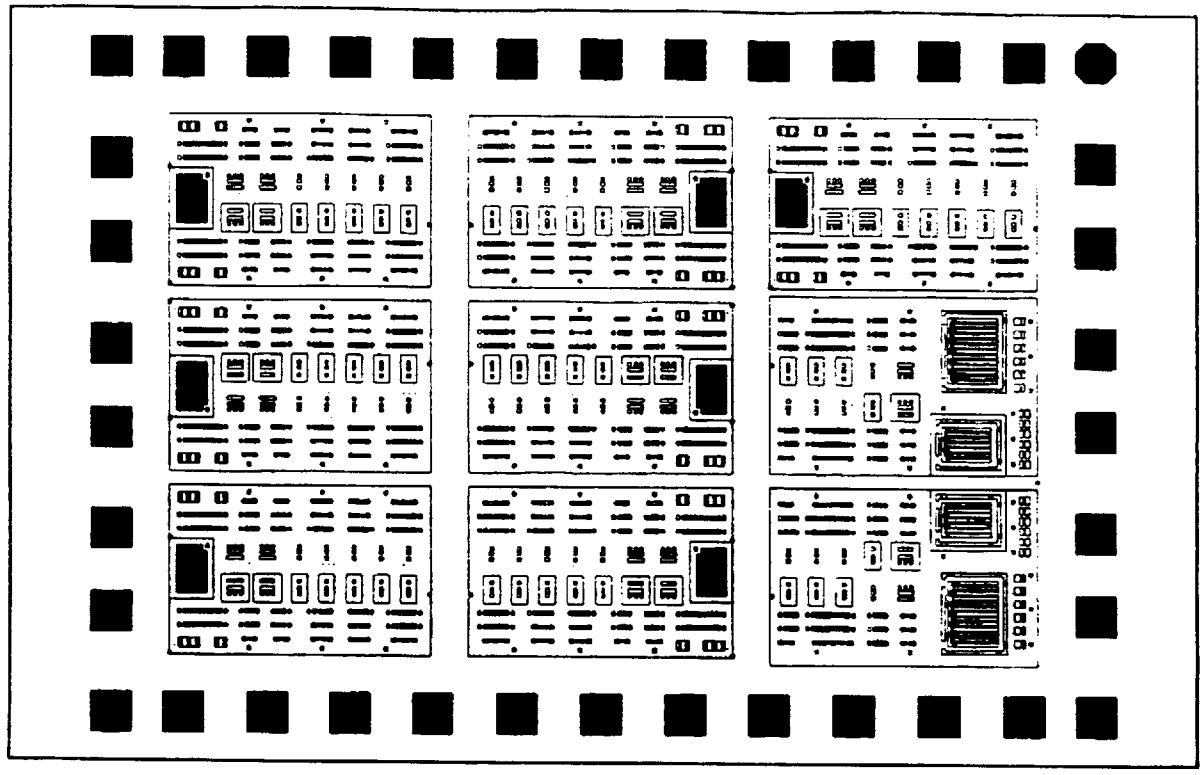
- Integration of general-purpose discrete circuitry (PC board and hybrid cost reduction)
  - — Analog glue circuitry
- Instrumentation
  - — Preamplifier (30 MHz)
  - — Precision amplifiers:
    Low noise (1.8 nVrms/$\sqrt{Hz}$)
    Low distortion (–40 dB)
- Pin electronics
  - — Slew rate (400 V/µs)
- Special circuitry
  - — Low power supply (1.5 V amplifiers)
  - — Precision references
- Telephony
  - — Signal conditioning
  - — Signal monitoring
  - — Regeneration (T1 rates)

Description

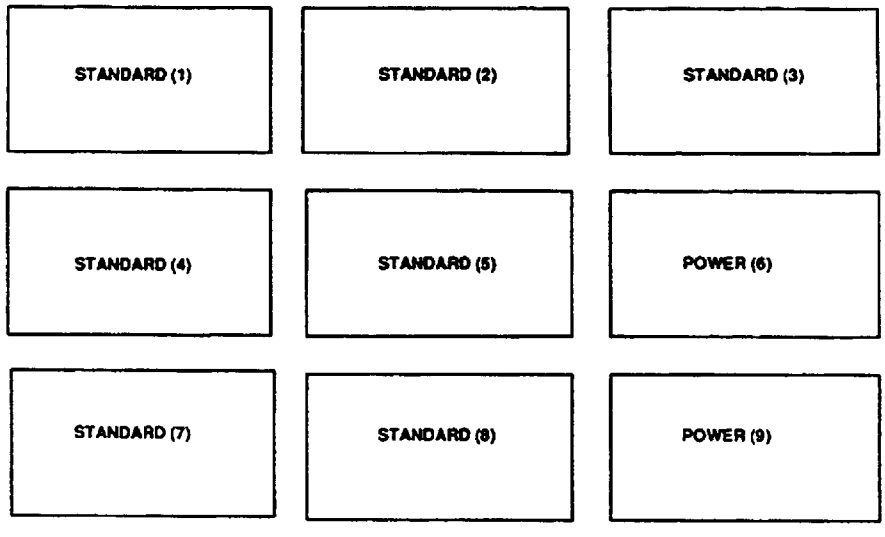
The ALA401/402 Semicustom Linear Arrays are integrated circuits consisting of vertical NPN and PNP transistors, programmable capacitors, and implanted boron resistors. Designed on a regular grid system, the arrays provide easy interconnections for the designer. These arrays are fabricated in a complementary bipolar integrated circuit (CBIC-R) process that offers the advantage of similar NPN and PNP transistor characteristics at high speeds. Typical Peak f_T values of 250 MHz for the NPN and PNP (V_{CE} = 10 V and I_E = 1 mA and 0.5 mA) and high-current drive capability (5 mA for both 1X transistors) are unique to these arrays.

The ALA401 array is comprised of nine tiles, consisting of seven standard tiles and two power tiles. The ALA402 array is comprised of 16 tiles, consisting of ten standard tiles, four power tiles, and two JFET tiles. Each JFET tile contains two JFETS with pinch-off voltage specifications of 1.0 V to 2.5 V at I_{DS} = 100 nA and V_{DS} = 5 V. Because the tiles are on a regular grid system, the user interconnects components by drawing lines on a clearly defined grid marked layout sheet.

Two levels of metallization are available on these arrays. The designer has the ability to completely customize the bottom-metal, via holes, and top-metal levels. The bottom metal has a sheet resistance of approximately 0.85 Ω/sq. with a current capacity of 0.2 mA/µm of metal width. The top metal has a sheet resistance of approximately 0.04 Ω/sq. with a current capacity of 2.0 mA/µm of metal width. The standard 8 µm bottom-metal linewidths are capable of carrying a maximum of 1.6 mA dc current, and the standard 8 µm top-metal linewidths are capable of carrying a maximum of 16 mA dc current. For applications where higher interconnect resistance is required, the standard metal linewidths can be increased.

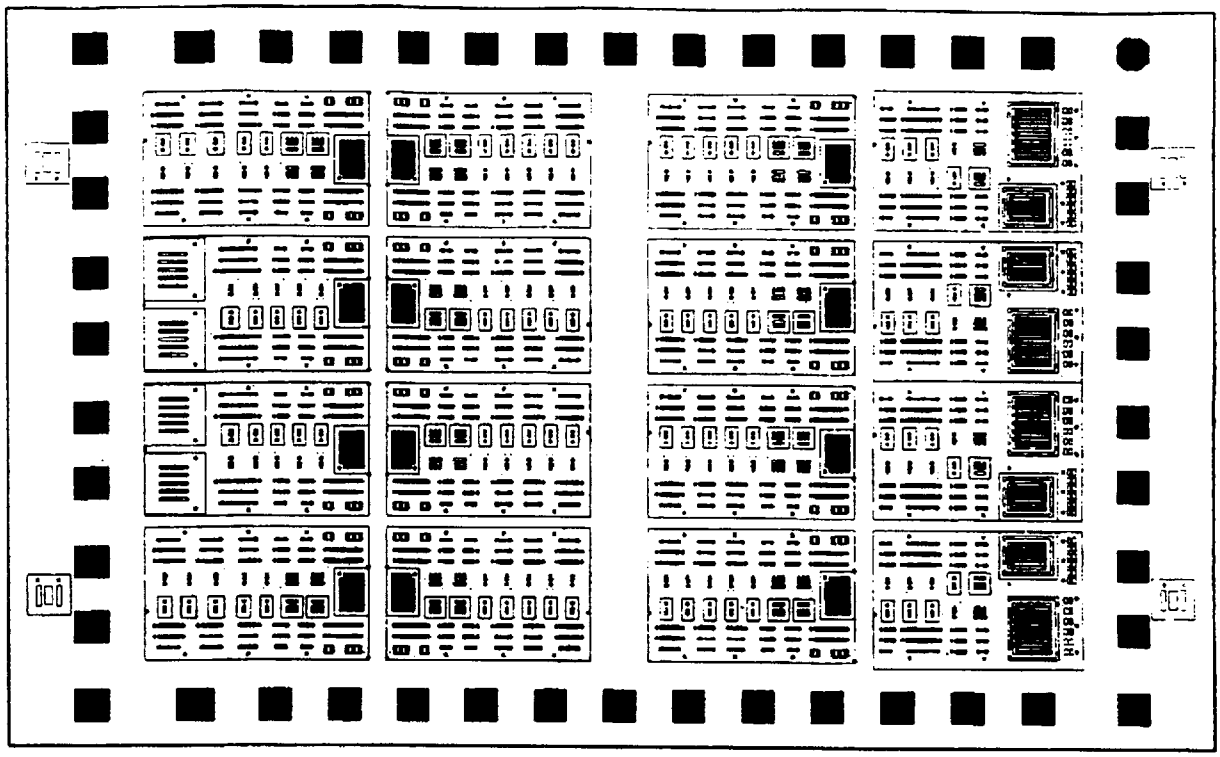


(a) Module Layout
4100 μm x 2600 μm

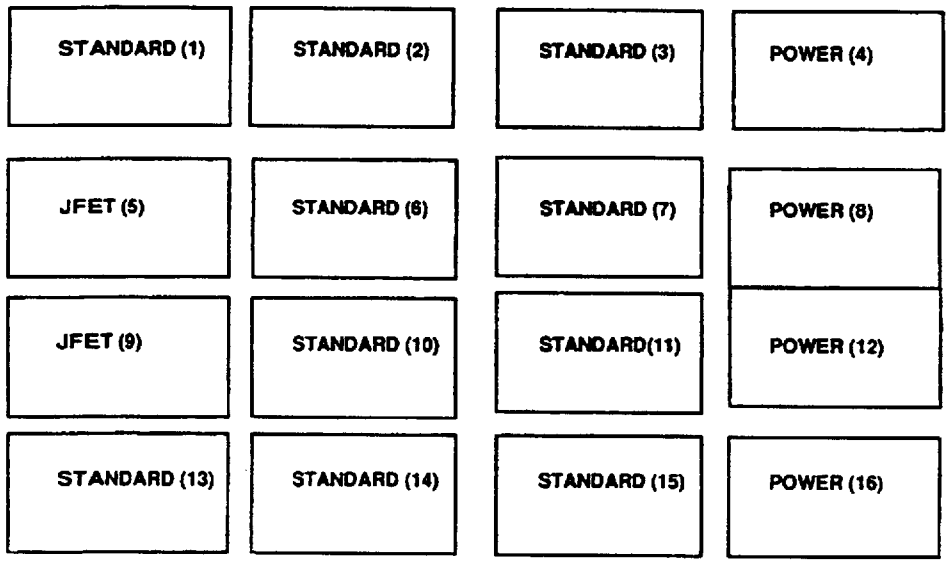


(b) Location of Tiles on Die

Figure 1. ALA401 Linear Array Die Schematic



(a) Module Layout
5220 μm x 3260 μm



(b) Location of Tiles on Die

Figure 2. ALA402 Linear Array Die Schematic

Electrical Characteristics (T_A = 25°C)

Table 1. NPN Parameters NR111A21 (1X)

Symbol	Measurement/Condition	Min	Typ	Max	Unit
h_{FE}*	I_E = −100 µA, V_{CB} = 2 V	40	105	—	—
f_T	I_E = −1 mA, V_{CE} = 10 V	200	250	—	MHz
V_A	I_B = 10 µA, V_{CE} = 2 V, 12 V	100	220	—	V
V_{CE} (sat)	I_C = 750 µA, I_B = 50 µA	—	190	220	mV
V_{BE}†	I_E = −100 µA, V_{CB} = 2 V	687	707	727	mV
BV_{CEO}	I_C = 100 µA	33	38	—	V
BV_{CBO}	I_C = 100 µA	33	50	—	V
BV_{CIO}	I_C = 100 µA	33	51	—	V
BV_{EBO}	I_E = 100 µA	7.7	8.2	—	V

* h_{FE} matching of adjacent transistors of the same type is within ±2%.
† V_{BE} matching of adjacent transistors of the same type is within ±2.5 mV.

Table 2. PNP Parameters PR111A21 (1X)

Symbol	Measurement/Condition	Min	Typ	Max	Unit
h_{FE}*	I_E = 100 µA, V_{CB} = −2 V	40	125	—	—
f_T	I_E = 500 µA, V_{CE} = −10 V	180	250	—	MHz
V_A	I_B = −10 µA, V_{CE} = −2 V, −12 V	35	50	—	V
V_{CE} (sat)	I_C = −750 µA, I_B = −50 µA	—	−250	−285	mV
V_{BE}†	I_E = 100 µA, V_{CB} = −2 V	−677	−702	−727	mV
BV_{CEO}	I_C = −100 µA	−33	−47	—	V
BV_{CBO}	I_C = −100 µA	−33	−48	—	V
BV_{CIO}	I_C = −100 µA	−33	−47	—	V
BV_{EBO}	I_E = −100 µA	−7.7	−8.2	—	V

* h_{FE} matching of adjacent transistors of the same type is within ±5%.
† V_{BE} matching of adjacent transistors of the same type is within ±2.5 mV.

Table 3. Metallization Data

				Resistance	
Metal	Min Width	Thickness	Max Current Density	Typ	Max
Bottom Metal	8 µm	0.3 µm	0.2 mA/µm of width	0.85 Ω/sq.	1.2 Ω/sq.
Top Metal	8 µm	1.8 µm	2 mA/µm of width	0.04 Ω/sq.	0.055 Ω/sq.
Via	—	—	6 mA each	0.0015 Ω	—
Ti-Pt Link	6 µm	0.3 µm	0.2 mA/µm of width	2.8 Ω	4.8 Ω

Transistor Data ALA401 (T_A = 25°C)

Transistor Name*	Type	Qty	Scale	Current Range (mA)				
				80% Beta		80% fT		dc
				Min	Max	Min	Max	Max
NR111A21	NPN	43	1X	0.004	1.6	0.09	3.2	5.0
NR131A21	NPN	16	3X	0.011	4.9	0.27	9.6	15.0
NR38XS	NPN	2	38X	0.011	80.2	7.01	126.4	100.0
PR111A21	PNP	43	1X	0.003	0.6	0.05	1.5	5.0
PR131A21	PNP	16	3X	0.009	1.7	0.15	4.5	15.0
PR90XS	PNP	2	90X	0.03	35.5	4.59	130.0	100.0

* An explanation of the transistor name coding scheme is given on the last page of the data sheet.

Resistor Data ALA401 (T_A = 25°C)

Value (Ω)	Type*	Sheet Res. (Ω/sq.)	Width (μm)	Tol (%)	TCR (ppm/°C)	Qty
8	RRN	7	19	±30	+1771	24
100	RRL	200	32	±20	+1906	42
500	RRL	200	8	±20	+1906	72
1000	RRL	200	8	±20	+1906	64
5000	RRH	2000	8	±20	+3000	132
10000	RRH	2000	8	±20	+3000	100

* Denotes an implanted resistor. Matching of adjacent resistors of the same sheet resistance is within ±1%.

Capacitor Data ALA401 (T_A = 25°C)

	Type	Value (pF)	Tol (%)	Qty
Programmable	CRR	0.75 to 7.00	±25	7

Transistor Data ALA402 (T_A = 25°C)

Transistor Name*	Type	Qty	Scale	Current Range (mA)				
				80% Beta		80% fT		dc
				Min	Max	Min	Max	Max
NR111A21	NPN	76	1X	0.004	1.6	0.08	3.2	5.0
NR131A21	NPN	24	3X	0.011	4.9	0.27	9.6	15.0
NR38XS	NPN	4	38X	0.011	80.2	7.01	126.4	100.0
PR111A21	PNP	76	1X	0.003	0.6	0.05	1.5	5.0
PR131A21	PNP	24	3X	0.009	1.7	0.15	4.5	15.0
PR90XS	PNP	4	90X	0.03	35.5	4.59	130.0	100.0

* An explanation of the transistor name coding scheme is given on the last page of the data sheet.

Resistor Data ALA402 (T_A = 25°C)

Value (Ω)	Type*	Sheet Res. (Ω/sq.)	Width (µm)	Tol (%)	TCR (ppm/°C)	Qty
8	RRN	7	19	±30	+1771	48
100	RRL	200	32	±20	+1906	72
500	RRL	200	8	±20	+1906	120
1000	RRL	200	8	±20	+1906	112
5000	RRH	2000	8	±20	+3000	216
10000	RRH	2000	8	±20	+3000	176

* Denotes an implanted resistor. Matching of adjacent resistors of the same sheet resistance is within ±1%.

Capacitor Data ALA402 (T_A = 25°C)

	Type	Value (pF)	Tol (%)	Qty
Programmable	CRR	0.75 to 7.00	±25	12

JFET

Name	Measurement	Condition	Min	Typ	Max	Unit
JRS4130A	V_P	I_{DS} = 100 nA, V_{DS} = 5 V	1.0	1.5	2.5	V

Component Totals ALA401

Component	Type	Scale	Qty	Standard Tile	Power Tile
Transistor					
NR111A21	NPN	1X	43	5	4
NR131A21	NPN	3X	16	2	1
NR38XS	NPN	38X	2	—	1
PR111A21	PNP	1X	43	5	4
PR131A21	PNP	3X	16	2	1
PR90XS	PNP	90X	2	—	1
Resistors*	**Value**				
	8 Ω	—	24	—	12
Resistors†	**Value**				
	100 Ω	—	42	6	—
	500 Ω	—	72	8	8
	1000 Ω	—	64	8	4
Resistors‡	**Value**				
	5000 Ω	—	132	16	10
	10000 Ω	—	100	12	8
Capacitors	**Value**				
	0.75 to 7.00 pF	—	7	1	1
Bonding Pads	—	—	38	—	—

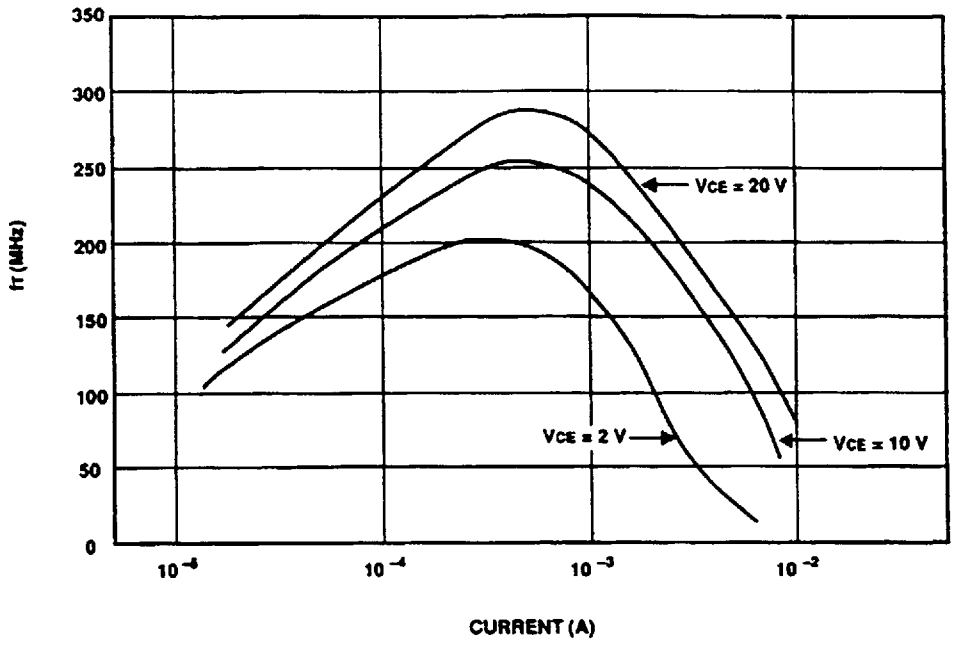
* Denotes a 7 Ω/sq. implanted phosphorus resistor.
† Denotes a 200 Ω/sq. implanted boron resistor.
‡ Denotes a 2000 Ω/sq. implanted boron resistor.

Component Totals ALA402

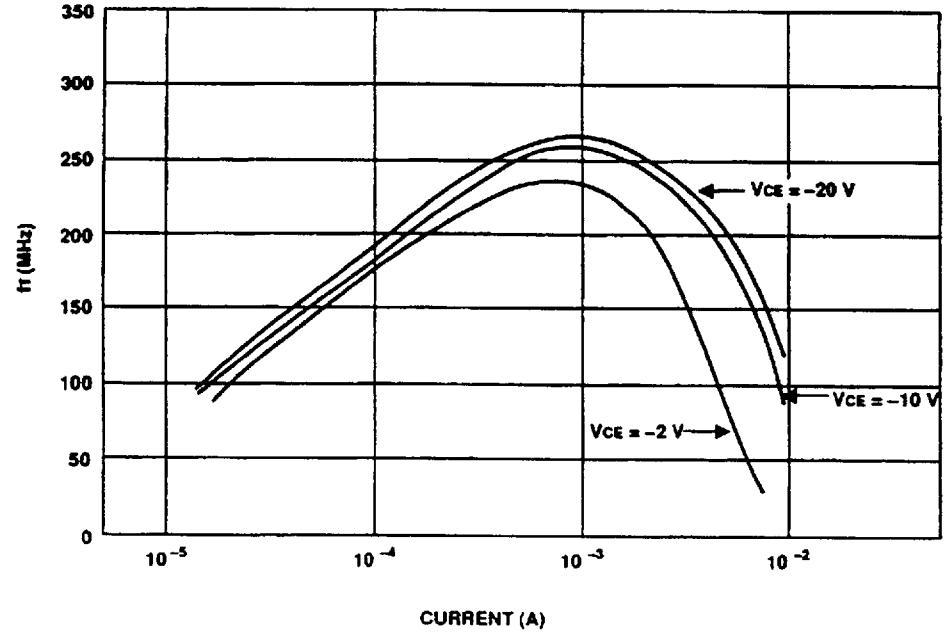
Component	Type	Scale	Qty	Standard Tile	Power Tile	JFET Tile
Transistor						
NR111A21	NPN	1X	76	5	4	5
NR131A21	NPN	3X	24	2	1	—
NR38XS	NPN	38X	4	—	1	—
PR111A21	PNP	1X	76	5	4	5
PR131A21	PNP	3X	24	2	1	—
PR90XS	PNP	90X	4	—	1	—
Resistors*	**Value**					
	8 Ω	—	48	—	12	—
Resistors†	**Value**					
	100 Ω	—	72	6	—	6
	500 Ω	—	120	8	8	8
	1000 Ω	—	112	8	4	8
Resistors‡	**Value**					
	5000 Ω	—	216	16	10	8
	10000 Ω	—	176	12	8	12
Capacitors	**Value**					
	0.75 to 7.00 pF	—	12	1	—	1
JFETs	—	—	4	—	—	2
Bonding Pads	—	—	46	—	—	—

* Denotes a 7 Ω/sq. implanted phosphorus resistor.
† Denotes a 200 Ω/sq. implanted boron resistor.
‡ Denotes a 2000 Ω/sq. implanted boron resistor.

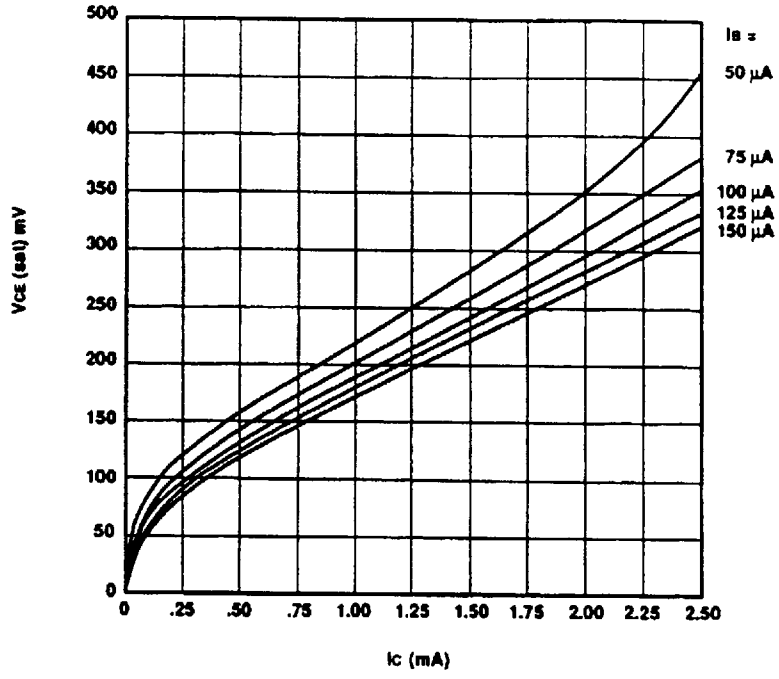
Unity-Gain Frequency Response (NR111A21)



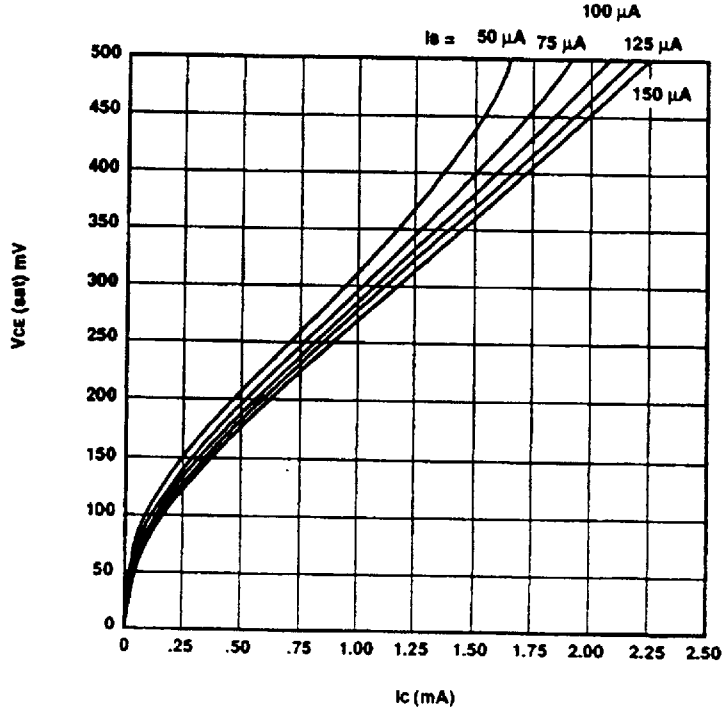
Unity-Gain Frequency Response (PR111A21)



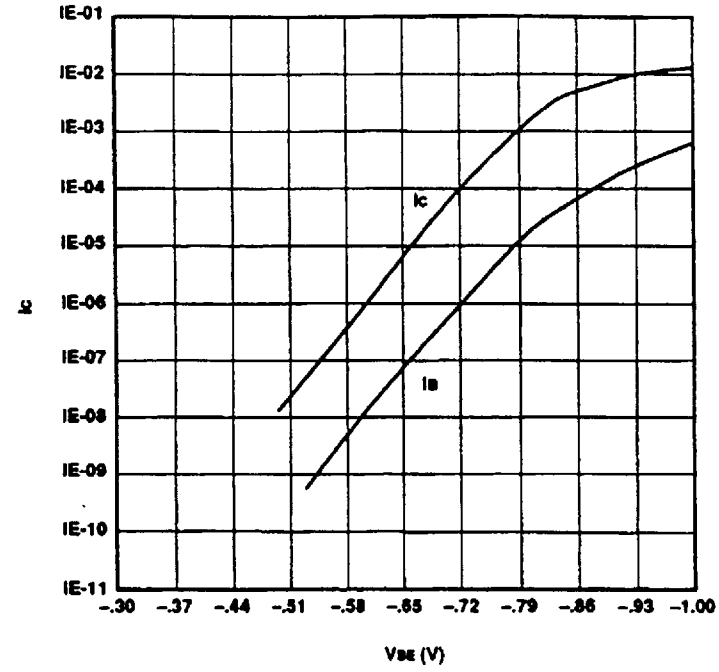
Current vs. Saturation Voltage (NR111A21)



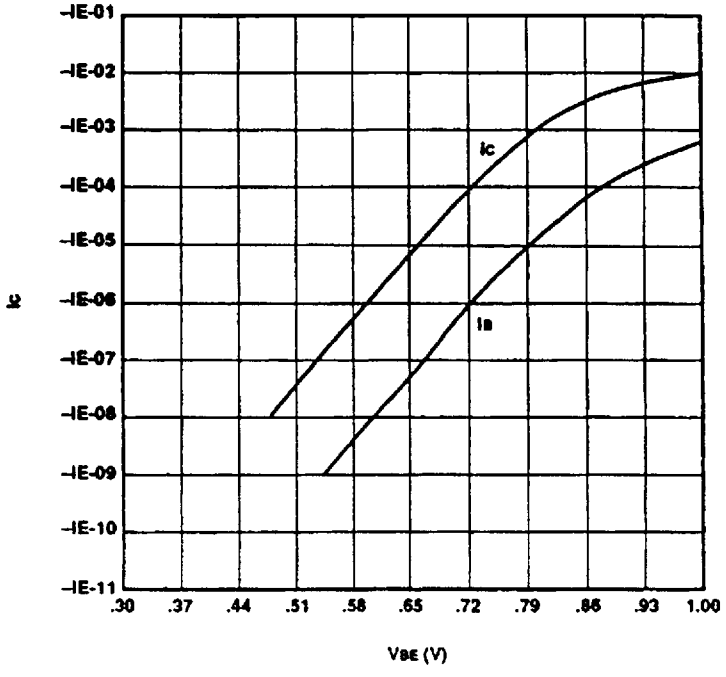
Current vs. Saturation Voltage (PR111A21)



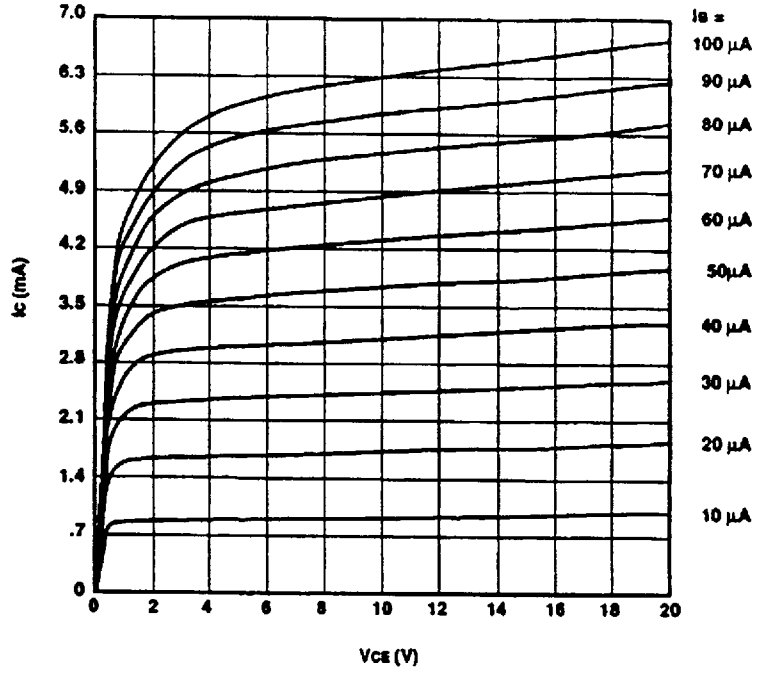
Current vs. Voltage Characteristics (NR111A21)



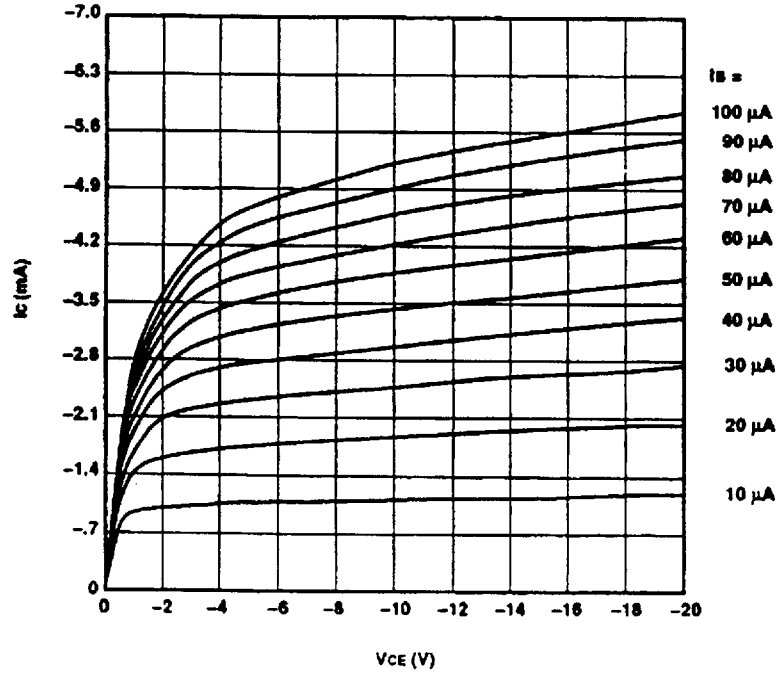
Current vs. Voltage Characteristics (PR111A21)



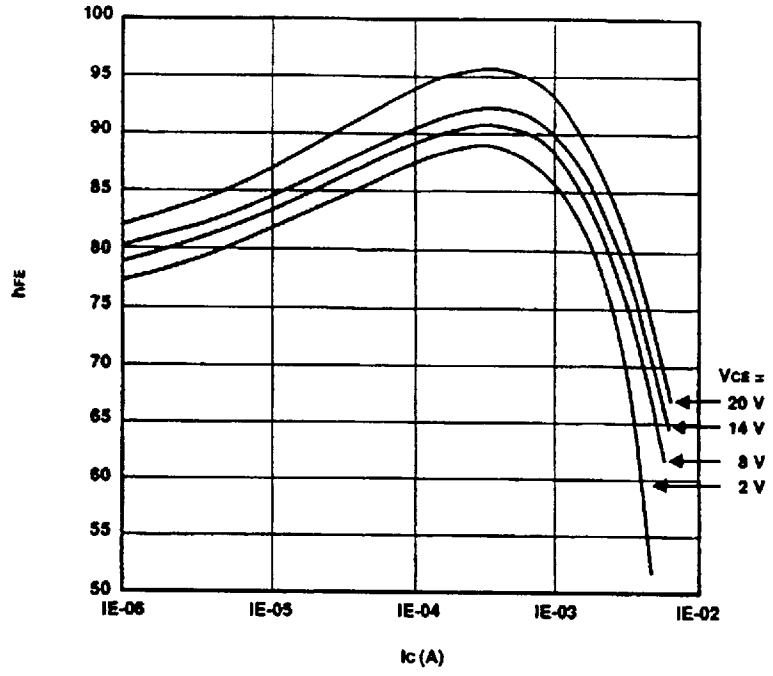
Output Voltage Characteristics (NR111A21)



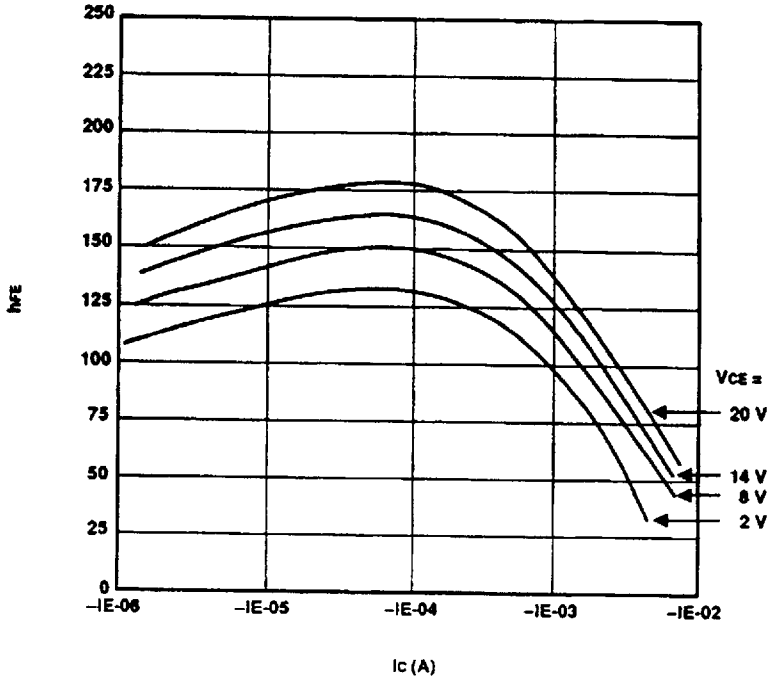
Output Voltage Characteristics (PR111A21)



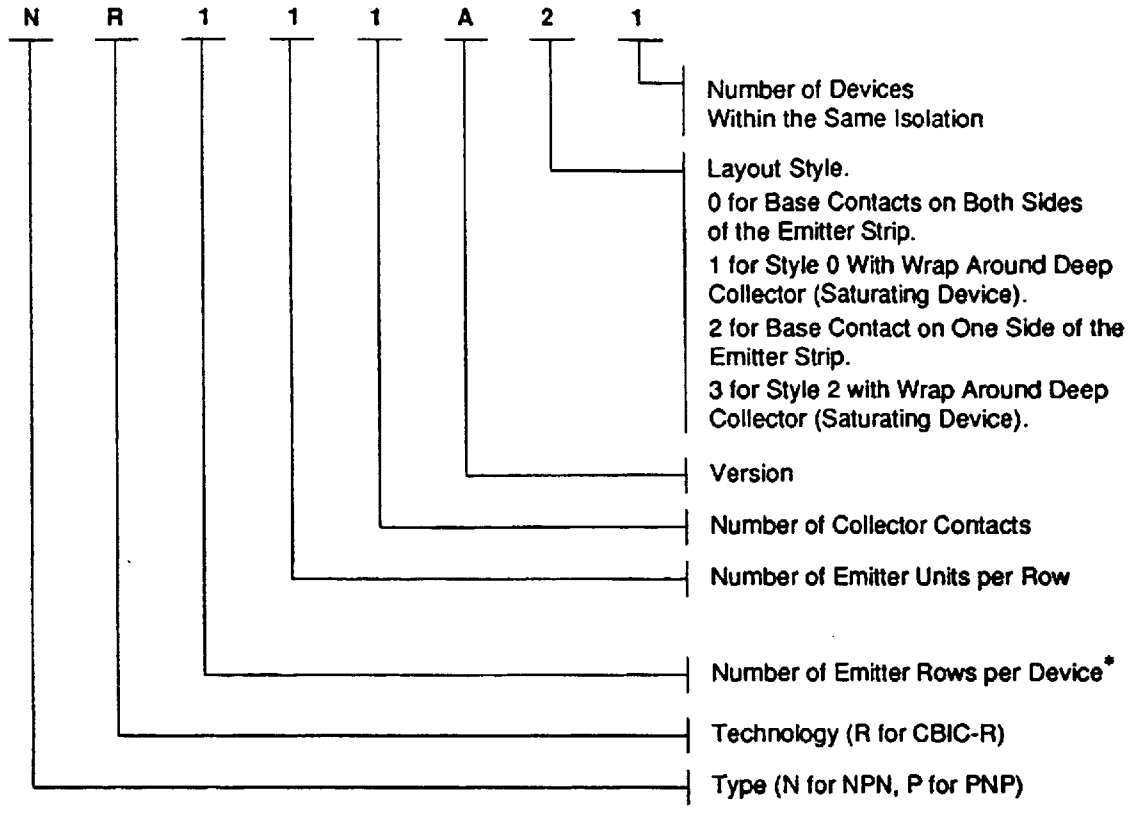
Current Gain Characteristics (NR111A21)



Current Gain Characteristics (PR111A21)



Transistor Name Coding Scheme — CBIC-R



* Integers greater than 9 are represented by alpha characters, such as A = 10, B = 11, C = 12, etc.

Examples:

PR352A21 — A PNP transistor in the CBIC-R technology with three emitter strips each containing five emitters and two collector contacts. The layout architecture is one PR352A2 device in a single isolation.

NR151A01 — An NPN transistor in the CBIC-R technology with one emitter strip, containing five emitters and one collector contact. The base contact is made to both sides of the emitter. The layout architecture is one NR151A0 device in a single isolation.