Am7000 Series

T-42-11-09

Silicon-Gate HCMOS Logic Arrays

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- Silicon-gate 2.0-micron (drawn) HCMOS technology
- Speeds higher than 74S TTL — 1.4 ns through 2-input NAND gate and interconnection
  - $T_A = 25°C$
  - Fanout = 2
  - $V_{DD} = 5$ V
- Optimal block structure of 2N and 2P transistors
- Complexities ranging from 2,224 to 10,013 blocks
- Pin counts ranging up to 224
- Fully supported by LDS* (LSI Design System), Daisy LOGICIAN*, Mentor Graphics IDEA 1000*, Valid Logic SCALDsystem*, and FutureNet Dash-1 Schematic Designer* Systems
- Extensive macrocell and macrofunction libraries
- All non-power pads configurable as inputs, outputs, or bidirectional I/O
- TTL/CMOS I/O compatibility
- Configurable output drive up to 12 mA under worst-case commercial conditions
- All inputs and outputs protected from over-voltage and latch-up
- Am7220Q evaluation device available
- Full military capability
- Ceramic and plastic packages

GENERAL DESCRIPTION

The Am7000 Series of silicon-gate HCMOS logic arrays from Advanced Micro Devices exhibits bipolar speeds, while at the same time offers low-power consumption, high-noise margins, and ease of design of HCMOS. The Am7000 Series is implemented in silicon-gate, 2-micron drawn gate length, dual-layer metal interconnection technology. A range of complexities from 2,224 to 10,013 blocks is offered — each block equivalent to a 2-input NAND or NOR gate. Maximum pin counts range up to 224.

The speed and the range of block counts available in the Am7000 Series make it ideal for LSI and VLSI implementation of a variety of high-performance functions. The high-density members of the series can be used for VLSI implementation of complete high-performance sub-system architectures such as intelligent special-purpose processors or multi-function controllers. The low-block count members can be used for the replacement of high-speed logic such as Schottky TTL or even 10K ECL. The intermediate members can be used for high-performance-dedicated peripheral controllers, intelligent support functions, etc.

PRODUCT SELECTOR GUIDE

Device Number	Am7220	Am7320	Am7420	Am7600	Am7840	Am71000
Gate Complexity	2224	3192	4242	6072	8370	10,013
Maximum Pads[3]:						
Plastic or Ceramic	78	96	114	138	166	174
Ceramic	106	128	150	186	222	232
Maximum I/O Pads[3]:						
Plastic or Ceramic	70	80	98	122	150	158
Ceramic	98	112	134	170	206	216
Maximum Package Pins[4]:						
Plastic or Ceramic	76	92	110	134	162	170
Ceramic	104	124	146	182	218	228
Gate Speed (ns)[1]:						
Typical	1.4	1.4	1.4	1.4	1.4	1.4
Maximum[2]	2.4	2.4	2.4	2.4	2.4	2.4

Notes: 1. Two-input NAND gate, fanout = 2; and statistically necessary interconnection.
2. $T_A = 0$ to $+70°C$, $V_{DD} = 5$ V ±5%.
3. The difference between the maximum number of pads and I/Os is the number of dedicated V_{DD} or V_{SS} pads. It may be necessary to configure additional I/O pads for V_{DD}/V_{SS}, depending on the number and drive of the output buffers.
4. Wherever possible, the lower pad count plastic or ceramic pad pitch should be used — if ceramic-only pad pitch is used there is no possibility of using plastic package in the future.

Order #07687A

February 1986

FUNCTIONAL DESCRIPTION

The Am7000 Series of arrays is manufactured using an advanced 2-micron, oxide-isolated silicon-gate HCMOS fabrication process. The use of short channel lengths, thin gate oxides and two levels of metal interconnection provides bipolar speeds. The small device structures and low-power consumption also allow high block counts due to the smaller chip size and the minimal heat dissipation. The Am7000 Series eliminates the need in the large majority of applications, for bipolar technology and its attendant limitations — such as low-to-medium complexities, special packaging, cooling, lower noise immunity, etc.

Macrocells

The arrays consist of columns of blocks in the core region, I/O buffers around the periphery, and wiring channels between. Each block consists of 2N and 2P transistors. These blocks can be configured into a variety of logic elements such as exclusive-OR gates or flip-flops using unique metal interconnections. These elements are called macrocells, and are the basic building blocks available to the user. The Am7000 Series contains approximately 150 macrocells. Macrocells needed to support scan testing are available.

Macrofunctions

To specify the logic, a user often defines elements of greater complexity. These more complex elements are called macrofunctions, and are composed of macrocells. Simple macrofunctions are used to hierarchically build higher-level macrofunctions until the logic is completely specified.

A selection of macrofunctions (composed of macrocells) is available in the Am7000 Series library. These macrofunctions implement generic functions such as counters, decoders, shift registers, etc., and are optimized for gate usage and for performance characteristics. Under some circumstances, such as upgrading existing products using 7400/4000 series MSI/SI functions — or because of previous familiarity, designers may prefer to use 7400/4000 series functions as building blocks. A large selection of these elements is also provided in the Am7000 Series macrofunction library.

Table 1 lists some representative macrofunctions. Detailed information on available macrocells and macrofunctions is provided in other AMD publications. The AC Characteristics section lists some of the commonly used macrofunctions, their propagation delays, and their complexity.

TABLE 1. REPRESENTATIVE MACROFUNCTIONS

Adders	Up to 16 bits
Comparators	Magnitude; Equality; 4 and 8 bits
Parity Generators	8-bit odd parity detector
Registers	8-bit data latch; 8-bit data register, clear direct; 4-bit shift register, sync parallel load and clear; 4-bit shift register, async parallel load
Counters	Binary, BCD, Gray and Johnson counters in a variety of configurations; large modulo counters
Clock Generators	Two-phase clock generator, buffered
Decoders	2-to-4 decoders; 3-to-8 decoders; 4-to-10 decoders
ALUs	16-bit 181 type
2900 Family	2901; 2909; 2910
FIFO	16 x 4
Multipliers	8 x 8; 12 x 12; 16 x 16

Macrocells for Level-Sensitive Scan Design

The Am7000 Series macrocell libraries also contain macrocells needed to support scan testing. Scan testing simply involves the capability to serially shift the contents of all internal flip-flops off-chip in a test mode.

I/O Buffers

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Each I/O buffer around the perimeter of the array consists of an input-protection circuit and large N- and P-channel transistors for driving off-chip loads. Eight through twenty-eight dedicated power and ground pads are provided. All the remaining peripheral cells can be used as input, output, or bidirectional three-state. If necessary, they can even be used to buffer heavily loaded internal signals. Further flexibility is available in the use of pullup/pulldown resistors and choice of input levels and current drive:

- All I/O pads have pullup and pulldown resistors available (typically 80 kilohm).
- Output drive may be tailored to 1.0 mA, 2.0 mA, or 4.0 mA. Additional drive capability may be obtained by paralleling two (8.0 mA) or three (12.0 mA) drivers.
- Three input-voltage level options are available on any I/O pin. CMOS buffers provide standard 1.5-V and 3.5-V input levels. TTL-input buffers provide standard 0.8-V and 2.0-V (2.25-V on industrial and military devices) input levels. Schmitt trigger inputs provide 1.5 V of hysteresis (see DC Characteristics section for more details).
- All I/Os are protected against latch-up and static discharge.

Propagation Delays

Propagation delays of the Am7000 Series logic elements are a function of several factors: fanout, interconnection routing, junction temperature, supply voltage, processing tolerance, input-transition time, and input-signal polarity.

The LDS (LSI Design System) design-verifier program automatically generates the propagation delays for all networks once the network has been entered into the development system or workstation. Prior to layout, these values are based on estimated interconnections. After layout, the program is rerun and final delay values — based on actual interconnections — are obtained.

Prior to availability of the network in computer format, approximate delay calculations may be used. This may be done as follows:

Propagation delays for some popular macrocells are shown in the AC Characteristics' section for nominal processing — 5-V operation, 25°C temperature — and for various fanouts — with statistically estimated wirelengths.

The effect of temperature may be estimated from Figure 1. The maximum junction temperature will determine a temperature multiplier (K_T). The AMD Macrocell Manual should be consulted for package thermal resistances. In CMOS technology, the junction temperature is usually close to the ambient temperature. Similarly, Figure 2 shows the effect of supply voltage (K_V). AMD assumes a 40% variability resulting from all other factors including processing — or in other words, a factor of 1.4 for the worst-case processing multiplier (K_O).

The maximum propagation is: $T_{MAX} = K_O \times K_T \times K_V \times T_{TYP}$

A simple example will illustrate the technique:

The circuit of Figure 3 must operate over 0 to 70°C and at 4.75- to 5.25-volt power supply voltage. Using Figures 1 and 2, and the K_O multiplier, we determine the worst-case maximum delay to be $1.4 \times 1.16 \times 1.07 = 1.74$ times the typical delay.

The FD1 flip-flop, clocked by the signal CLK, feeds an AO2 AND-NOR gate combination and three other loads. The AO2

drives a BTS1 three-state buffer directly. The BTS1 drives off-chip (through a PC board) and on to another array using a TLCHT input-level shifter. The total capacitance at the output, interconnect, and input is 50 pF. The TLCHT drives the D input of an FD1 D flip-flop and two other loads. The delay charcteristics of all the macrocells are tabulated as shown in Table 2. The total clock-to-clock delay is 17.3 ns typical, and 17.3 x 1.74 = 30.1 ns worst-case. LDS programs are used to obtain accurate delays after the logic has been entered into the system.

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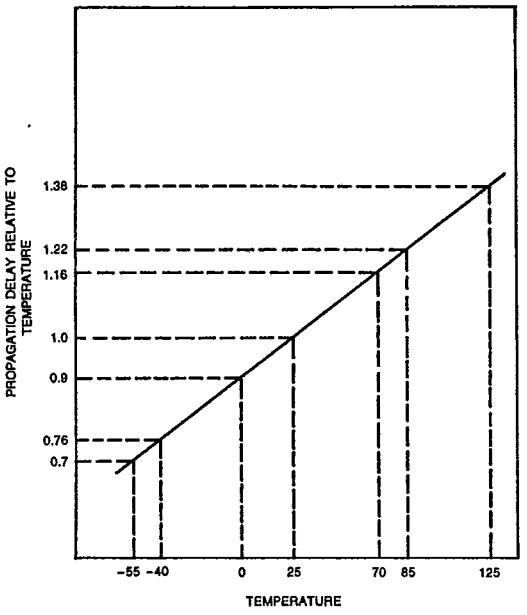

Figure 1. CMOS Propagation Delays as a Function of Temperature

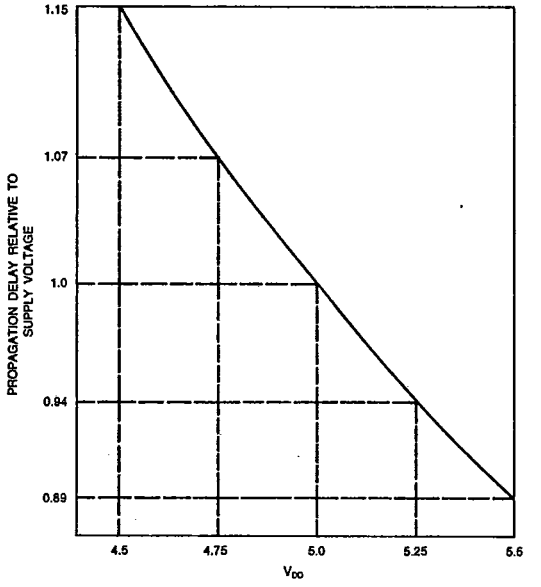

Figure 2. CMOS Propagation Delays as a Function of Supply Voltage

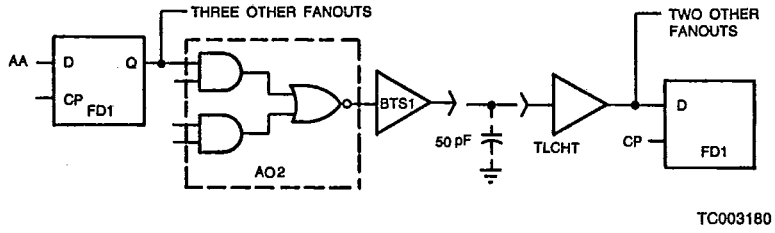

Figure 3. Example of Worst-Case Propagation Delay through Critical Path

TABLE 2. PROPAGATION DELAY CALCULATION

Input Signal AA	FD1 (FO = 4)	AO2 (FO = 1)	Three-State Output BTS1 (C_L = 50 pF)	TLCHT (FO = 3)	FD1 Setup	Typical Path Delay	W.C. Path Delay
Goes HIGH	4.4	1.2	6.8	4.4	1.5	17.3	30.1
Goes LOW	3.2	2.9	5.4	3.1	1.5	16.1	28.0

Product Options Available

The Am7000 Series is offered in a variety of operating-temperature ranges and production-processing flows. The standard operating-temperature ranges offered are Military (−55°C to +125°C), Industrial (−40°C to +85°C), and Commercial (0 to +70°C). Other special temperature ranges are also available (consult the local AMD sales office to obtain additional information).

Production flow options other than standard commercial flow are available. Various military flows — including MIL-STD-883C, Level B — are supported.

Packaging

The Am7000 Series can be packaged in a variety of plastic and ceramic dual-in-line packages, leadless and leaded chip carriers, and pin grid arrays. Plastic packages are not available for the full military temperature range. The compatibility chart of Table 3 (Package Selector Guide for the Am7000 Series) lists the packages and pin counts available for the various members of the Am7000 Series. See LSI Application Note A33, Logic Array Packaging, for more details.

TABLE 3. PACKAGE SELECTOR GUIDE FOR THE Am7000 SERIES

Device Number	Am7220	Am7320	Am7420	Am7600	Am7840	Am71000
Dual-In-Line Packages:						
Plastic (Note 1)	22 +	24 +	28 +	28 +	N/A	N/A
Ceramic (Note 2)	22 +	24 +	24 +	40 +	64 +	64 +
Chip Carriers:						
Plastic Leaded (Note 3)	44 +	44 +	44 +	44 +	68 +	68 +
Ceramic Leadless (Note 4)	28 +	44 +	52 +	68 +	84 +	84 +
Pin Grid Arrays:						
Ceramic (Note 5)	64 +	64 +	64 +	64 +	68 +	68 +
Fiberglass (Note 6)	68 +	68 +	68 +	68 +	68 +	68 +

Notes: Package families include:
1. Ceramic DIPs — 24, 28, 40, 42, 48, and 64 leads
2. Plastic DIPs — 24, 28, 40, 48, and 64 (0.070″ pitch) leads
3. Ceramic LCCs — 28, 44, 52, 68, 84, and 100 leads
4. Plastic LCCs — 68, 84, and 124 leads
5. Ceramic PGAs — 64, 68, 84, 100, 120, 144, 180, and 224 leads
6. Fiberglass PGAs — 68, 84, 100, 120, 144, and 180 leads

Am7220Q Evaluation Device

Potential users of the Am7000 Series can — prior to design commencement — measure its performance under their own unique system and environmental conditions. The Am7220Q contains a variety of logic functions such as 2-, 3-, or 4-input NAND gates; 2- or 4-input NOR gates; output buffers with different drive capability; a variety of different flip-flops, inverters, TTL-to-CMOS level shifters, etc. In addition, complex circuits such as ALUs and up-down counters are included. These functions are implemented in several different test circuits. Technology parameters such as propagation delays, power consumption, input/output characteristics, etc., can be measured under different conditions of loading, supply voltage, ambient temperature, etc. See the Am7220Q Product Specification for additional information.

Getting Started on the Design

To get started on a logic array design, the following sequence of preliminary steps is suggested.

1. The complete system is partitioned into building blocks. An effort should be made to minimize the I/O count when partitioning between circuits. Each functional block to be implemented in a logic array is then converted to a logic schematic. Users can describe their logic using AMD's macrofunction/macrocell libraries or 7400/4000 series functions. The use of hierarchical design techniques on the LDS design system allows design expression at these various levels. Ultimately, when the logic is compiled on LDS, it is "flattened" into macrocells. It is advisable to structure the complete schematic as a set of functional sub-systems such as a 16-bit ALU, a data receiver, a programmable timer, or a register file, to allow comprehensible and easy hierarchical simulation.
2. The base clock frequency and the critical-path timing are necessary to make the correct choice of technology. The Am7000 Series can support designs operating up to 40 MHz. The critcal-path timing is determined based on macrocell propagation delays (see Propagation Delays and AC Characteristics sections). To verify the capability of a technology under the unique environmental and system conditions of a user application, an evaluation device such as the Am7220Q may be used.
3. The next step is an estimation of the gate count and I/O requirements of the logic to establish the complexity of the array required. For gate count equivalence tables for the 7400/4000 series or macrocells/macrofunctions, see LSI Application Note A31A. The gate utilization actually achieved in a given array for a specific design depends on the gate count, pin requirements, as well as factors that affect routability. For example, block-oriented logic with minimum inter-block interaction provides high utilization; whereas wide, extensive busing lowers it.
4. Finally, a choice of array size, package, temperature range, performance, etc., is made.

During all these steps, the customer usually consults AMD to ensure compatibility and completeness.

A set of specifications is then submitted to AMD. After their acceptance, the logic designer takes a one week LDS training class and starts his design. The design process and the user

interface to LDS are oriented toward the skills of a system designer rather than a semiconductor device or VLSI designer.

Design Support and Interface

The LDS System may be used for logic specification, basic network verification (gate usage, I/O pad usage, average fanout per net, estimated automatic wireability), logic simulation and performance analysis, automatic placement and routing, resimulation with actual wire-lengths to verify the AC performance, mask P.G.-tape generation and test-tape generation. The basic design flow is outlined in Figure 4.

V_{DD} and V_{SS} Requirements

HCMOS is a fast technology rivaling Schottky TTL speeds. High-speed operation places stringent requirements on the ground busing and the number of power and ground pads required to avoid current spikes when the output buffers charge and discharge their output capacitance.

To increase noise immunity, two ground buses (V_{SS} and V_{SS2}) are used on the array. All inputs and interior are logic on the V_{SS2} bus, all output buffers on the V_{SS}. These two buses are connected to independent package-ground pins.

More than two power (V_{DD}) and ground (V_{SS}) pins may be required to support several high-drive outputs switching simultaneously at fast speeds. For example, the type B1 buffer has a low impedance for high-drive capability and may provide a peak transient current of 50 mA. If sixteen B1 buffers switch simultaneously, a peak current of nearly one amp is generated through the V_{SS} bus, bonding wire, package, and out to the PC board. There are therefore guidelines on the number of V_{SS} and V_{DD} pins based on three factors:

1. The driver capability of the buffer,
2. The number of buffers switching simultaneously, and
3. The location of power and ground pads relative to the outputs.

Each V_{SS} pad can support a maximum of sixteen B1-equivalent buffers (eight on each side of the V_{SS} pad). Each V_{DD} pad can support up to thirty-two B1-equivalent B1 buffers (sixteen per side). The number of V_{SS2} pads required depends on the array size and on the number of output buffers used. Table 4 shows the minimum number of V_{SS2} pads required by each array size.

Output types can be mixed — high drive when needed, low drive when acceptable — to reduce noise and power dissipation. Note that inputs may be ignored when calculating power pins since CMOS inputs sink and source minimal current. Table 5 shows the current drive capabilities of some of the more common output-buffer types compared to the B1 buffer.

TABLE 4. MINIMUM ALLOWABLE V_{SS2} PADS REQUIRED BY EACH ARRAY SIZE

Array	Minimum Number of V_{SS2} Pads Required
Am7220	2
Am7320	4
Am7420	4
Am7600	4
Am7840	4
Am71000	4

TABLE 5. CURRENT DRIVE CAPABILITIES OF OUTPUT BUFFER TYPES

Buffer Type	B1 Equivalent Drive Capability
B14	0.25
B18	0.50
B1	1.00
B2	2.00
B3	3.00

Dedicated V_{SS}, V_{SS2}, and V_{DD} power pads are separated into primary and secondary pads. The primary pads are grouped together in sets of two or four at the midpoint of each of the four sides. The secondary pads are located individually near the four corners of the chip. All primary pads must be used first. Primary pads cannot be used as signal pads; if additional power pads are required, the secondary power pads will be used. All secondary pads not used for power may be used as a signal pad.

If pin count is high, request a "tight pitch" footprint — each Am7000 Series device is available with shorter pad-to-pad spacing — or a "tighter pad pitch," allowing approximately 25% more pads. This pad pitch can only be used with ceramic packages.

Power Dissipation

Power dissipation in CMOS circuits is made up of four basic elements.

The first is due to leakage. It constitutes the quiescent power dissipation and is essentially negligible (few microwatts) for CMOS technology.

The second is DC current through ON transistors. This can be from a variety of sources:

- A LOW on an input with a pullup resistor (all TTL inputs have nominal 80-kilohm pullup resistors),
- Outputs which sink or source current,
- Any unconnected inputs without a pullup or pulldown,
- Any internal gates whose inputs are floating (e.g., a data bus with all the lines disabled),
- Inputs at worst-case levels, particularly TTL inputs at 2 volts.

Care should be exercised during logic design to make sure that there is a test condition in which all this DC current may be turned off, so that DC leakage may be easily measured.

The third source of power dissipation is due to overlap currents when the P-and N-transistors are switching from the HIGH-to-LOW state or vice-versa. This contributes less than 10% of the power dissipated and occurs for the transition period when $V_{TH(N)} < V_{IN} < V_{DD} - V_{TH(P)}$.

The fourth and the most important factor is the charging and discharging of circuit capacitance. The charging of a capacitor C to a voltage V through a P-channel device builds up a charge CV and stores energy CV^2f. This AC power dissipation usually contributes in excess of 90% of the total power dissipated. Thus, the power dissipation in a CMOS circuit is essentially a function of the frequency and logic configuration. Each internal gate in the Am7000 Series typically consumes 18 microwatts/gat/MHz. Each I/O buffer, with its higher output capacitance and larger capacitive loads, consumes 25 microwatts/I/O/MHz/pF. The total power consumption is the sum of the power dissipated by all the gates and I/O buffers switching each cycle. Table 6 illustrates typical power calculations.

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TABLE 6. POWER DISSIPATION CALCULATION EXAMPLE

Parameter	Array Type	
	Am7220	Am7600
Number of available gates	2224	6072
Percentage of gates utilized	85	75
Number of gates utilized	1890	4554
Number of gates switching each cycle (15%)	284	683
Dissipation/gate/MHz (μW)	18	18
Total core dissipation/MHz (mW)	5.1	12.3
Number of available I/O buffers	98	170
Percentage of I/O buffers utilized as outputs	50	50
Number of I/O buffers utilized as outputs	49	85
Number of I/O outputs switching each cycle (20%)	10	17
Dissipation/output buffer/MHz/pF (μW)	25	25
Output capacitive load (pF)	50	50
Dissipation/output buffer/MHz (mW)	1.25	1.25
Total output buffer dissipation/MHz (mW)	12.50	21.30
Total dissipation/MHz (mW)	17.60	33.60
Total dissipation at 10-MHz clock speed (mW)	176	336
Total dissipation at 25-MHz clock speed (mW)	440	840

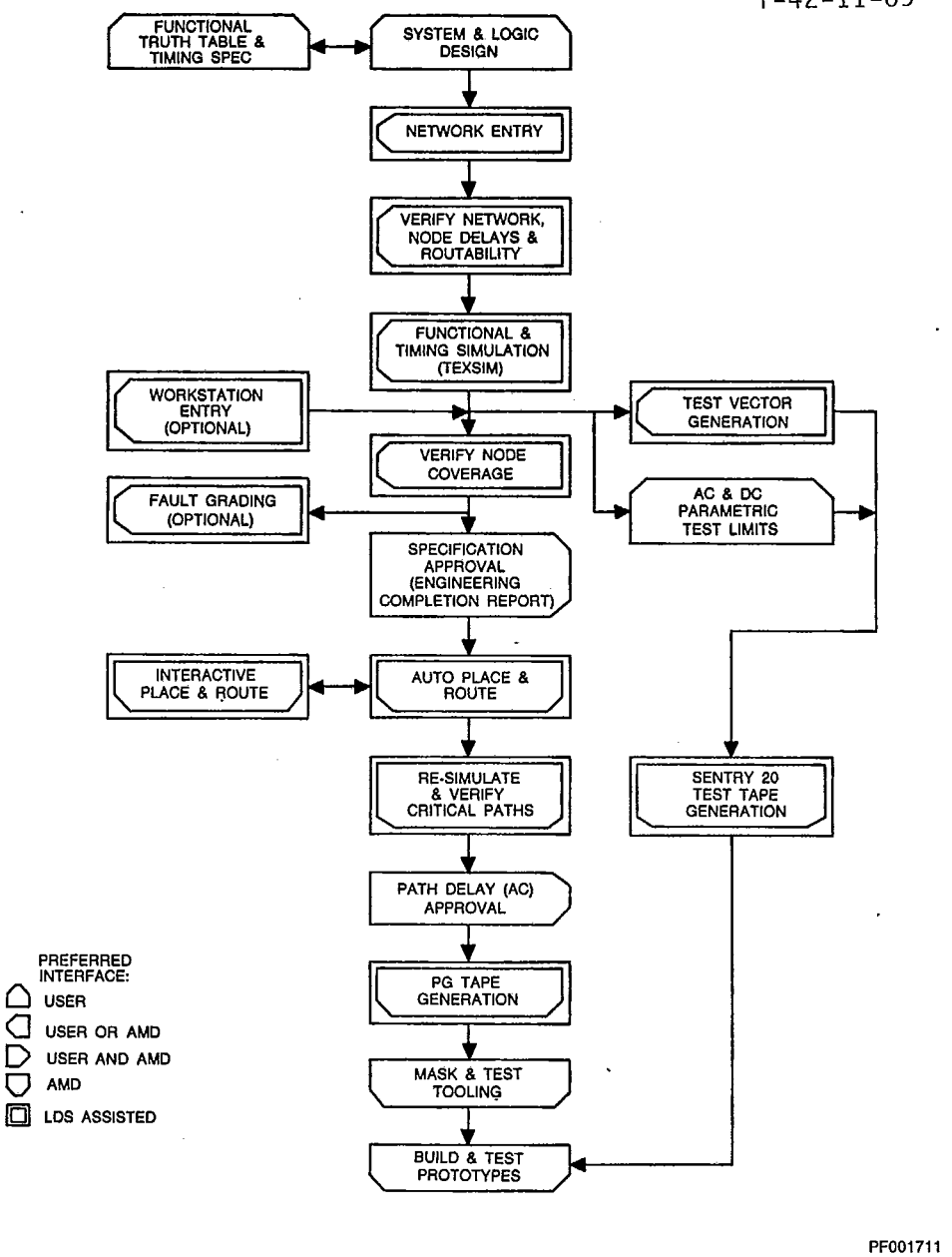

Figure 4. Array Development Flowchart

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
- Ceramic Packages ..... −65 to +150°C
- Plastic Packages ..... −40 to +125°C

Ambient Temperature with Power Applied ..... −55 to +125°C
DC Supply Voltage ..... −0.3 to +7.0 V
Input Voltage ..... −0.3 to V_{DD} +0.3 V
DC Input Current ..... ±10 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
- Temperature (T_A) ..... 0 to +70°C
- Supply Voltage (V_{DD}) ..... +3.0 to +6.0 V

Industrial (I) Devices
- Temperature (T_A) ..... −40 to +85°C
- Supply Voltage (V_{DD}) ..... +3.0 to +6.0 V

Military (M) Devices
- Temperature ..... −55 to +125°C
- Supply Voltage ..... +3.0 to +6.0 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified. (Note 1)

Table continued on next page.

Parameter Symbol	Parameter Description	Test Conditions			Min.	Typ.	Max.	Units
V_{IL}	Input LOW Voltage on TTL Inputs						0.8	V
	CMOS Levels						1.5	
V_{IH}	Input HIGH Voltage on TTL Inputs		C Devices		2.0	1.7		V
			I/M Devices		2.25	1.7		
	on CMOS Levels				3.5	3.0		
V_{T+}	Schmitt-Trigger, Positive-going Threshold					3.0	4.0	V
V_{T-}	Schmitt-Trigger, Negative-going Threshold				1.0	1.5		V
	Hysteresis, Schmitt Trigger	V_{IL}-to-V_{IH}, V_{IH}-to-V_{IL}			1.0	1.5		V
I_{IN}	Input Current, on CMOS, TTL Inputs	$V_{IN} = V_{DD}$			−10.0	±1	10.0	µA
	on Inputs with Pulldown Resistors					45.0	200.0	
	on CMOS Inputs	$V_{IN} = V_{SS}$			−10.0	±1	10.0	
	on TTL Inputs and Inputs w/Pullup Resistors				−200.0	−70.0		
V_{OH}	Output HIGH Voltage on Type B14	I_{OH} =	Com.	Mil.	2.4	4.5		V
	on Type B18		− 1 mA	−0.8 mA				
	on Type B1		− 2 mA	−1.6 mA				
	on Type B2 (Note 2)		− 4 mA	−3.2 mA				
	on Type B3 (Note 3)		− 8 mA	−6.4 mA				
			−12 mA	−9.6 mA				
V_{OL}	Output LOW Voltage on Type B14	I_{OL} =	Com.	Mil.		0.2	0.4	V
	on Type B18		1 mA	0.8 mA				
	on Type B1		2 mA	1.6 mA				
	on Type B2 (Note 2)		4 mA	3.2 mA				
	on Type B3 (Note 3)		8 mA	6.4 mA				
			12 mA	9.6 mA				

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DC CHARACTERISTICS

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
I_{OZ}	Three-State Output Leakage Current	$V_{OH} = V_{SS}$ or V_{DD}	-10.0	±1	10.0	µA
I_{OS}	Output Short-Circuit Current (Note 4)	V_{DD} = Max., $V_O = V_{DD}$	25.0		90.0	mA
		V_{DD} = Max., V_O = 0 V	-15.0		-60.0	
I_{DD}	Quiescent Supply Current	$V_{IN} = V_{DD}$ or V_{SS}	User-Design Dependent			
C_{IN}	Input Capacitance	Any Input (Note 5)	2.0	2.0	2.0	pF
C_{OUT}	Output Capacitance	Any Output (Note 6)	4.0	4.0	4.0	pF

Notes: 1. Specified at V_{DD} = 5 V ±5% ambient temperature over the specified temperature range. Military temperature range is -55 to +125°C, ±10% power supply (ceramic packages only); industrial temperature range is -40 to +85°C, ±5% power supply; commercial temperature range is 0 to +70°C, ±5% power supply.
2. Requires two output pads.
3. Requires three output pads.
4. Type B1 output. Output short-circuit current for other outputs will scale. Not more than one output may be shorted at a time for a maximum duration of one second.
5. Not applicable to assigned bidirectional buffer (excluding package).
6. Output using single buffer structure (excluding package).

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AC CHARACTERISTICS over operating range unless otherwise specified. (Note 1)
V_{DD} = 5 V, T_A = 25°C
Note: Delays through interconnect are included. Interconnect wirelengths are assumed from statistical distributions for given fanouts.
Table continued on next page.

Macrocell	Input Transition	Propagation Delays: Output Load Capacitance 15 pF	50 pF	85 pF	100 pF	Equivalent Gate Count
UNIDIRECTIONAL BUFFERS						
Three-state Output Buffer with 1 mA Drive (BTS14)	t_{PHL} t_{PLH}	9.1 5.5	21.1 10.4	33.3 15.2	38.5 17.3	5
Three-state Output Buffer with 12 mA Drive (BTS3)	t_{PHL} t_{PLH}	4.8 4.8	6.2 5.2	7.6 5.5	8.1 5.7	11
THREE-STATE BIDIRECTIONAL BUFFERS						
Three-state I/O Buffer with 4 mA Drive (BTS7)	t_{PHL} t_{PLH}	3.7 4.1	6.6 5.5	8.4 6.8	10.7 7.4	7
Three-state I/O Buffer with Pullup (BTS7U)/ Pulldown (BTS7D)	t_{PHL} t_{PLH}	3.7 4.1	6.6 5.5	9.5 6.8	10.7 7.4	7
OUTPUT BUFFERS						
Output Buffer with 1 mA Drive (B14)	t_{PHL} t_{PLH}	8.3 4.7	20.3 9.6	32.5 14.2	37.7 16.5	1
Output Buffer with 12 mA Drive (B3)	t_{PHL} t_{PLH}	5.6 6.8	7.0 7.2	8.4 7.5	9.0 7.7	2

		Fanout 1	2	3	4	8	
INPUT RECEIVERS							
Input Buffer with CMOS Inputs (IBUF)	t_{PHL} t_{PLH}	2.9 3.1	2.9 3.2	3.0 3.2	3.0 3.3	3.1 3.5	0
Input Buffer with Schmitt Trigger (SCHMIT1)	t_{PHL} t_{PLH}	4.3 3.0	4.4 3.2	4.5 3.3	4.6 3.5	4.9 4.1	3
Input Buffer with TTL Inputs (TLCHT)	t_{PHL} t_{PLH}	4.2 3.0	4.3 3.1	4.4 3.1	4.4 3.2	4.7 3.5	0
INTERNAL BUFFERS							
Single Inverter (IV)	t_{PHL} t_{PLH}	0.8 1.5	0.9 1.8	1.1 2.1	1.2 2.4	1.7 3.6	1
Power Inverter (IVP)	t_{PHL} t_{PLH}	0.6 1.0	0.7 1.2	0.7 1.3	0.8 1.5	1.1 2.1	1-2
LOGIC GATES							
Two-input Exclusive OR (EO)	t_{PHL} t_{PLH}	2.5 2.0	2.6 2.1	2.7 2.3	2.8 2.4	3.1 3.1	3
Two-input NAND (ND2)	t_{PHL} t_{PLH}	1.0 1.4	1.2 1.7	1.4 2.0	1.6 2.4	2.5 3.6	1
Three-input NAND (ND3)	t_{PHL} t_{PLH}	1.5 1.7	1.8 2.0	2.1 2.3	2.4 2.6	3.6 3.8	2
Four-input NAND (ND4)	t_{PHL} t_{PLH}	1.6 1.7	2.0 2.0	2.4 2.3	2.8 2.6	4.3 3.8	2
Eight-input NAND (ND8)	t_{PHL} t_{PLH}	3.7 3.0	3.8 3.1	3.9 3.3	3.9 3.5	4.3 4.2	6
Two-input NOR (NR2)	t_{PHL} t_{PLH}	1.0 2.0	1.1 2.5	1.2 3.1	1.4 3.6	1.9 5.8	1
Three-input NOR (NR3)	t_{PHL} t_{PLH}	1.2 3.3	1.3 4.1	1.5 4.9	1.6 5.7	2.2 9.0	2
Four-input NOR (NR4)	t_{PHL} t_{PLH}	1.3 4.8	1.4 5.9	1.6 7.0	1.7 8.1	2.2 12.3	2
Eight-input NOR (NR8)	t_{PHL} t_{PLH}	2.2 4.9	2.3 5.1	2.3 5.2	2.4 5.4	2.7 6.0	6

AC CHARACTERISTICS

T-42-11-09

V_{DD} = 5 V, T_A = 25°C

Macrocell	Input Transition	Fanout 1	2	3	4	8	Equivalent Gate Count
FLIP-FLOPS							
D Flip-flop (FD1)	t_{PHL}	2.8	2.9	3.1	3.2	3.8	5
	t_{PLH}	3.5	3.8	4.1	4.4	5.7	
	t_S	1.5	1.5	1.5	1.5	1.5	
	t_H	1.0	1.0	1.0	1.0	1.01	
D Flip-flop with Scan Test Inputs (FD1S)	t_{PHL}	4.0	4.2	4.4	4.6	5.5	7
	t_{PLH}	3.7	4.0	4.4	4.7	6.0	
	t_S	2.50	2.50	2.50	2.50	2.50	
	t_H	1.25	1.25	1.25	1.25	1.25	
D Flip-flop with Set Direct, Clear Direct (FD3)	t_{PHL}	2.8	2.9	3.1	3.2	3.8	7
	t_{PLH}	3.5	3.8	4.1	4.4	5.7	
	t_S	1.5	1.5	1.5	1.5	1.5	
	t_H	0	0	0	0	0	
D Flip-flop with Set Direct, Clear Direct, and Scan Test Inputs (FD3S)	t_{PHL}	4.0	4.2	4.4	4.6	5.5	9
	t_{PLH}	3.7	4.0	4.4	4.7	6.0	
	t_S	2.75	2.75	2.75	2.75	2.75	
	t_H	1.50	1.50	1.50	1.50	1.50	
J-K Flip-flop (FJK1)	t_{PHL}	2.8	2.9	3.1	3.2	3.8	8
	t_{PLH}	3.5	3.8	4.1	4.4	5.7	
	t_S	2.50	2.50	2.50	2.50	2.50	
	t_H	0	0	0	0	0	
J-K Flip-flop with Scan Test Inputs (FJK1S)	t_{PHL}	4.3	4.5	4.7	4.9	5.8	10
	t_{PLH}	4.0	4.3	4.6	5.0	6.2	
	t_S	3.50	3.50	3.50	3.50	3.50	
	t_H	0	0	0	0	0	
LATCHES							
Gated D Latch (LD1)	t_{PHL}	2.9	3.0	3.2	3.3	3.9	3
	t_{PLH}	3.0	3.4	3.7	4.0	5.3	
	t_S	0	0	0	0	0	
	t_H	1.0	1.0	1.0	1.0	1.0	
S-R Latch with Separate Input Gates, Set Direct and Reset Direct (LSR1)	t_{PHL}	1.9	2.2	2.5	2.8	3.9	4
	t_{PLH}	3.0	3.5	4.0	4.6	6.7	
D Latch with Scan Test Inputs (LS1)	t_{PHL}	2.9	3.0	3.2	3.3	3.9	6
	t_{PLH}	3.7	4.0	4.3	4.7	5.9	
	t_S	2.50	2.50	2.50	2.50	2.50	
	t_H	1.00	1.00	1.00	1.00	1.00	
MISCELLANEOUS							
2-to-1 Multiplexer (MUX21LA)	t_{PHL}	1.5	1.5	1.6	1.7	2.0	3
	t_{PLH}	1.3	1.4	1.6	1.8	2.4	

AC CHARACTERISTICS

V_{DD} = 5 V, T_A = 25°C

Macrofunctions		Performance	Gate Count
16-Bit Barrel Shifter		12 ns	116
8-Bit Barrel Shifter		9 ns	55
16-Bit Adder		21 ns	248
16-Bit 74181 Type ALU	Any Input to F	29 ns	363
16-Bit 100181 Type ALU	Any Input to F	39 ns	558
8 x 8 Multiplier		39 ns	517
12 x 12 Multiplier		47 ns	1102
16 x 16 Multiplier		50 ns	1796
2901 4-Bit ALU Slice	Minimum Clock Period	33 ns	720
2909 μProgram Sequencer		24 ns	258
2910 μProgram Controller	Minimum Clock Period	36 ns	856
8-Bit Magnitude Comparator		15 ns	87
8-Bit Priority Encoder		11 ns	37
16 x 4 FIFO (Fall-thru type)		—	324

Note 1: Delay for worst-case path with typical interconnection length under nominal conditions (V_{DD} = 5 V, T_A = 25°C).

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