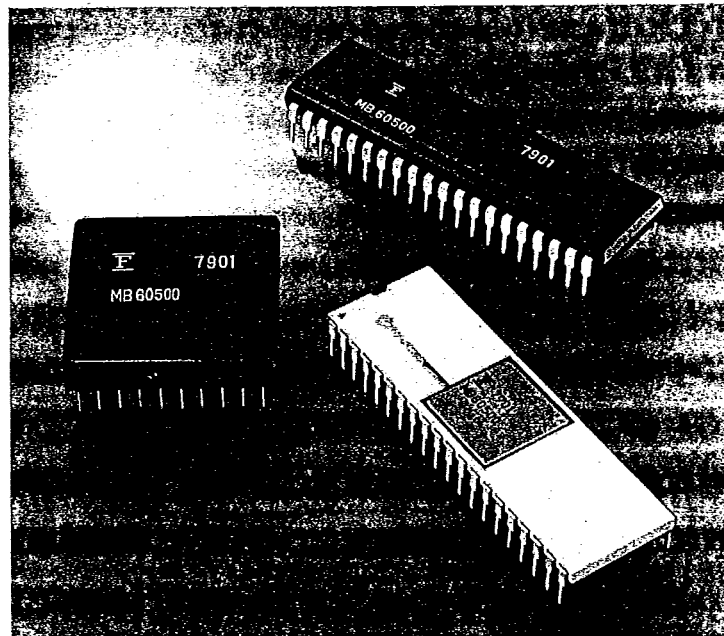


C-2000 Gate Array

MB60K Silicon Gate CMOS LSI

The Fujitsu C-2000 (MB60K Series) is a highly integrated, low power, gate array LSI fabricated with silicon gate CMOS technology. The array consists of 2000 internal basic unit cells (2 input NAND equivalent) and 72 I/O cells. With the application of a customized double-layer metal mask, a wide variety of random logic functions can be made. To assure quick, simple error-free implementation of the metal interconnection routing, Fujitsu utilizes a unique Computer-Aided Design System (CAD) to interface custom specifications with the manufacturing function. This CAD software provides the physical layout of the array, line routing, mask pattern data generation, and test programs as well as computer simulation of the final circuit.

The C-2000 can be packaged in a plug-in type 64 pin square package or 40-pin DIP depending on the number of input and output connections required by the design.



Features

- * Fast turn-around on design (15 weeks typically)
- * Simplified customer interface with CAD support (Only logic design and test pattern information required)
- * Sixty pre-designed logic cells available
- * Standard 40 pin DIP or a plug-in type 64 pin square package
- * Internal gate
 - High speed (5 to 15 ns/gate)
 - Low power dissipation (0 mW: Steady state, 50 mW: Operation)
- * Output buffer
 - Versatile output option (Push-pull, Three-state, Bi-directional bus)
- * Input buffer
 - Clock input buffer option

Absolute Maximum Ratings

Rating	Symbol	Min.	Max.	Unit
Supply Voltage	V_{DD}	$V_{SS}-0.3^*$	7.0	V
Input Voltage	V_I	$V_{SS}-0.3^*$	$V_{DD}+0.3^*$	V
Output Voltage	V_O	$V_{SS}-0.3^*$	$V_{DD}+0.3^*$	V
Temperature under Operation	T_{op}	0	70	°C
Temperature under Storage	T_{st}	-55	150	°C

*Note: Can accept 0.5V in transient (20~30 ns)

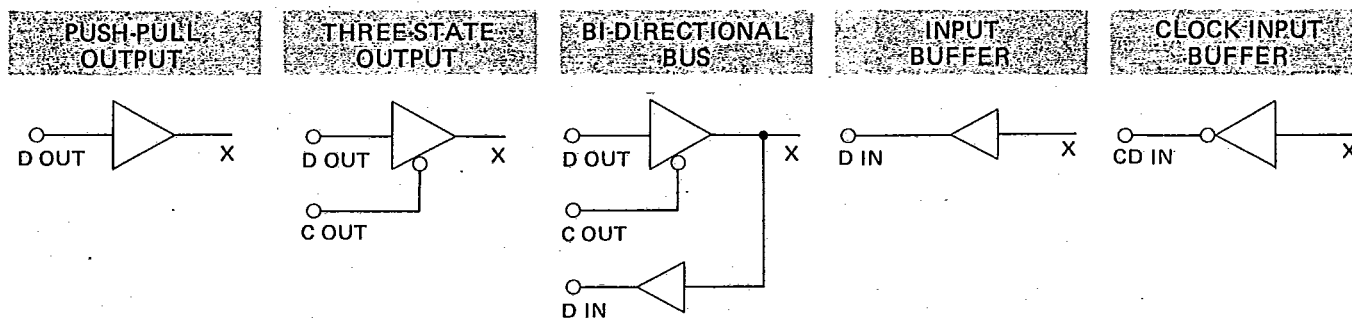
Recommend Operational Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	4.75	5.0	5.25	V
Input Voltage	V_{IH} V_{IL}	2.0		0.8	V V
Temperature under Operation	T_{op}	0		70	°C

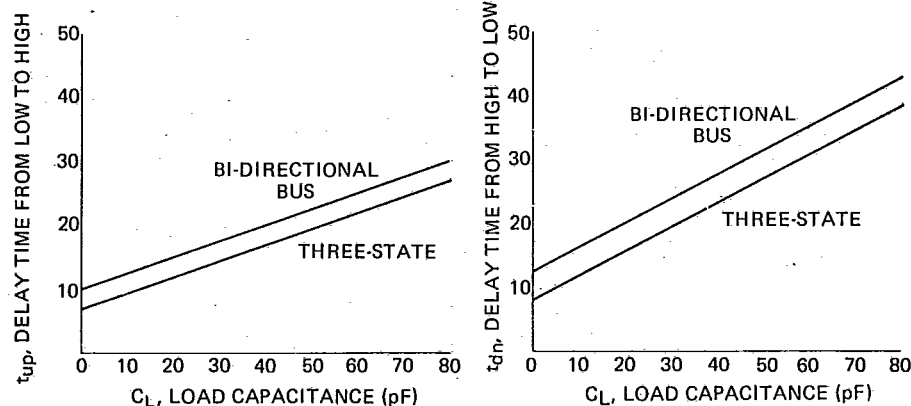
C-2000 Gate Array

T-42-11-09

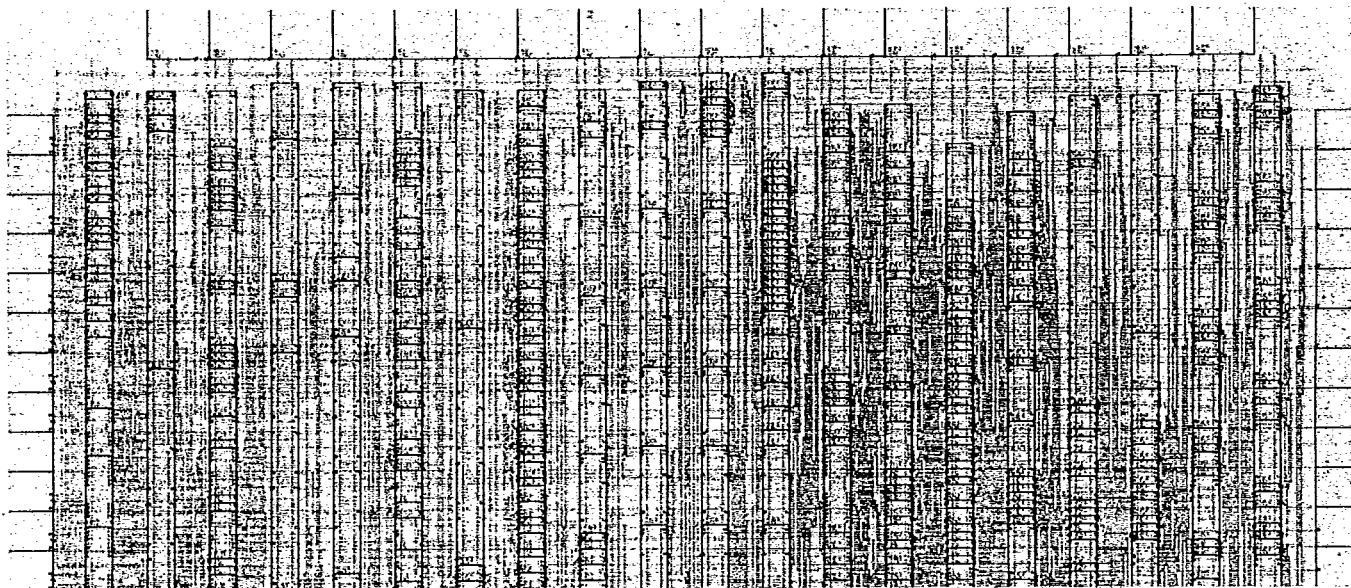
I/O CELL Family



Output Buffer Switching Characteristics (MEASURED AT 1.5 VOLTS)



Chip Design Drawing via CAD



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Printed in Japan