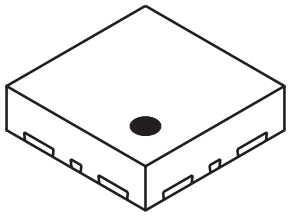
SONY

CXG1172UR

JPHEMT High Power DPDT Switch with Logic Control

12 pin UQFN (Plastic)



Description

The CXG1172UR can be used in wireless communication systems, for example, CDMA handsets, W-CDMA handsets.

The IC has on-chip logic for operation with 1 CMOS control input.

The Sony JPHEMT process is used for low insertion loss and on-chip logic circuit.

Features

- Low insertion loss: 0.3dB@900MHz, 0.45dB@2GHz
- 1 CMOS compatible control line
- Small package size: 12-pin UQFN

Applications

Antenna switch for cellular handsets
W-CDMA, CDMA

Structure

GaAs JPHEMT MMIC

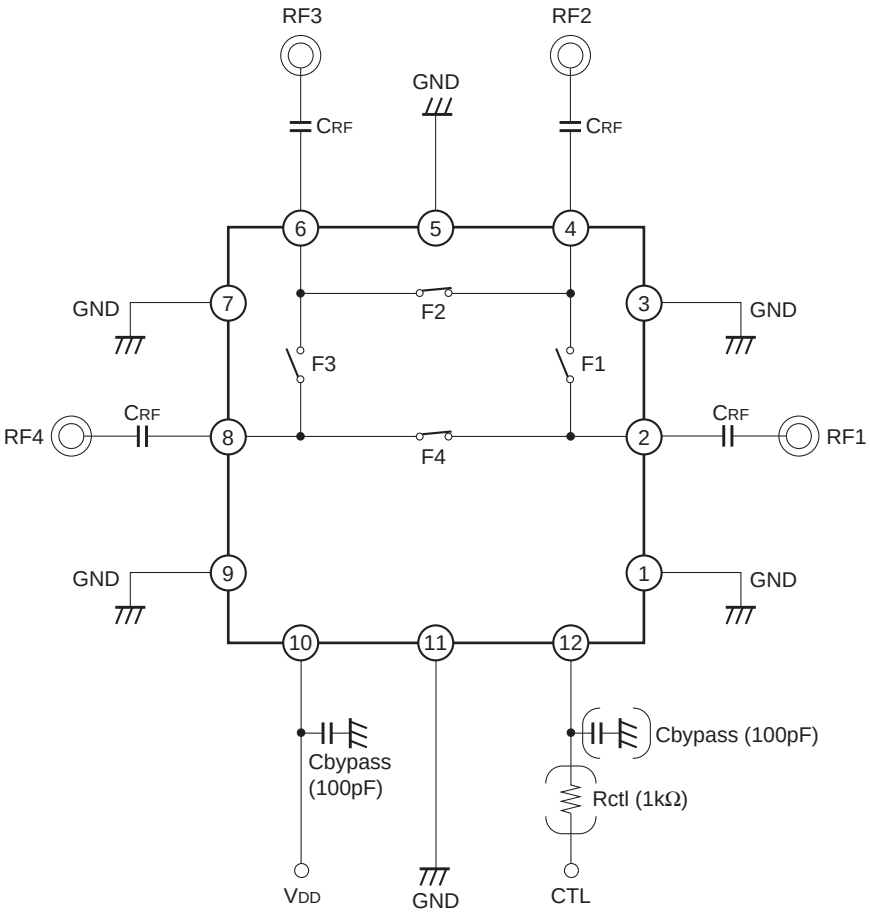
Absolute Maximum Ratings (Ta = 25°C)

• Bias voltage	V_{DD}	7	V
• Control voltage	Vctl	5	V
• Operating temperature	Topr	–35 to +85	°C
• Storage temperature	Tstg	–65 to +150	°C

GaAs MMICs are ESD sensitive devices. Special handling precautions are required.

E04522-PS

Block Diagram and Recommended Circuit



When using this IC, the following external components should be used.

Rctl: This resistor is used to improve ESD performance. 1kΩ is recommended.

C_{RF}: This capacitor is used for RF decoupling and must be used for all applications.

Cbypass: This capacitor is used for DC line filtering. 100pF is recommended.

Truth Table

CTL	ON state	OFF state	F1	F2	F3	F4
L	RF1 – RF2, RF3 – RF4	RF2 – RF3, RF4 – RF1	ON	OFF	ON	OFF
H	RF2 – RF3, RF4 – RF1	RF1 – RF2, RF3 – RF4	OFF	ON	OFF	ON

DC Bias Condition (Ta = 25°C)

Item	Min.	Typ.	Max.	Unit
Vctl (H)	2.0	2.85	3.6	V
Vctl (L)	0	—	0.4	V
V_{DD}	2.5	2.85	3.6	V

Electrical Characteristics (Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Insertion loss	IL	900MHz		0.30	0.50	dB
		1500MHz		0.35	0.55	dB
		2000MHz		0.45	0.65	dB
Isolation	ISO.	900MHz	14	22		dB
		1500MHz	10	18		dB
		2000MHz	8	16		dB
VSWR	VSWR	50Ω		1.2	1.5	—
Switching speed	TSW			8		µs
1dB compression input power	P1dB	*1, *2	33			dBm
Input IP3	IIP3	*3	50	60		dBm
ACLR	ACLR1	*1, ±5MHz		–60	–50	dBc
	ACLR2	*1, ±10MHz		–60	–55	dBc
Harmonics	2fo	*1		–75	–55	dBc
	3fo	*1		–75	–55	dBc
	2fo	*2		–75	–60	dBc
	3fo	*2		–75	–60	dBc
Bias current	I_{DD}	V_{DD} = 2.85V		25	50	µA
Control current	Ictl	Vctl (H) = 2.85V		15	25	µA

*1 Pin = 25dBm, 0/2.85V control, V_{DD} = 2.85V, 1920 to 1980MHz

*2 Pin = 25dBm, 0/2.85V control, V_{DD} = 2.85V, 900MHz

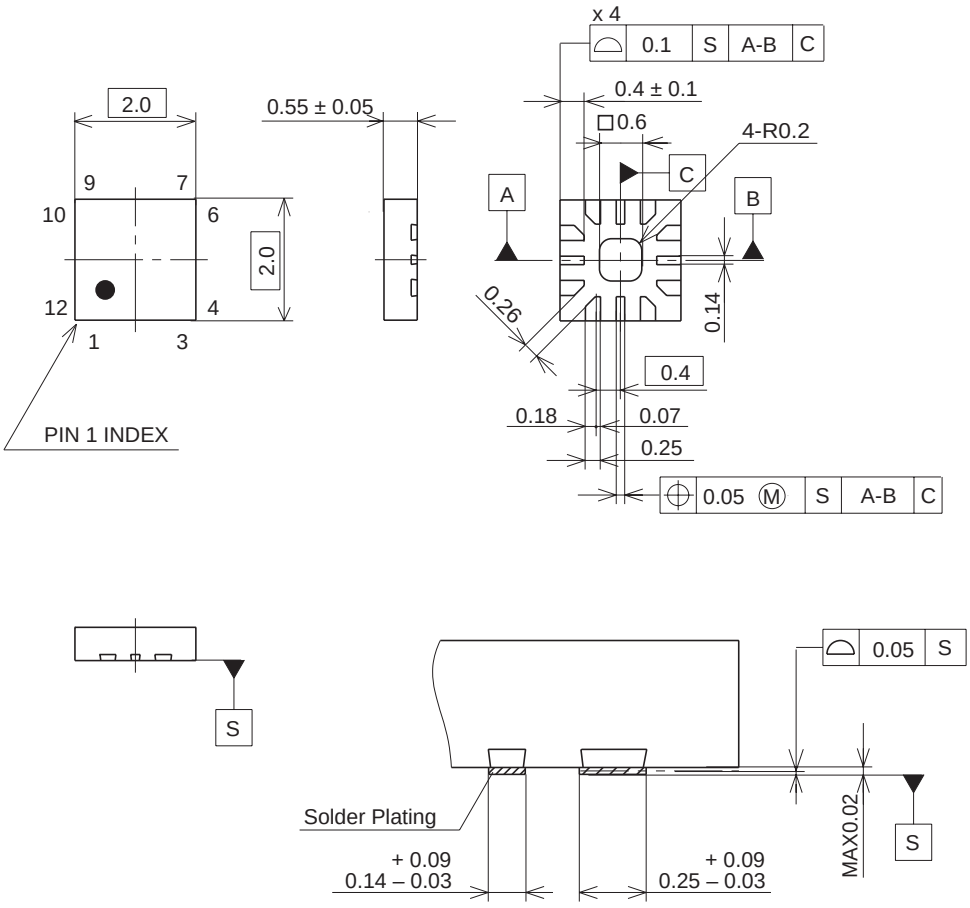
*3 Pin = 25dBm (900MHz) + 25dBm (901MHz), 0/2.85V control, V_{DD} = 2.85V

Pin Description

Pin No.	Symbol	Description
2	RF1	RF input/output. Connect capacitor (recommended value: 100pF) in use
4	RF2	RF input/output. Connect capacitor (recommended value: 100pF) in use
6	RF3	RF input/output. Connect capacitor (recommended value: 100pF) in use
8	RF4	RF input/output. Connect capacitor (recommended value: 100pF) in use
10	V_{DD}	DC power supply
12	CTL	Logic control
1, 3, 5, 7, 9, 11	GND	GND

Package Outline Unit: mm

12PIN UQFN (PLASTIC)



TERMINAL SECTION

Note:Cutting burr of lead are 0.05mm MAX.

SONY CODE	UQFN-12P-01
EIAJ CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.01g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm