National Semiconductor

DM77S401/DM87S401, DM77S402/DM87S402 First-In, First-Out (FiFo) 64 x 4, 64 x 5 Serial Memories

General Description

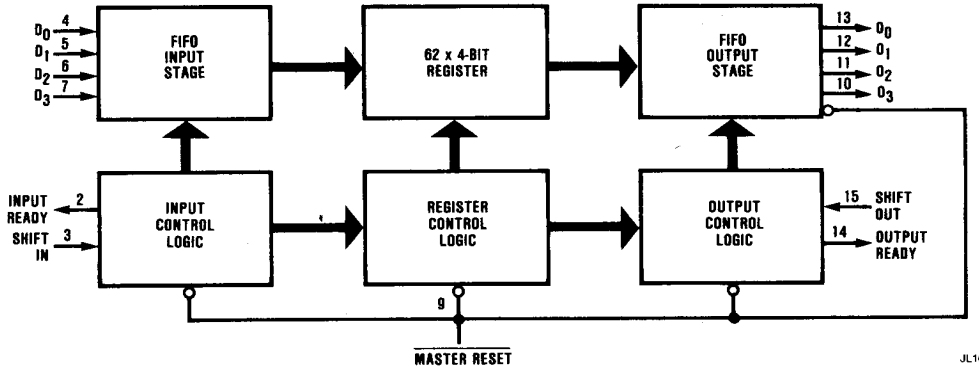
The DM77S401 is an expandable "fall-through" type high-speed First-in, First-out (FiFo) memory organized in 64-word by 4-bit, and 64-word by 5-bit structures respectively. A 10 MHz data rate allows usage in high-speed disc or tape controllers as well as PCM and communications buffer applications.

Features

- 10 MHz shift in, shift out
- TTL inputs and outputs
- Inputs and outputs are symmetrically placed on package
- Easily expandable word and bit dimensions
- Either synchronous or asynchronous operation
- Fairchild F3341 MOS FiFo pin compatible but many times faster!
- Choice of 4-bit or 5-bit data width

Block Diagrams

DM77/DM87S401
64 x 4



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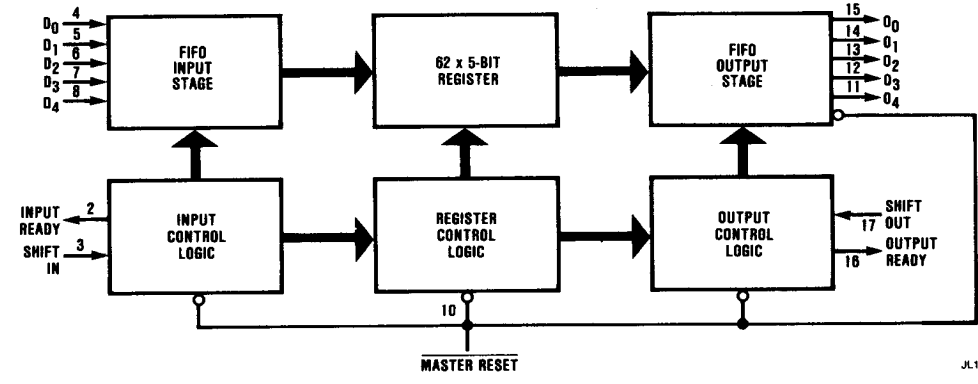
DM77/DM87S402
64 x 5



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Absolute Maximum Ratings

Supply Voltage, V_{CC}	7 Volts
Input Voltage	7 Volts
Off-State Output Voltage	5.5 Volts
Storage Temperature	− 65° to +150° C

Electrical Characteristics Over Operating Conditions DM77/DM87S401; DM77/DM87S402

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IL}	Low-Level Input Voltage					0.8	V
V_{IH}	High-Level Input Voltage			2			V
V_{IC}	Input Clamp Voltage	V_{CC} = Min,	I_I = -18mA			-1.5	V
I_{IL}	Low-Level Input Current D_0-D_4, MR	V_{CC} = Max,	V_I = 0.45V			-0.4	mA
I_{IH}	High-Level Input Current	V_{CC} = Max,	V_I = 2.4V			50	μA
I_I	Maximum Input Current	V_{CC} = Max,	V_I = 5.5V			1.0	mA
V_{OL}	Low-Level Output Voltage	V_{CC} = Min V_{IL} = 0.8V V_{IH} = 2V	I_{OL} = 8mA			0.5	V
V_{OH}	High-Level Output Voltage	V_{CC} = Min V_{IL} = 0.8V V_{IH} = 2V	I_{OH} = -0.9mA	2.4			V
I_{OS}	Output Short-Circuit Current (Note 1)	V_{CC} = Max,	V_O = 0V	-20		-90	mA
I_{CC}	Supply Current	V_{CC} = Max Inputs Low, Outputs Open	DM77S401 DM87S401 DM77S402 DM87S402			190 160 210 180	mA

Operating Conditions

Symbol	Parameter	DM77S401/402			DM87S401/402			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-Air Temperature (Note 2)	-55		+125	0		+75	°C
t_{SIH}	Shift In HIGH Time	45	15		35	15		ns
t_{SIL}	Shift In LOW Time	45	22		35	22		ns
t_{IDS}	Input Data Setup	10	− 9		0	− 9		ns
t_{IDH}	Input Data Hold Time	55	30		45	30		ns
t_{SOH}	Shift Out HIGH Time	45	15		35	15		ns
t_{SOL}	Shift Out LOW Time	45	15		35	15		ns
t_{MRW}	Master Reset Pulse (Note 3)	40	15		35	15		ns
t_{MRS}	Master Reset to SI	45	15		35	15		ns

Note 1: Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
Note 2: Case temperature.
Note 3: Master reset clears all the cells to the empty state, and the data outputs to a LOW state.

Switching Characteristics Over Operating Conditions

Symbol	Parameter	DM77S401/402			DM87S401/402			Units
		Min	Typ	Max	Min	Typ	Max	
f_{IN}	Shift In Rate	7	16		10	16		MHz
t_{IRL}	Shift In to Input Ready LOW		30	60		30	45	ns
t_{IRH}*	Shift In to Input Ready HIGH		33	60		33	45	ns
f_{OUT}	Shift Out Rate	7	16		10	16		MHz
t_{ORL}	Shift Out to Output Ready LOW		40	65		40	55	ns
t_{ORH}**	Shift Out to Output Ready HIGH		45	70		45	60	ns
t_{OD}**	Output Data Delay		38	65		38	55	ns
t_{PT}	Data Throughput or "Fall Through"		1.8	4		1.8	3	μs
t_{MRORL}	Master Reset to OR LOW		30	65		30	60	ns
t_{MRIRH}	Master Reset to IR HIGH		30	65		30	60	ns
t_{IPH}	Input Ready Pulse HIGH	15	22		15	22		ns
t_{OPH}	Output Ready Pulse HIGH	15	22		15	22		ns

*This delay is dependent upon positive pulse width of SI input.

**These delays are dependent upon positive pulse width of SO input.

Functional Description

DATA INPUT

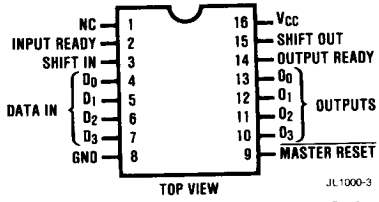
Data is entered in the FiFo on D_0-D_3 (D_0-D_4 on the 402) inputs. If the first location is ready to accept data, the Input Ready (IR) pin will be high. Data then present on the four input pins will be entered to the first location when the Shift In (SI) pin goes high. A high on the SI pin will cause the IR pin to go low. The old data will remain on the first location until SI is brought low again and IR goes low. If SI is brought low before IR goes low, data transfer will not take place until IR goes low. If the FiFo is not full (i.e., all locations contain data), IR will go high, indicating that the first location can accept more data from the four input pins. Simultaneously with IR going high, data will shift to the second location and so forth until it either reaches the output stage or a full location. When the memory is full, IR will remain low and the FiFo will accept no more data.

DATA TRANSFER

Once data is entered into the second location, the transfer of any full location to the downstream adjacent empty location is automatically activated by an on-chip control. Thus data will stack up at the end of the FiFo while empty locations fill to the front. The time required for the first data to travel from input to output locations is called Data Throughput Time or t_{PT}.

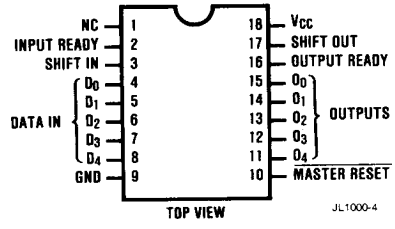
Connection Diagrams

DM77/DM87S401
Dual-In-Line Package



TOP VIEW JL1000-3

DM77/DM87S402
Dual-In-Line Package



TOP VIEW JL1000-4

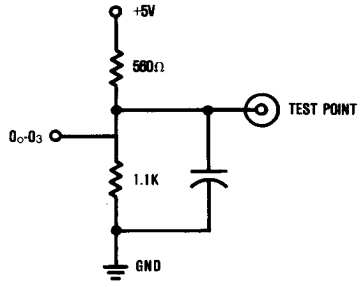
Order Number DM77S401J, DM87S401J, DM77S402J, DM87S402J, DM77S401N, DM87S401N, DM77S402N or DM87S402N
See NS Package J16A or N16A

DATA OUTPUT

- Data is output from Pins O_0-O_3 (O_0-O_4 on the 402). When data is shifted into the output stage, Output Ready (OR) goes high to indicate the presence of valid data. When the OR is high, data may be shifted out of O_0-O_3 by pulling Shift Out (SO) high. A high signal on the SO pin will cause the OR pin to go low. When the SO pin is brought low again, and OR is low, any valid data at the next upstream stage is shifted to the output. Then all valid upstream data moves down one location. New valid data on the output stage will again cause OR to go high unless the output stage is empty (all data shifted out), in which case OR stays low.

  Input Ready (IR) and Output Ready (OR) may also be used as status signals since IR will stay low for at least t_{PT} if the FiFo is full and OR will stay low for at least t_{PT} if the FiFo is empty.

Standard Test Load



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