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Mosaic Semiconductor Inc.

MIXED TECHNOLOGY PUMA

PUMA 2X0211

Issue 1.0 : September 1991

ADVANCE PRODUCT INFORMATION

2,097,152 bit UVEPROM and 131,072 bit SRAM

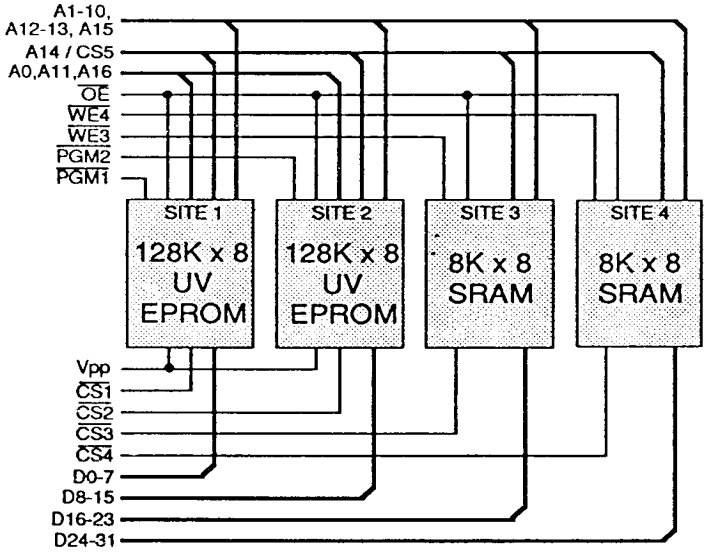
Features

Output user configurable as 8 / 16 bit wide.
Average Power UVEPROM 237 / 396 mW (maximum).
SRAM 429 / 781 mW (maximum).
Standby Power 15 µW (typical).
Power Supply voltage of V_{CC} = 5.0V±5%.
On-board decoupling capacitors.
All Inputs and Outputs TTL Compatible.
May be screened in accordance with MIL-STD-883C.

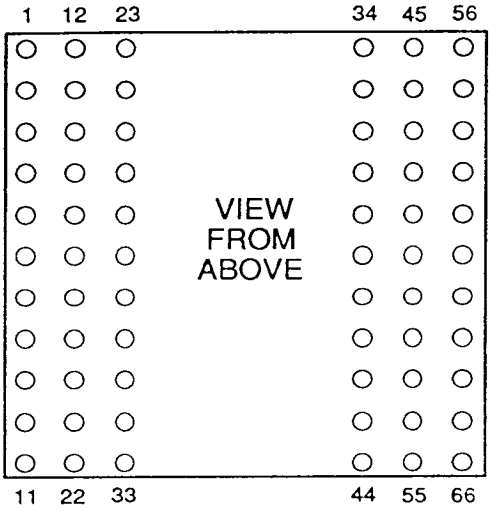
EPROM Data Access times of 90/120/150 ns.
Fast Page Programming of 14 sec (typ).
Programming Voltage of 12.5V±0.3V

SRAM Data Access times of 55/70/85 ns.
Completely static operation.

Block Diagram



Pin Definition

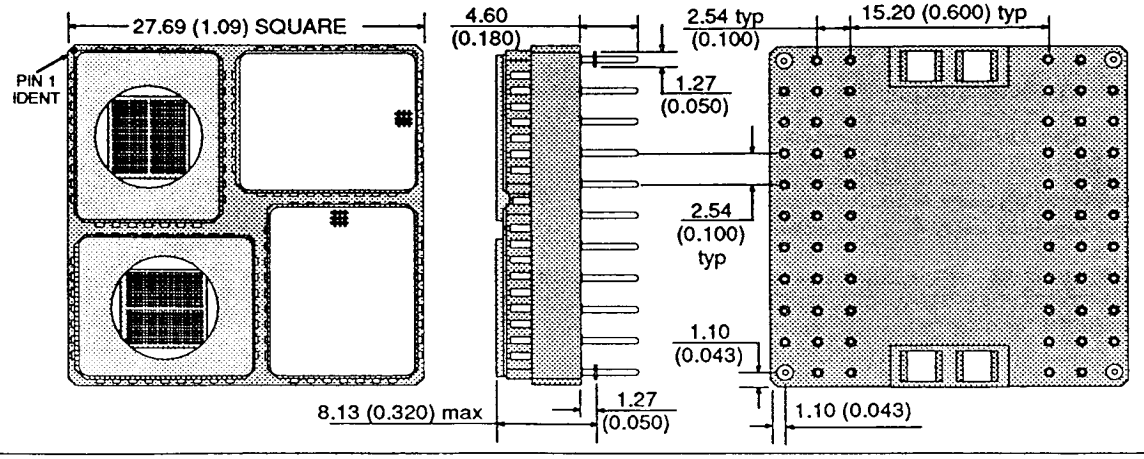


For module pinout see page 2.

Pin Functions

A0-A16	Address Inputs
D0-D31	Data Input/Output
$\overline{CS1\text{-}5}$	Chip Selects
$\overline{OE}$	Output Enable
$\overline{WE3\text{-}4}$	Write Enables
$\overline{PGM1\text{-}2}$	Programming Enables
V_{PP}	Programming Voltage
V_{CC}	Power (+5V)
GND	Ground

Package Details Dimensions in mm (inches).



GENERAL DESCRIPTION AND COMMON PARAMETERS

The PUMA 2X0211 is a mixed memory technology module using 2,097,152 bit UV EPROM and 131,072 bit SRAM. Although intended for use in 16 bit mode, it is configurable as 8 or 16 bit wide output using $\overline{CS1}$-4, allowing flexibility in a wide range of applications.

The operation of the UV EPROMs is obviously different from the operation of the SRAMs. For this reason the technical data which follows is separated into an EPROM section (pages 4 to 9) and a SRAM section (pages 10 to 13), with both 8 and 16 bit modes covered for both types of memory. Note that the DC Characteristics in both sections are for the ***entire*** module, irrespective of whether they are in the EPROM part or the SRAM part.

On this module the UV EPROM devices are controlled by input lines $\overline{CS1}$, $\overline{CS2}$, $\overline{PGM1}$ and $\overline{PGM2}$, while the SRAMs are controlled by lines $\overline{CS3}$, $\overline{CS4}$, $\overline{WE3}$ and $\overline{WE4}$.

The UV EPROMs are byte/page programmable using a fast high reliability programming algorithm, with complete device programming being possible in 14 seconds (in 16 bit mode). Both of these devices are erased by irradiating them with ultra violet light via the window on the top of the LCC packages. Note that normally, in order to automatically match UV EPROM devices to their correct programming algorithm, both manufacturer and device codes are accessible by placing 12.0V onto address line A9. On this mixed memory technology PUMA this is ***not possible***, so the actual device type and relevant codes are given below:

Manufacturer	*Code*	*Device Number*	*Code*
Hitachi	07_H	HN27C101A	38_H

The SRAMs used on the PUMA 2X0211 module are CMOS devices giving high speed access combined with low power consumption. They are fully static in operation, with a reduced power consumption standby mode when disabled.

Connection Table

PGA Pin No.	*Signal Name*	*PGA Pin No.*	*Signal Name*	*PGA Pin No.*	*Signal Name*	*PGA Pin No.*	*Signal Name*	*PGA Pin No.*	*Signal Name*
1	D8	2	D9	3	D10	4	A14/CS5	5	A16/NC
6	A11/NC	7	A0/NC	8	NC	9	D0	10	D1
11	D2	12	$\overline{PGM2}$	13	$\overline{CS2}$	14	GND	15	D11
16	A10	17	A9/A11	18	A15/A12	19	V_{CC}	20	$\overline{CS1}$
21	NC	22	D3	23	D15	24	D14	25	D13
26	D12	27	$\overline{OE}$	28	NC	29	$\overline{PGM1}$	30	D7
31	D6	32	D5	33	D4	34	D24	35	D25
36	D26	37	A7/A6	38	A12/A7	39	V_{PP}	40	A13/A8
41	A8/A9	42	D16	43	D17	44	D18	45	V_{CC}
46	$\overline{CS4}$	47	$\overline{WE4}$	48	D27	49	A4/A3	50	A5/A4
51	A6/A5	52	$\overline{WE3}$	53	$\overline{CS3}$	54	GND	55	D19
56	D31	57	D30	58	D29	59	D28	60	A1/A0
61	A2/A1	62	A3/A2	63	D23	64	D22	65	D21
66	D20								

Note: Some pins in the above table have been allocated two functions. Where this is the case, the functions specified refer to the EPROM pinout and SRAM pinout respectively; for example, pin 41, allocated A8/A9, connects to A8 on the EPROMs, and to A9 on the SRAMs.

Absolute Maximum Ratings (1)

Temperature Under Bias	T_{OPR}	-55 to +125 °C
Storage Temperature	T_{STG}	-65 to +150 °C
Voltage on Any Pin with respect to GND (2)	V_{IN}	-0.6 to +7.0 V
Voltage on V_{PP} pin with respect to GND (3)	V_{PT}	-0.6 to +13.5 V

Notes (1) Stresses above those listed may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) V_{IN} and V_{PT} minimum may be -1.0V for pulse width ≤ 50ns.

Recommended Operating Conditions

			min	*typ*	*max*	
Supply Voltage		V_{CC}	4.75	5.0	6.25	V
Programming Voltage	Read	V_{PPR}	4.75	5.0	5.25	V
	Program	V_{PPW}	12.2	12.5	12.8	V
Input High Voltage	TTL	V_{IH}	2.2	-	V_{CC}+1.0	V
	CMOS	V_{IHC}	0.7 V_{CC}	-	V_{CC}+1.0	V
Input Low Voltage	TTL	V_{IL}	-0.3	-	0.8	V
	CMOS	V_{ILC}	-0.3	-	0.3	V
Operating Temperature		T_A	0	-	70	°C
		T_{AI}	-40	-	85	°C (-I suffix)
		T_{AM}	-55	-	125	°C (-M, MB suffix)

Capacitance (T_A=25°C, f=1MHz) These parameters are calculated, not measured.

Parameter		*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance	A1-10, A12-15, $\overline{OE}$	C_{IN1}	V_{IN}=0V	-	56	pF
	A0, A11, A16	C_{IN2}	V_{IN}=0V	-	40	pF
	$\overline{CS1-2}$, $\overline{PGM1-2}$	C_{IN3}	V_{IN}=0V	-	40	pF
	$\overline{CS3-4}$, $\overline{WE3-4}$	C_{IN4}	V_{IN}=0V	-	36	pF
Output Capacitance	D0-D15	C_{OUT1}	V_{OUT}=0V	-	25	pF
	D16-D31	C_{OUT2}	V_{OUT}=0V	-	18	pF

UV EPROM DATA - READ

DC Electrical Characteristics (T_A = -55°C to +125°C, V_{CC} = 5V ± 5%, V_{PP} = V_{CC})

Parameter		*Symbol*	*Test Condition*	*min*	*typ(2)*	*max*	*Unit*
I/P Leakage Current	A0 -A16, $\overline{OE}$	I_{LI1}	V_{CC} = V_{CC} max, V_{IN} = 0V or V_{CC}, V_{PP} = V_{PPL}	-	-	±6	µA
	$\overline{PGM1\text{-}2}$, $\overline{CS1\text{-}2}$	I_{LI2}	V_{CC} = V_{CC} max, V_{IN} = 0V or V_{CC}	-	-	±4	µA
Output Leakage Current	D0-D15	I_{LO}	V_{CC} = V_{CC} max, V_{OUT} = 0V or V_{CC}	-	-	±2	µA
V_{PP} Leakage Current		I_{PPS}	V_{PP} ≤ V_{CC}	-	2	40	µA
V_{CC} Average Read Current	16 bit	I_{CCO16}	$\overline{CS}$ (1) = V_{IL}, I_{OUT} = 0mA, f = 5MHz	-	-	72	mA
	8 bit	I_{CCO8}	As above	-	-	43	mA
V_{CC} Average Read Current	16 bit	I_{CCA16}	$\overline{CS}$ (1) = V_{IL}, I_{OUT} = 0mA, f = 10MHz	-	-	112	mA
	8 bit	I_{CCA8}	As above	-	-	63	mA
Standby Supply Current	TTL	I_{SB}	$\overline{CS}$ (1) = V_{IH}	-	5	8	mA
	CMOS	I_{SB1}	$\overline{CS}$ (1) = V_{IHC}, V_{ILC} ≥ V_{IN} ≥ V_{IHC}	-	3	240	µA
V_{PP} Voltage During Read		V_{PPL}	Programming is inhibited if V_{PP} = V_{PPL}	5.75	-	5.25	V
Output Low Voltage	D0-D15	V_{OL}	I_{OL} = 2.1mA.	-	-	0.45	V
Output High Voltage	TTL loading	V_{OH1}	I_{OH} = -1.0mA. (D0-D15)	2.4	-	-	V
	CMOS loading	V_{OH2}	I_{OH} = -100µA. (D0-D15)	V_{CC}-0.7	-	-	V

Notes (1) $\overline{CS}$ above are accessed through $\overline{CS1\text{-}2}$. These inputs must be operated simultaneoulsy for 16 bit operation and singly for 8 bit mode.

(2) Typical figures are measured at 25°C and nominal V_{CC}

(3) **CAUTION:** the PUMA 2X0211 must not be removed from or inserted into a socket when V_{CC} or V_{PP} is applied.

(4) During the above operations, $\overline{CS3\text{-}4}$ and $\overline{WE3\text{-}4}$ must be held at a logic high level.

Operating Modes

The Table below shows the logic inputs required to control the operating modes of each EPROM on the PUMA 2X0211.

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{PGM}$	*Vpp*	*Vcc*	*Outputs*
Read	0	0	1	5V	5V	Data out
Output Disable	0	1	1	5V	5V	Floating
Standby	1	X	X	5V	5V	Floating
Program	0	1	0	12.5V	6V	Data in
Program Verify	0	0	1	12.5V	6V	Data out
Page Data Latch	1	0	1	12.5V	6V	Data in
Page Program	1	1	0	12.5V	6V	Floating
Program Inhibit	0	0	0	12.5V	6V	Floating
	0	1	1	12.5V	6V	
	1	0	0	12.5V	6V	
	1	1	1	12.5V	6V	

Note: In this table, $\overline{CS}$ is accessed through $\overline{CS1}$ and $\overline{CS2}$. $\overline{CS3}$ and $\overline{CS4}$ are both held high throughout all modes.

Also, where TTL or CMOS levels are applied they are used on all $\overline{CS}$s at the same time i.e.

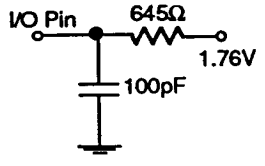
if $\overline{CS1,2}$ = V_{IL} then $\overline{CS3,4}$ = V_{IH}

1 = V_{IH}
0 = V_{IL}
X = Don't Care

AC Test Conditions

* Input pulse levels: 0V to 3.0V.
* Input and Output timing reference levels: 1.5V
* Input rise and fall times: ≤ 10ns.
* Output load : see diagram
* Module is tested in 8 bit mode.

Output Load

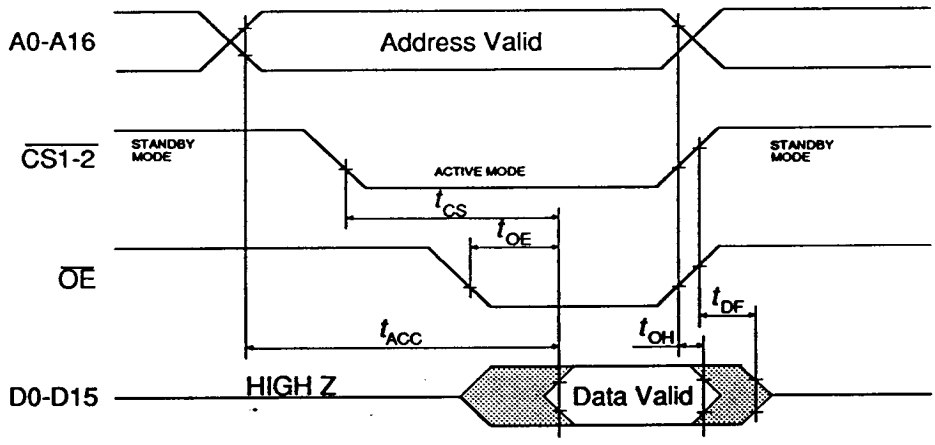


AC Characteristics

Parameter	Symbol	-90 min	-90 max	-12 min	-12 max	-15 min	-15 max	Unit
Address to Output Delay	t_{ACC}	-	90	-	120	-	150	ns
Chip Select to Output Delay	t_{CS}	-	90	-	120	-	150	ns
Output Enable to Output Delay	t_{OE}	-	60	-	60	-	70	ns
$\overline{OE}$ or $\overline{CS}$ High to Output Float (1)	t_{DF}	0	50	0	50	0	60	ns
Output Hold from Address, $\overline{CS}$ or $\overline{OE}$	t_{OH}	0	-	0	-	0	-	ns

Notes: (1) t_{DFZ} is defined as the time at which the outputs achieve the open circuit conditions and is not referenced to output voltage levels. This parameter is sampled and not 100% tested.

Read Cycle Timing Waveform



UV EPROM DATA - PROGRAM (Note : The following information is provided for design purposes only.)

DC Electrical Characteristics (T_A = 25°C ± 5°C, V_{CC} = 6.0V ± 0.25, V_{PP} = 12.5V ± 0.3V)

Parameter		*Symbol*	*Test Condition*	*min*	*typ*[2]	*max*	*Unit*
I/P Leakage Current	A0 -A16, $\overline{OE}$	I_{LI1}	$V_{CC} = V_{CC}$ max, V_{IN} = 0V or V_{CC}, $V_{PP} = V_{PPL}$	-	-	±6	µA
	$\overline{PGM1\text{-}2}$, $\overline{CS1\text{-}2}$	I_{LI2}	$V_{CC} = V_{CC}$ max, V_{IN} = 0V or V_{CC}	-	-	±4	µA
Output Leakage Current	D0-D15	I_{LO}	$V_{CC} = V_{CC}$ max, V_{OUT} = 0V or V_{CC}	-	-	±2	µA
V_{CC} Program Current	16 bit	I_{CCP16}	$\overline{CS}$ [1] = $\overline{PGM}$ [1] = V_{IL}, Program in progress	-	-	72	mA
	8 bit	I_{CCP8}	As above	-	-	43	mA
V_{PP} Byte Program Current	16 bit	I_{PPB16}	$V_{PP} = V_{PPH}$, Byte Program in progress	-	-	80	mA
	8 bit	I_{PPB8}	As above	-	-	40	mA
V_{PP} Page Program Current	16 bit	I_{PPP16}	$V_{PP} = V_{PPH}$, Page Program in progress	-	-	100	mA
	8 bit	I_{PPP8}	As above	-	-	50	mA
V_{CC} Voltage During Program		V_{CCP}		5.75	6.0	6.25	V
V_{PP} Voltage During Program		V_{PPH}		12.2	12.5	12.8	V
Output Low Voltage	D0-D15	V_{OLV}	I_{OL} = 2.1mA, Verify in progress	-	-	0.45	V
Output High Voltage	D0-D15	V_{OHV}	I_{OH} = -400µA, Verify in progress	2.4	-	-	V

Notes (1) $\overline{CS}$ and $\overline{PGM}$ above are accessed through $\overline{CS1\text{-}2}$ and $\overline{PGM1\text{-}2}$ respectively.
(2) Typical figures are measured at 25°C and nominal V_{CC}
(3) Maximum program current is the sum of I_{CC} and I_{PP}.
(4) **CAUTION**: the PUMA 2X0211 must not be removed from or inserted into a socket when V_{CC} or V_{PP} is applied.
(5) During the above operations, $\overline{CS3\text{-}4}$ and $\overline{WE3\text{-}4}$ must be held at a logic high level.

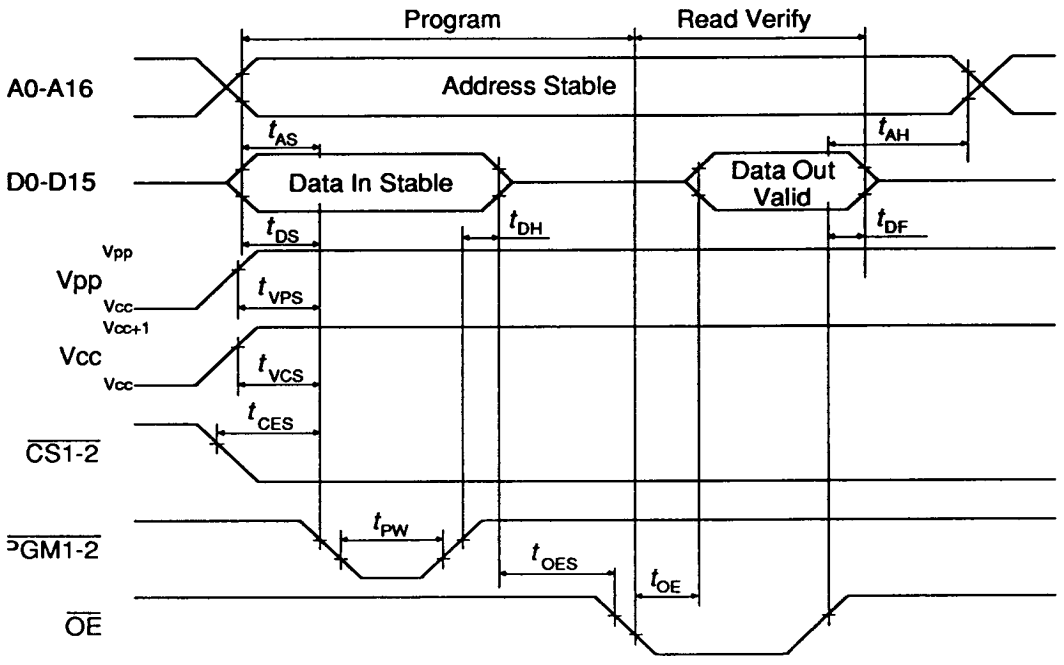
AC Characteristics

Parameter	*Symbol*	*min*	*typ*	*max*	*Unit*
Address Setup Time	t_{AS}	2	-	-	µs
Output Enable Setup Time	t_{OES}	2	-	-	µs
Output Enable Hold Time	t_{OEH}	2	-	-	µs
Data Setup Time	t_{DS}	2	-	-	µs
Address Hold Time	t_{AH}	0	-	-	µs
	t_{AHL}	2	-	-	µs
Data Hold Time	t_{DH}	2	-	-	µs
Output Enable High to Output Float Delay [1]	t_{DF}	0	-	130	ns
V_{PP} Setup Time	t_{VPS}	2	-	-	µs
V_{CC} Setup Time	t_{VCS}	2	-	-	µs
Program Initial Program Pulse Width [2]	t_{PW}	0.19	0.2	0.21	ms
Program Overprogram Pulse Width [3]	t_{OPW}	0.19	-	5.25	ms
Data Valid from Output Enable	t_{OE}	0	-	150	ns
Program Setup Time	t_{PGMS}	2	-	-	µs
Chip Select Setup Time	t_{CES}	2	-	-	µs
Chip Select Hold Time	t_{CSH}	2	-	-	µs
Output Enable Pulse Width during Data Latch	t_{LW}	1	-	-	µs

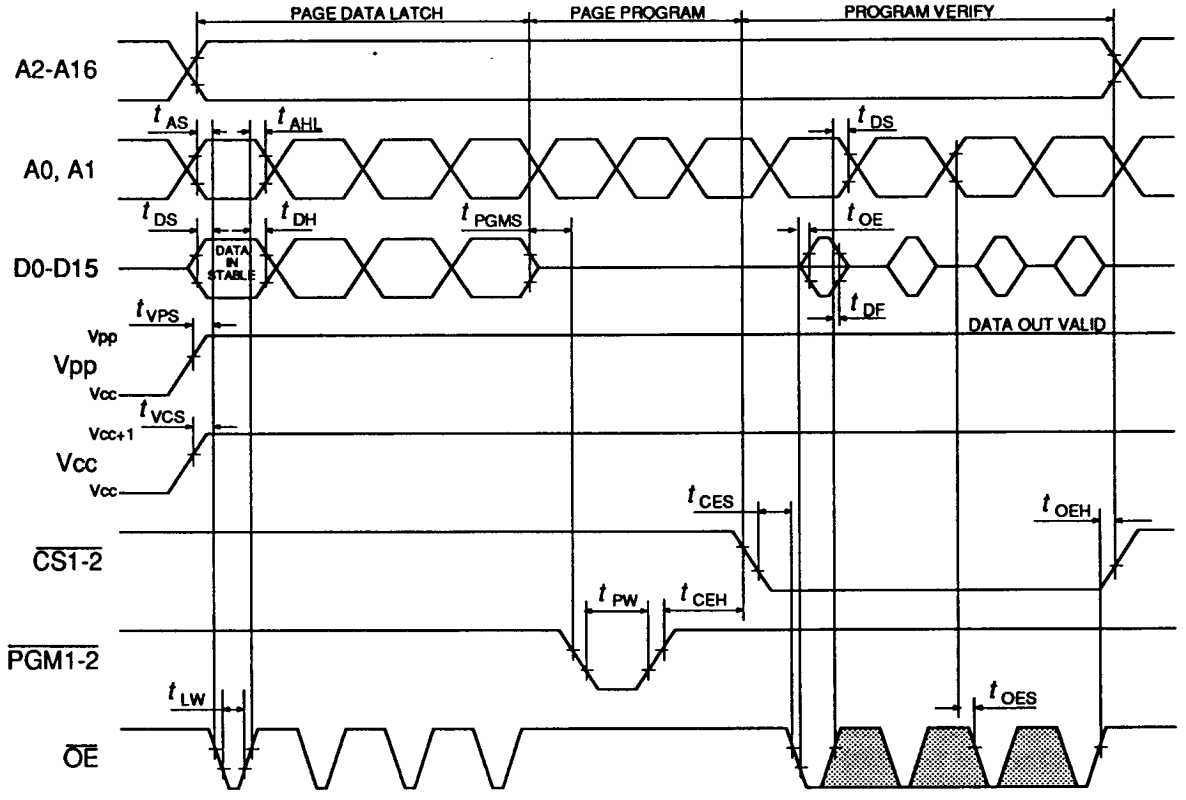
Notes (1) Defines the time at which the output achieves the open circuit condition and is no longer driven.
(2) The value of this pulse is 0.2 ms ± 5%.
(3) Length of this pulse may vary as a function of the iteration counter value n.

Programming Cycle Timing Waveforms

Single Byte Programming



Page Mode Programming

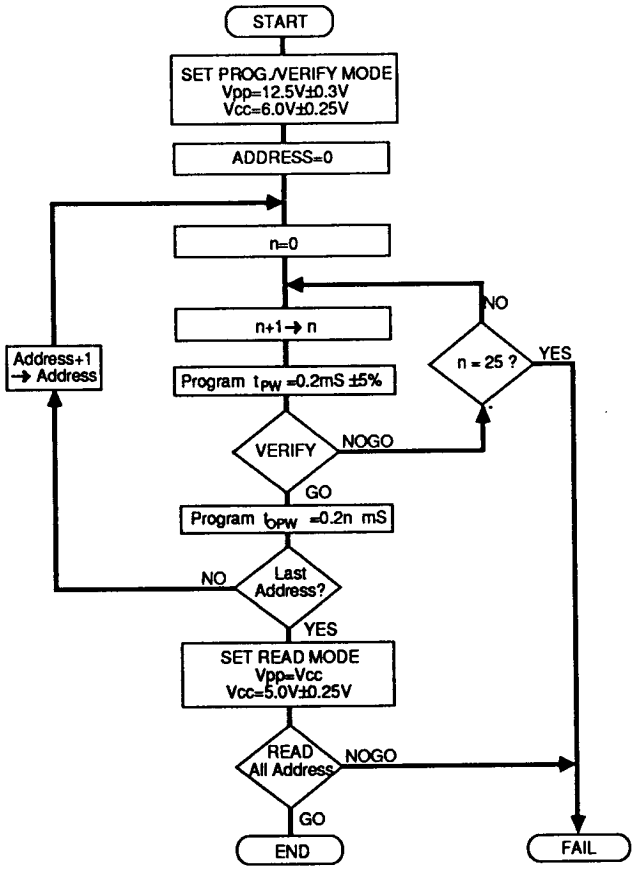


High Performance Programming Algorithm

The PUMA 2X0211 can be programmed using either of the algorithms shown below. These allow faster programming times without stressing the device or causing deterioration in Data Retention Time. Two methods are described here, Single Byte and Page Mode; see the Truth Table on page 3 for selection of these modes.

Single Byte

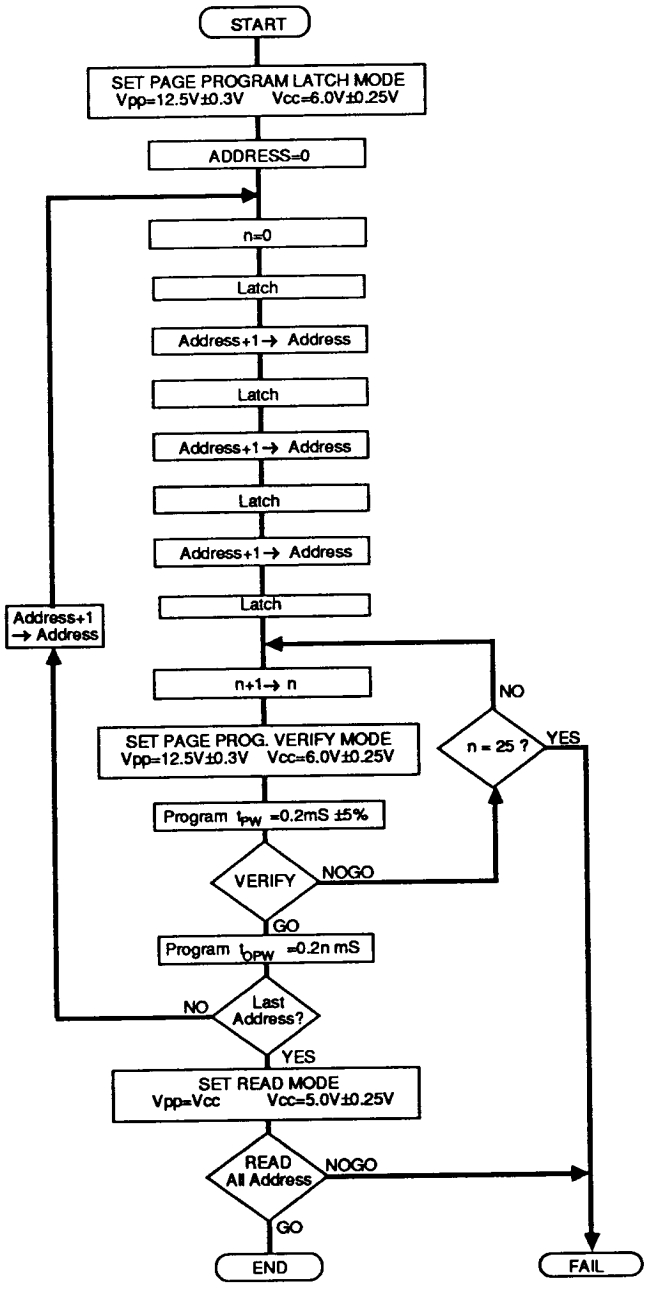
When the Program logic conditions are satisfied, the location is designated by A0 - A16, and the data to be programmed is applied 8 bits in parallel on D0 - D7. In this state, Byte programming is completed when PGM is at a low level.



NOTE: THE ALGORITHM SHOWN HERE MUST BE USED TO ENSURE CORRECT PROGRAMMING OF THE PUMA 2X0211. THIS MAXIMIZES THE DATA RETENTION TIME OF THE DEVICE AND DOES NOT STRESS THE MEMORY CELLS.

Page Mode

Page Mode allows 4 bytes of data to be simultaneously programmed. The destination address for a Page Programming operation must reside on the same page i.e. A2 - A16 must not change. When the logic conditions in the Truth Table are satisfied, Page Mode Programming is activated. The four locations in the same page are designated by A0 - A1, and the data is applied in parallel on D0 - D7. In this state the data latch (4 bytes) is completed, and the data is programmed when OE is high. Programming is completed when PGM is low.



PROGRAMMING NOTES

Upon delivery, or after each erasure, the PUMA 2X0211 has all 1,048,576 bits in the ONE or HIGH state. ZEROs are loaded into the devices through the procedure of programming.

This mode is entered when 12.5V±0.3V is applied to the V_{PP} pin, $\overline{CS1\text{-}2}$ and $\overline{PGM1\text{-}2}$ are at V_{IL} and $\overline{OE}$ is at V_{IH}, as shown on the Table on page 2.

The algorithms reduce programming time by using 200µs pulses followed by byte verification to determine if the byte has been successfully programmed. If the data does not verify, up to 25 such pulses (n) can be applied, after which, if verification fails, programming stops. This process is repeated for each memory location within the PUMA 2X0211. After successful programming each memory location is given an overprogram pulse of n times 0.2 ms duration to ensure that all bits have an adequate margin.

The algorithms program at V_{CC}=6.0V in order to ensure that each EPROM bit is programmed to a sufficiently high threshold voltage. After programming is complete, all bytes are compared with the original data with V_{CC}=5.0V±5%.

In order to overcome the voltage drop caused by the inductive effects of the printed circuit board on which the PUMA 2X0211 is used, it is recommended that a 4.7µF electrolytic capacitor is used between V_{CC} and GND for every two devices. This capacitor should be placed close to the point where the power supply is routed to the UV EPROM array.

ERASE

Complete erasure of the PUMA 2X0211 is performed by exposure to an ultraviolet light source giving a dosage of 15WS/cm². This dosage can be obtained by using an ultraviolet lamp with a wavelength of 2537 Å at a minimum intensity of 12,000µW/cm², for approximately 15 - 20 minutes. The PUMA 2X0211 should be directly under and about 1 inch from the light source.

Note that sunlight and fluorescent light may contain sufficient ultraviolet light to erase the programmed information. Although erasure times will be much longer at these levels, the transparent lids on this module should be covered with an opaque label to realise maximum system reliability.

SRAM DATA

DC Electrical Characteristics (V_{CC}=5V±10%,T_A=-55°C to +125°C)

Parameter		*Symbol*	*Test Condition*	*min*	*typ*(1)	*max*	*Unit*
I/P Leakage Current	A0-A12,CS5, $\overline{OE}$	I_{LI1}	V_{IN} = 0V to V_{CC}	-	-	±6	µA
	$\overline{WE3\text{-}4}$, $\overline{CS3\text{-}4}$	I_{LI2}	As above	-	-	±1	µA
Output Leakage Current	D16-D31	I_{LO}	$\overline{CS}$(2) = V_{IH} or $\overline{CS5}$ = OE = V_{IH}	-	-	±1	µA
Average Supply Current	16 bit	I_{CCA16}	$\overline{CS}$(2) = V_{IL}, CS5 = V_{IH}, minimum cycle	-	82	142	mA
	8 bit	I_{CCA8}	As above	-	45	78	mA
Standby Supply Current	TTL levels	I_{SB1}	$\overline{CS}$(2) = V_{IH} or CS5 = V_{IL}	-	5	8	mA
	CMOS levels	I_{SB2}	$\overline{CS}$(2) ≥ V_{IHC}, CS5 ≤ V_{ILC}, V_{ILC} ≥ V_{IN} ≥ V_{IHC}	-	3	240	µA
Output Voltage Low	D16-D31	V_{OL}	I_{OL} = 4.0 mA	-	-	0.4	V
Output Voltage High	D16-D31	V_{OH}	I_{OH} = - 1.0 mA	2.4	-	-	V

Notes: (1) Typical values are at V_{CC}=5.0V,T_A=25°C and specified loading.

(2) $\overline{CS}$ above is accessed through $\overline{CS3\text{-}4}$. These inputs must be operated simultaneously for 16 bit mode and singly for 8 bit mode.

(3) **CAUTION:** the PUMA 2X0211 must not be removed from or inserted into a socket when V_{CC} or V_{PP} is applied.

(4) During the above operation, $\overline{CS1\text{-}2}$ and $\overline{WE1\text{-}2}$ must be held at a logic high level.

Operating Modes

This Table shows the inputs required to control the operating modes of the SRAMs on the PUMA 2X0211 and shows the SRAMs operating in 16 bit mode. If 8 bit operation is required, $\overline{CS3\text{-}4}$, CS5 and $\overline{WE3\text{-}4}$ are controlled independently.

Note that during 16 bit operation, $\overline{CS1\text{-}2}$ and $\overline{WE1\text{-}2}$, which control the EPROM devices on the PUMA 2X0211, must be at a high level. Additionally, where TTL or CMOS levels are applied they are used on all Chip Selects simultaneously i.e.

if $\overline{CS3,4}$ = V_{IL} then $\overline{CS1,2}$ = V_{IH}

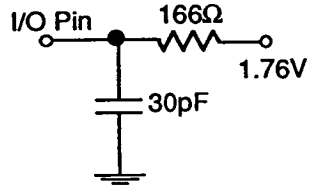
MODE	CS5	$\overline{CS3,4}$	$\overline{OE}$	$\overline{WE3,4}$	Outputs	Ref. Cycle
Standby	0	X	X	X	High Z	
Standby	X	1	X	X	High Z	
Read	1	0	0	1	D_{OUT}	Read Cycle 1, 2
Write	1	0	1	0	D_{IN}	Write Cycle 1
Write	1	0	0	0	D_{IN}	Write Cycle 2
Output Disable	1	0	1	1	High Z	

1 = V_{IH} 0 = V_{IL} X = V_{IL} or V_{IH}

AC Test Conditions

* Input pulse levels: 0.45V to 2.4V.
* Input and Output timing reference levels: 0.8V and 2.0V
* Input rise and fall times: ≤ 10ns.
* Output load : see diagram
* Module is tested in 16 bit mode.

Output Load

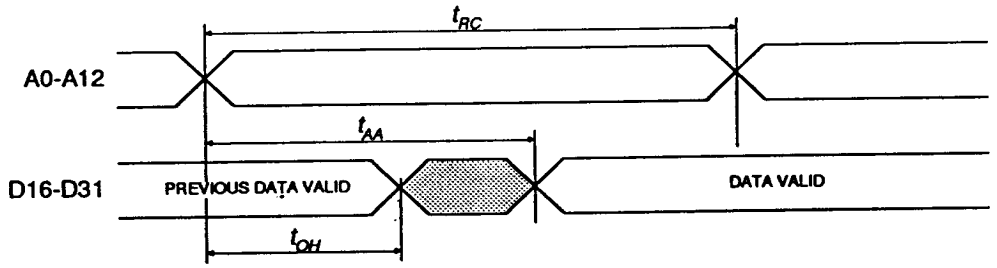


Electrical Characteristics & Recommended AC Operating Conditions

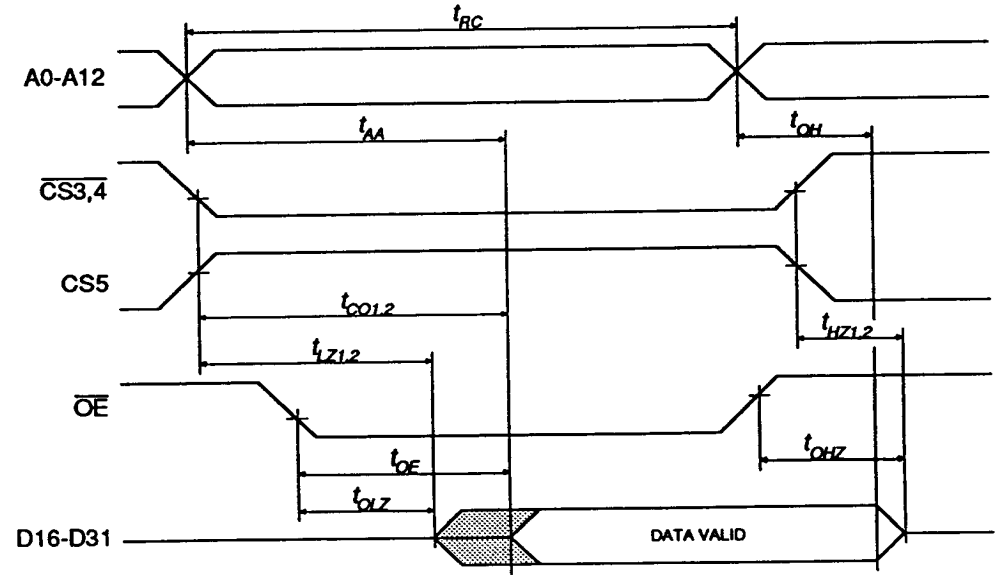
Read Cycle

Parameter	Symbol	-55 min	-55 max	-70 min	-70 max	-85 min	-85 max	Unit
Read Cycle Time	t_{RC}	55	-	70	-	70	-	ns
Address Access Time	t_{AA}	-	55	-	70	-	70	ns
Chip Selection to Output ($\overline{CS3,4}$)	t_{CO1}	-	55	-	70	-	70	ns
Chip Selection to Output (CS5)	t_{CO2}	-	55	-	70	-	70	ns
Output Enable to Output Valid	t_{OE}	-	30	-	35	-	35	ns
Output Hold from Address Change	t_{OH}	10	-	10	-	10	-	ns
Chip Selection to Output in Low Z ($\overline{CS3,4}$)	t_{LZ1}	5	-	5	-	5	-	ns
Chip Selection to Output in Low Z (CS5)	t_{LZ2}	5	-	5	-	5	-	ns
Output Enable to Output in Low Z	t_{OLZ}	0	-	0	-	0	-	ns
Chip Deselection to Output in High Z ($\overline{CS3,4}$)	t_{HZ1}	-	30	0	30	0	30	ns
Chip Deselection to Output in High Z (CS5)	t_{HZ2}	0	30	0	30	0	30	ns
Output Enable to Output in High Z	t_{OHZ}	-	30	-	30	-	30	ns

Read Cycle 1 Timing Waveform (1) (2) (4) (5) (9)



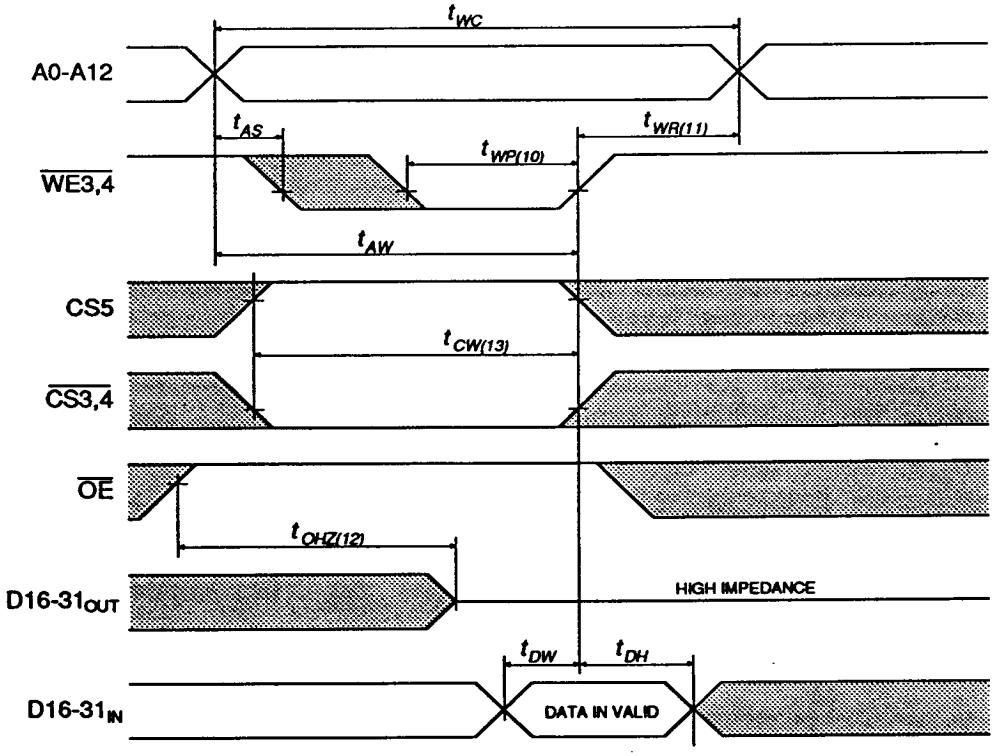
Read Cycle 2 Timing Waveform (1) (2) (3) (4) (5) (6) (7) (8)



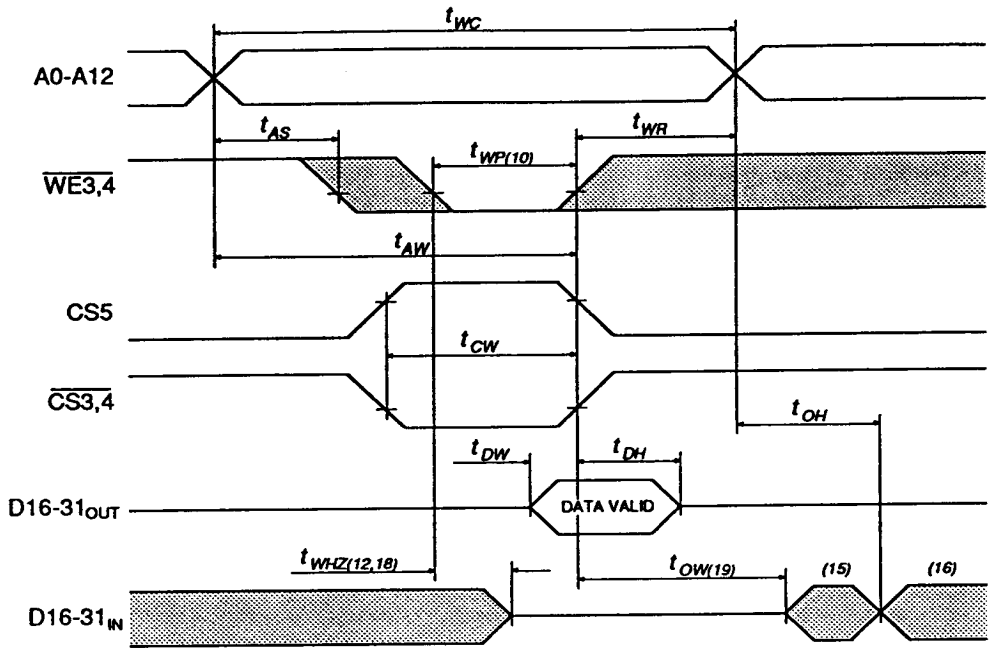
Write Cycle

Parameter	Symbol	-55 min	-55 max	-70 min	-70 max	-85 min	-85 max	Unit
Write Cycle Time	t_{WC}	55	-	70	-	70	-	ns
Chip Selection to End of Write	t_{CW}	50	-	65	-	65	-	ns
Address Valid to End of Write	t_{AW}	50	-	65	-	65	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	30	-	35	-	35	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
End of Write to Output in Low Z	t_{OW}	5	-	5	-	5	-	ns
Write to Output in High Z	t_{WHZ}	-	20	-	25	-	25	ns
Data to Write Time Overlap	t_{DW}	25	-	30	-	30	-	ns
Data Hold from Write Time	t_{DH}	5	-	5	-	5	-	ns

Write Cycle 1 Timing Waveform : $\overline{WE}$ Controlled



Write Cycle 2 Timing Waveform : $\overline{CS}$ Controlled



AC Write Characteristics Notes

(1) During a Read Cycle, $\overline{WE3,4}$ should be high.

(2) Device is enabled when $\overline{CS3,4}$ are low and CS5 is high.

(3) All address lines are valid prior to or coincident with the $\overline{CS3,4}$ going low and CS5 going high.

(4) $\overline{OE}$ is low.

(5) Address inputs may be floating.

(6) The parameters $t_{LZ1,2}$ and $t_{CO1,2}$ are measured from whichever occurs last, $\overline{CS3,4}$ low or CS5 high; $t_{HZ1,2}$ are measured from whichever occurs first, $\overline{CS3,4}$ high or CS5 low.

(7) Transition is measured ±200mV from steady state voltage for $t_{LZ1,2}$, t_{OLZ}, t_{OHZ} and $t_{HZ1,2}$ with specified loading.

(8) The parameters $t_{LZ1,2}$, t_{OLZ}, t_{OHZ} and $t_{HZ1,2}$ are sampled and not 100% tested.

(9) If D_{OUT} in two consecutive Read Cycles is the same, D_{OUT} remains stable.

(10) A Write occurs when $\overline{CS3,4}$, CS5 and $\overline{WE3,4}$ are all active at the same time.
A Write begins at the latest transition among $\overline{CS3,4}$ going low, CS5 going high and $\overline{WE3,4}$ going low.
A Write ends at the earliest transition among $\overline{CS3,4}$ going high, CS5 going low and $\overline{WE3,4}$ going high.
t_{WP} is measured from the beginning of Write to the end of Write.

(11) The parameter t_{WR} is measured from whichever occurs first, $\overline{CS3,4}$ high, $\overline{WE3,4}$ high or CS5 low, to the address change.

(12) During this time, I/O pins are in the output state, so input signals in opposite phase to the output signals must not be applied to them.

(13) If the $\overline{CS3,4}$ or CS5 transition occurs simultaneously to or after the $\overline{WE3,4}$ low transition, the outputs remain in a high impedance state.

(14) $\overline{OE}$ is continuously low.

(15) D_{OUT} is in the same phase as the Write data of this Write Cycle.

(16) D_{OUT} is the Read data of the next address.

(17) If $\overline{CS3,4}$ are low and CS5 is high and I/O pins are in the output state during this period, then input data signals of opposite phase to the outputs must not be applied to the I/O pins.

(18) The parameters t_{WHZ} and t_{OW} are sampled and not 100% tested.

Military Screening Procedure

Module Screening Flow for high reliability product is in accordance with MIL-STD-883C is shown below

MB MODULE SCREENING FLOW		
SCREEN	*TEST METHOD*	*LEVEL*
Visual and Mechanical		
External visual	2017 Condition B (or manufacturers equivalent)	100%
Temperature cycle	1010 Condition C (10 Cycles,-65°C to +150°C)	100%
Burn-In		
Pre Burn-in Electrical	Per Applicable device Specifications at T_A = +25°C (optional)	100%
Burn-In	Method 1015, Condition D, T_A = +125°C	100%
Final Electrical Tests	Per applicable Device Specification	
Static (dc)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (ac)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Percent Defective Allowable (PDA)	Calculated at Post Burn-in at T_A=+25°C	10%
Quality Conformance	Per applicable Device Specification	Sample
External Visual	2009 Per HMP or customer specification	

Ordering Information

PUMA 2X0211MB-9055

- SRAM Speed: 55 = 55 ns; 70 = 70 ns; 85 = 85 ns
- EPROM Speed: 90 = 90 ns; 12 = 120 ns; 15 = 150 ns
- Temperature range: Blank = Commercial Temperature Range. I = Industrial Temperature Range. M = Military Temperature Range. MB = Screened in accordance with MIL-STD-883C
- Organization: X0211 = 128K x 16 EPROM on sites 1 and 2, 8K x 16 SRAM on sites 3 and 4 (both user configurable as x8 outputs)
- Module Type: PUMA 2 = Ceramic 66 Pin Grid Array

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