SKY13267-321, SKY13267-321LF GaAs T/R Diversity Switch LF–6 GHz

Applications

• 802.11a/b/g transmit/receive diversity switch

Features

• Broadband: LF–6 GHz
• Very low insertion loss: 0.8 dB typ. @ 5.2 GHz
• $P_{1\ dB}$: +30 dBm typical @ 3 V
• Low distortion: IP3 +44 dBm typical @ 3 V
• Low current consumption: < 15 µA @ 3 V
• Miniature QFN-12 package

Figure 1. Functional Block Diagram

Description

The SKY13267-321 is a monolithic DPDT switch fabricated using Skyworks Solutions' proprietary GaAs PHEMTs as the switching elements. This wideband switch operates with RF signals from LF–6 GHz. The RF signal paths within the SKY13267-321 are fully bilateral.

Switching is controlled via two control voltage inputs, which are compatible with CMOS logic levels. Depending upon the logic voltage level applied to the control voltage pins, the TX input pin is connected to one of two antenna ports (ANT1 or ANT2) via a low insertion loss path, while the path between the RX pin is connected to the other antenna port. When the control voltages are toggled, the connections between the TX input and RX output pins and the antenna ports are toggled as well.

DC power consumption is very low, 15 µA maximum with control voltage of 5 V. The switch can operate over the temperature range of -40 °C to 85 °C.

This part is available in a lead (Pb)-free package as part number SKY13267-321LF.

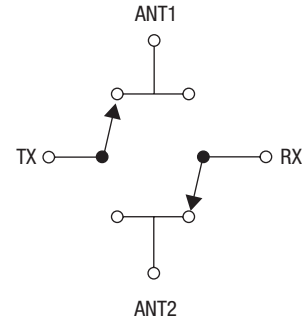An evaluation board is available upon request.

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NEW Skyworks offers lead (Pb)-free "environmentally friendly" packaging that is RoHS compliant (European Parliament for the Restriction of Hazardous Substances).

Table 1. Electrical Specifications (V$_{CTL}$ = 0 V/3V, T = 25 °C, P$_{INPUT}$ = 0 dBm, Z$_0$ = 50 Ω, unless otherwise noted)

Parameter	Condition	Frequency	Min.	Typ.	Max.	Unit
Insertion loss	ANT1, ANT2 to TX, RX ports	2.400–2.500 GHz		07	1.0	dB
		5.150–5.350 GHz		0.8	1.1	dB
		5.725–5.825 GHz		0.9	1.2	dB
Isolation	ANT1, ANT2 to TX, RX ports	2.400–2.500 GHz	30	32		dB
		5.150–5.350 GHz	23	25		dB
		5.725–5.825 GHz	21	23		dB
	ANT1 to ANT2, TX to RX ports	2.400–2.500 GHz		23		dB
		5.150–5.350 GHz		20		dB
		5.725–5.825 GHz		20		dB
Return loss	ANT1, ANT2 to TX, RX ports	2.400–2.500 GHz		22		dB
		5.150–5.350 GHz		19		dB
		5.725–5.825 GHz		17		dB

Table 2. Operating Characteristics (V$_{CTL}$ = 0 V/3V, T = 25 °C, P$_{INPUT}$ = 0 dBm, Z$_0$ = 50 Ω, unless otherwise noted)

Parameter	Condition	Frequency	Min.	Typ.	Max.	Unit
Switching characteristics Rise, fall On, off Video feedthru	10/90% or 90/10% RF 50% V$_{CTL}$ to 90/10% RF Pulse rise time = 1 ns, Measurement BW = 500 MHz			20 40 50		ns ns mV
Error vector magnitude	802.11a, OFDM, 64 QAM, 54 MBPS, P$_{IN}$ ≤ 27 dBm	5.8 GHz		≤1		%
Input third order intermodulation intercept	For two input tones. +15 dBm each tone, 5 MHz spacing, V$_{HIGH}$ = 3 V	2.4 GHz 5.2 GHz		49 44		dBm dBm
Thermal resistance				25		°C/W
Control voltage	V$_{LOW}$ = 0 V @ 10 µA max. V$_{HIGH}$ = 3 V to 5 V @ 15 µA max.					

Table 3. Absolute Maximum Ratings

Characteristic	Value
Control voltage range	-0.2 ≤ V$_C$ ≤ 8 V
RF input power @ 0/3V RF input power @ 0/5V	32 dBm 34 dBm
Storage temperature range	-65 °C to +150 °C
Operating temperature range	-40 °C to +85 °C

Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum specifications. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

CAUTION: *Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.*

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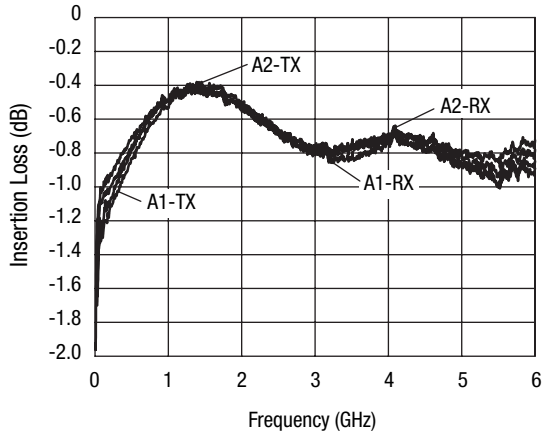
Typical Performance Data
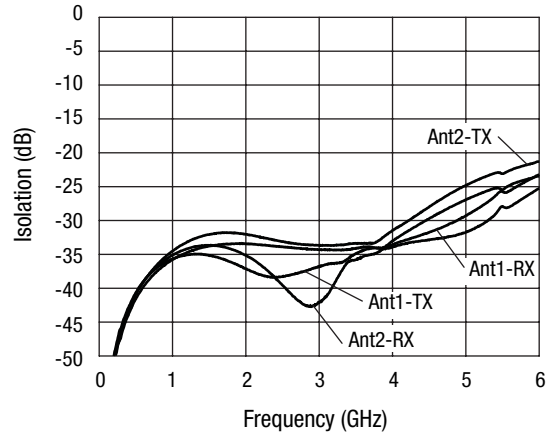
Figure 2. Insertion Loss vs. Frequency

Figure 3. Isolation vs. Frequency
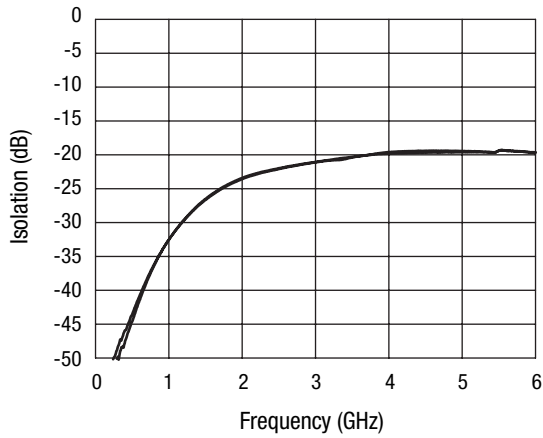
Figure 4. Isolation, TX - RX/ANT1 - ANT2 vs. Frequency

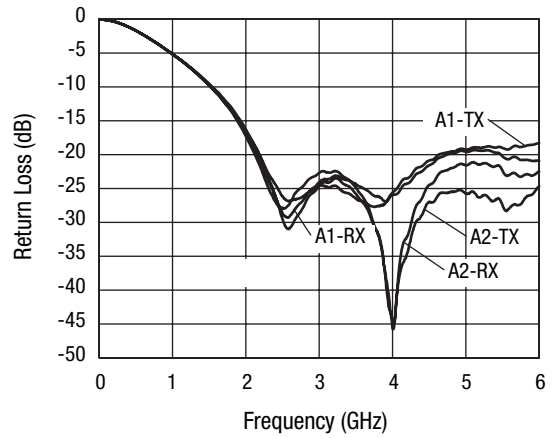Figure 5. Return Loss vs. Frequency

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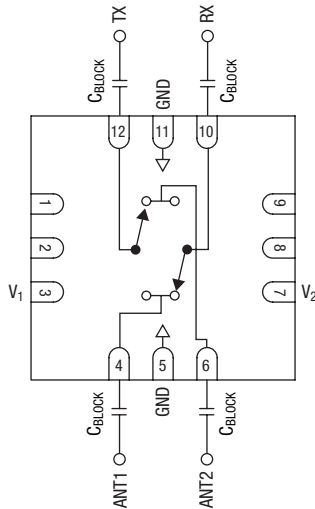
C_{BLOCK} = 4.7 pF

Figure 6. Pin Out Top View
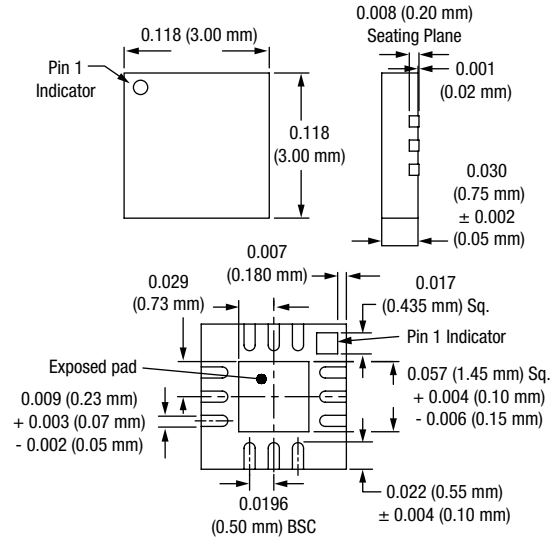
Figure 7. QFN-12 Package Outline

Table 4. Truth Table[1]

V_1	V_2	Low Insertion Loss Paths
V_{LOW}	V_{HIGH}	ANT1 - T_X, ANT2 - R_X
V_{HIGH}	V_{LOW}	ANT2 - T_X, ANT1 - R_X
V_{LOW}	V_{LOW}	Not allowed
V_{HIGH}	V_{HIGH}	Not allowed

1. 3 V $\leq V_{HIGH} \leq$ 5 V , 0 $\leq V_{LOW} \leq$ 0.2 V.

Table 5. Pin Descriptions

Pin Number	Pin Name	Description
1, 2, 8, 9		Not connected
3	V_1	Control voltage 1 – Control voltage input #1. The logic level voltage applied to this pin, along with the level voltage applied to pin 7, determines the states of the RF paths between the TX, RX, ANT1 and ANT2 ports
4	ANT1	RF input/output – RF input/output port which is either connected via a low insertion loss path to the TX or RX port, according to the logic levels applied to V_1 and V_2
6	ANT2	RF input/output – RF input/output port which is either connected via a low insertion loss path to the TX or RX port, according to the logic levels applied to V_1 and V_2
5, 11	GND	Equipotential point - Internal circuit common, which must be connected to the pcb ground or common via the lowest possible impedance
7	V_2	Control voltage 2 – Control voltage input #2. The logic level voltage applied to this pin, along with the level voltage applied to pin 3, determines the states of the RF paths between the TX, RX, ANT1 and ANT2 ports
10	R_X	RF output – RF output port which is typically connected to the input of a receiver signal path
12	T_X	RF input – RF input port which is typically connected to the output of a transmitter signal path

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Evaluation Board

The evaluation board for SKY13267-321 allows the part to be fully exercised. Note that blocking capacitors are required on each RF port (TX, RX, ANT1 and ANT2).

The state of the SKY13267-321 is controlled by applying the appropriate logic level voltages to ports V_1 and V_2, per Table 4.

Table 6. Evaluation Board Components

Component	Description	Default
C_{BLOCK}	DC blocking capacitor	4.7 pF, size 0402
U1	SKY13267-321 GaAs T/R-diversity switch	
TX, RX, ANT1, ANT2	SMA connectors	
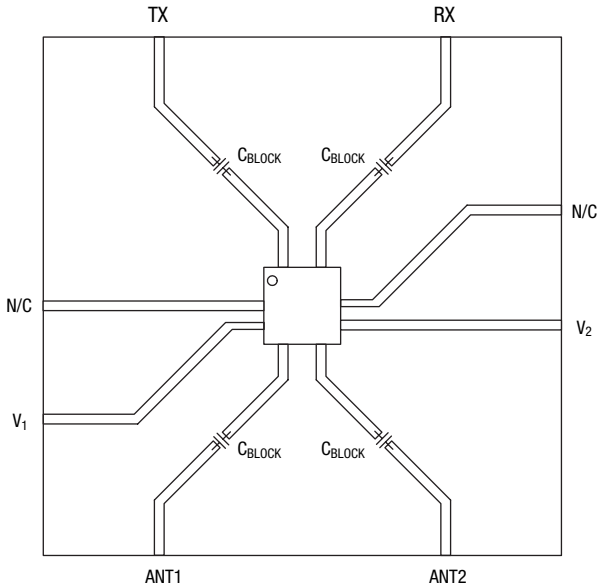
Figure 8. SKY13267-321 Evaluation Circuit

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