NEC Electronics Inc.

CMOS-6/6A 1.0-MICRON CMOS GATE ARRAYS

PRELIMINARY

February 1990

Description

NEC's CMOS-6 gate array families (CMOS-6, CMOS-6A) are ultra-high performance, sub-micron channel length CMOS products created for high-integration ASIC applications.

The device processing includes 1.0-micron (drawn) silicon-gate CMOS technology and three-layer (CMOS-6) and two-layer (CMOS-6A) metallization. This technology features channelless (sea of gates) architecture in densities of from 5,000 to 177,408 equivalent gates, with an internal gate delay of 270 ps (F/O=1). Output drive is variable to 18 mA.

CMOS-6 products are fully supported by NEC's ASIC design technology. NEC's OpenCAD™ integration system lets the designer choose the most powerful design tools and services available. Advanced macro cells and free-size memory configuration are features of the CMOS-6 families, allowing design flexibility and quick turnaround time on designs over 100,000 gates [free-size memory blocks to 64 Kbytes (16K×4, μPD65676)]. The CMOS-6/6A macro cell (block) library is compatible with the powerful CMOS-4 and CMOS-5 block libraries, which contain over 300 cells and more than 100 interface options.

NEC offers advanced packaging solutions with both through-hole and surface-mount ceramic PGAs and flat packages. These heat-sink-equipped packages give CMOS-6 devices the performance edge in high-integration applications.

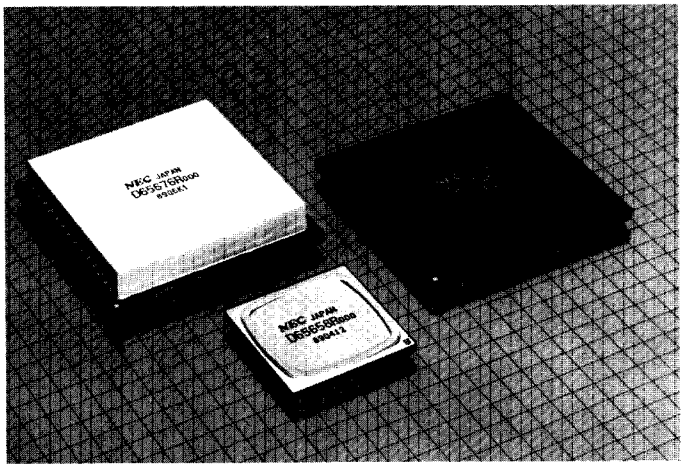
Features

- Channelless, high-density architecture
- Advanced CMOS technology
- High-speed operation
- Variable output drive
- Free-size memory blocks
- Surface-mount options for large packages

Publications

This data sheet contains preliminary specifications, package information, and operational data for the CMOS-6 gate array families. Additional design information is available in NEC's CMOS-6 Block Library and CMOS-6 Design Manual. Contact your local NEC Design Center or the NEC Literature Center for further ASIC design information; see the back of this data sheet for locations and phone numbers.

Figure 1. Sample CMOS-6 Packages



Gate Array Sizes

Device (μPD)	Available Gates	Usable Gates: Target Design = 50% Memory	Usable Gates: Target Design = All Random	I/O Pins (Max.)
CMOS-6 Devices				
65630	5,000	3,000	2,000	96
65636	8,000	4,800	3,200	114
65640	11,000	6,600	4,400	132
65646	16,000	9,600	6,400	154
65650	21,000	12,600	8,400	174
65654	30,000	18,000	12,000	204
CMOS-6A Devices				
65658	42,240	31,680	21,120	220
65644	75,576	54,432	36,288	288
65672	119,232	89,424	59,616	370
65676	177,408	133,056	88,704	448

Figure 2. Chip Layout and Internal Cell Configuration

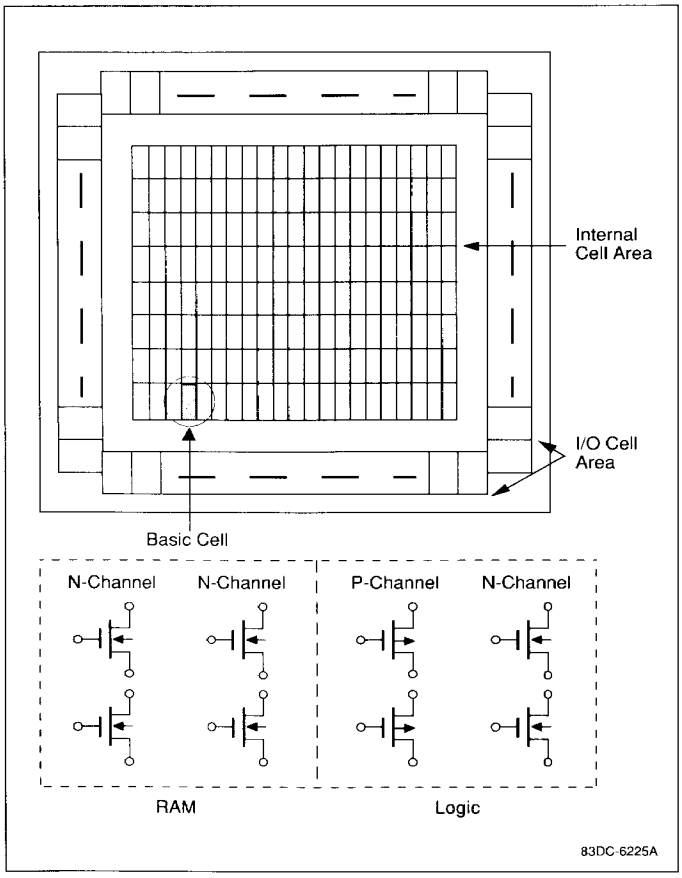
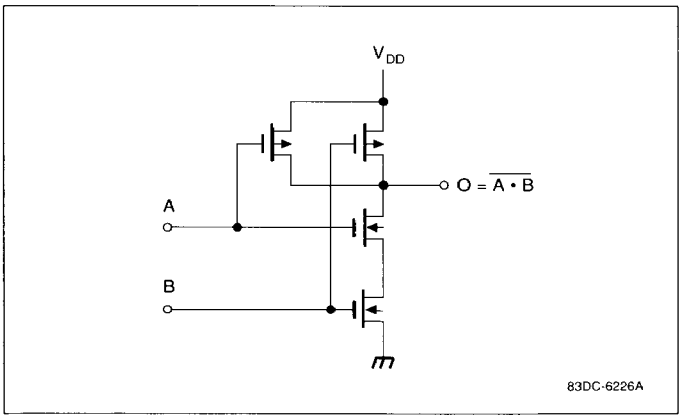


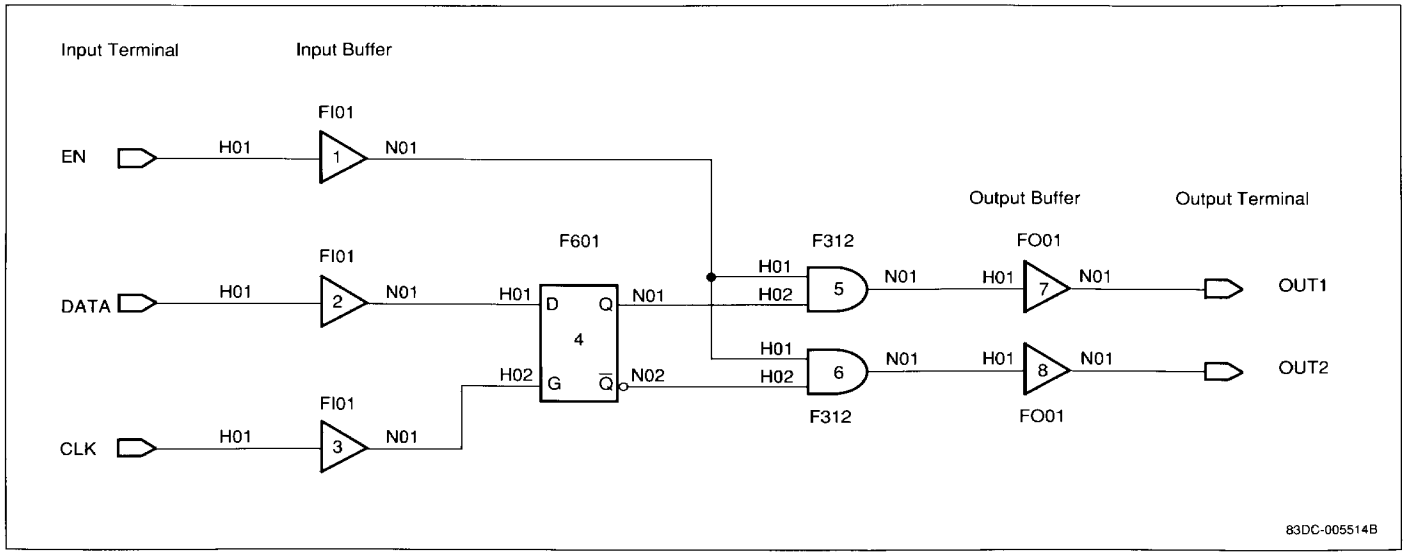
Figure 3. Cell Configured as a Two-Input NAND



Circuit Architecture

CMOS-6 products are built with NEC's 1-micron channelless architecture. As shown in figure 2, CMOS gate array chips are divided into I/O and internal cell areas. The I/O cell area contains input and output buffers that isolate the internal cells from high-energy external signals. The internal cell area is an array of basic cells, each composed of two p-channel MOS transistors and two n-channel MOS transistors, as well as four additional n-channel MOS transistors for compact RAM design. These p-channel and n-channel transistors are sized to offer a superb ratio of speed to silicon area.

Figure 4. Example of a Circuit Diagram



Absolute Maximum Ratings

Power supply voltage, V_{DD}	–0.5 to +6.5 V
Input/output voltage, V_I / V_O	–0.5 V to V_{DD} + 0.5 V
Latch-up current, I_{LATCH}	>1 A (typ)
Output current, I_O	
4.5-mA drive	10 mA
9-mA drive	20 mA
13.5-mA drive	30 mA
18-mA drive	40 mA
Operating temperature, T_{OPT}	–40 to +85 °C
Storage temperature, T_{STG}	–65 to +150 °C

Caution: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should not be operated outside the Recommended Operating Conditions.

Input/Output Capacitance

$V_{DD} = V_I = 0$ V; f = 1 MHz

Terminal	Symbol	Typ	Max	Unit
Input	C_{IN}	10	25	pF
Output	C_{OUT}	10	25	pF
I/O	$C_{I/O}$	10	25	pF

Note:

(1) Values include package pin capacitance.

Power Consumption

Description	Limits (max)	Unit	Test Conditions
Internal cell	8	μW/MHz	F/O = 3; L = 3 mm
Input block	46	μW/MHz	F/O = 3; L = 3 mm
Output block	.98	mW/MHz	C_L = 15 pF

Recommended Operating Conditions

		CMOS Level		TTL Level		
Parameter	Symbol	Min	Max	Min	Max	Unit
Power supply voltage	V_{DD}	4.5	5.5	4.75	5.25	V
Ambient temperature	T_A	–40	+85	0	+70	°C
Low-level input voltage	V_{IL}	0	0.3 V_{DD}	0	0.8	V
High-level input voltage	V_{IH}	0.7 V_{DD}	V_{DD}	2.2	V_{DD}	V
Input rise or fall time	t_R, t_F	0	200	0	200	ns
Input rise or fall time, Schmitt	t_R, t_F	0	10	0	10	ms
Positive Schmitt-trigger voltage	V_P	1.8	4.0	1.2	2.4	V
Negative Schmitt-trigger voltage	V_N	0.6	3.1	0.6	1.8	V
Hysteresis voltage	V_H	0.3	1.5	0.3	1.5	V

AC Characteristics

$V_{DD} = 5$ V ± 10%; $T_A = -40$ to +85 °C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Toggle frequency	f_{TOG}	120			MHz	D-F/F; F/O = 1
Delay time, internal gate	t_{PD}		270		ps	F/O = 1; L = 0 mm
			700		ps	F/O = 3; L = 3 mm
Delay time, buffer						
Input (FI01)	t_{PD}		0.8		ns	F/O = 1; L = 0 mm
			1.0		ns	F/O = 3; L = 3 mm
Output (FO01)	t_{PD}		2.0		ns	C_L = 15 pF
Output rise time	t_R		3.0		ns	C_L = 15 pF
Output fall time	t_F		2.0		ns	C_L = 15 pF

DC Characteristics

V_{DD} = 5 V ± 10%; T_A = −40 to +85 °C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Quiescent current (Note 1)	I_L		0.1	400	µA	$V_I = V_{DD}$ or GND
Input leakage current						
Regular	I_I		10^{-5}	10	µA	$V_I = V_{DD}$ or GND
50 kΩ pullup	I_I	−40	−100	−270	µA	V_I = GND
5 kΩ pullup	I_I	−0.35	−1.0	−2.2	mA	V_I = GND
50 kΩ pulldown	I_I	45	120	300	µA	$V_I = V_{DD}$
Off-state output leakage current	I_{OZ}			10	µA	$V_O = V_{DD}$ or GND
Input clamp voltage	V_{IC}	−1.2			V	I_I = 18 mA
Output current limit (Note 2)	I_{OS}	−250			mA	V_O = 0 V
Low-level output current (CMOS)						
4.5 mA (Note 3)	I_{OL}	4.5	TBD		mA	V_{OL} = 0.4 V
9 mA (Note 3)	I_{OL}	9.0	TBD		mA	V_{OL} = 0.4 V
13.5 mA (Note 3)	I_{OL}	13.5	TBD		mA	V_{OL} = 0.4 V
18 mA (Note 3)	I_{OL}	18.0	TBD		mA	V_{OL} = 0.4 V
High-level output current (CMOS)						
4.5 mA (Note 3)	I_{OH}	−2.5	TBD		mA	$V_{OH} = V_{DD}$ −0.4 V
9 mA (Note 3)	I_{OH}	−5.0	TBD		mA	$V_{OH} = V_{DD}$ −0.4 V
13.5 mA (Note 3)	I_{OH}	−7.5	TBD		mA	$V_{OH} = V_{DD}$ −0.4 V
18 mA (Note 3)	I_{OH}	−10.0	TBD		mA	$V_{OH} = V_{DD}$ −0.4 V
Low-level output current (TTL)						
9 mA (Note 4)	I_{OL}	9.0	TBD		mA	V_{OL} = 0.4 V
18 mA (Note 4)	I_{OL}	18.0	TBD		mA	V_{OL} = 0.4 V
High-level output current (TTL)						
9 mA (Note 4)	I_{OH}	−0.5	TBD		mA	V_{OH} = 2.4 V
18 mA (Note 4)	I_{OH}	−1.0	TBD		mA	V_{OH} = 2.4 V
Low-level output voltage	V_{OL}			0.1	V	I_{OL} = 0 mA
High-level output voltage (CMOS) (Note 3)	V_{OH}	V_{DD}−0.1			V	I_{OH} = 0 mA
High-level output voltage (TTL) (Note 4)	V_{OH}	2.6	3.4		V	I_{OH} = 0 mA

Notes:

(1) The maximum value reflects the use of pullup/pulldown resistors and oscillator blocks. Contact an NEC ASIC Design Center for assistance in calculation.

(2) Rating is for only one output operating in this mode for less than 1 second.

(3) CMOS-level output buffer (V_{DD} = 5 V ± 10%, T_A = −40 to +85 °C).

(4) TTL-level output buffer (V_{DD} = 5 V ± 5%, T_A = 0 to +70 °C).

NEC's ASIC Design System

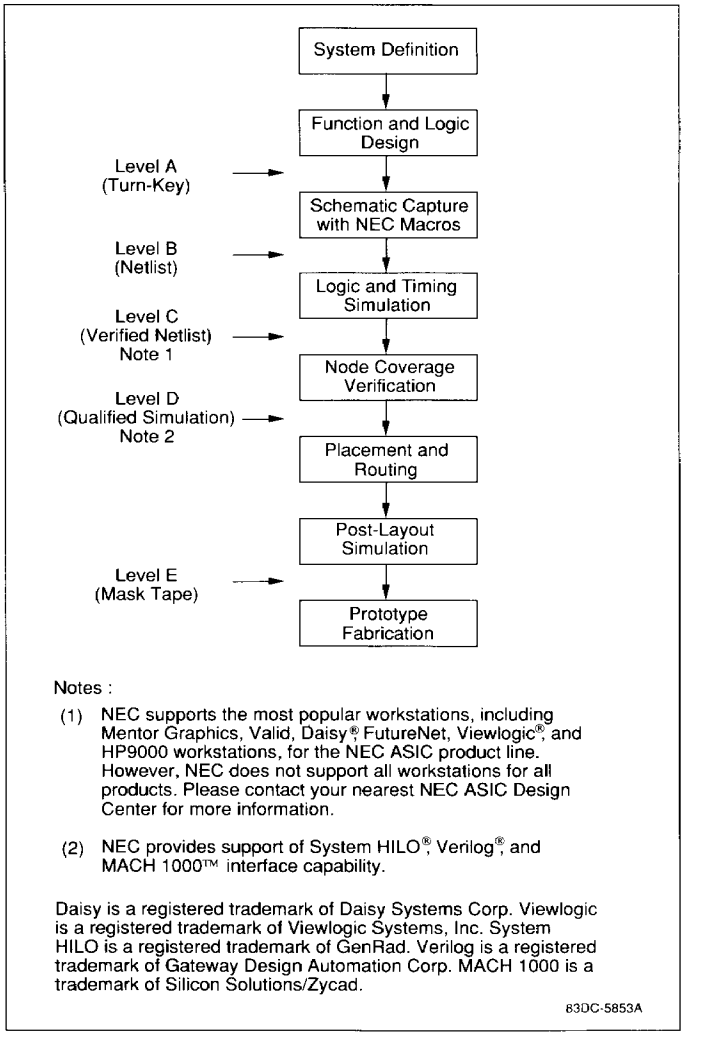
CMOS-6/6A gate arrays are fully supported by NEC's network of ASIC Design Centers, listed on the back of this data sheet.

Design flow for CMOS-6/6A gate arrays is shown in figure 5. Users can enlist Design Center support at any step in the design flow before actual manufacturing. Figure 5 shows the various levels at which Design Center support may begin — anywhere from level A through level E. Level C, "Verified Netlist," is the most popular interface.

NEC supports its ASIC products with a comprehensive CAD system that significantly reduces the time and expense usually associated with the development of semi-custom devices. NEC's OpenCAD integration system supports tools for floor-planning, logic synthesis, automatic test generation, accelerated fault grading and full timing simulation, and advanced place-and-route algorithms. These advanced CAD tools ensure accurate designs.

Sample design kits are available at no charge to qualified users: contact an NEC ASIC Design Center for more information. (Software licensing required—NEC reserves the right to prioritize support based on user requirements.)

Figure 5. Gate Array Design Flow



Notes :

(1) NEC supports the most popular workstations, including Mentor Graphics, Valid, Daisy®, FutureNet, Viewlogic®, and HP9000 workstations, for the NEC ASIC product line. However, NEC does not support all workstations for all products. Please contact your nearest NEC ASIC Design Center for more information.

(2) NEC provides support of System HILO®, Verilog®, and MACH 1000™ interface capability.

Daisy is a registered trademark of Daisy Systems Corp. Viewlogic is a registered trademark of Viewlogic Systems, Inc. System HILO is a registered trademark of GenRad. Verilog is a registered trademark of Gateway Design Automation Corp. MACH 1000 is a trademark of Silicon Solutions/Zycad.

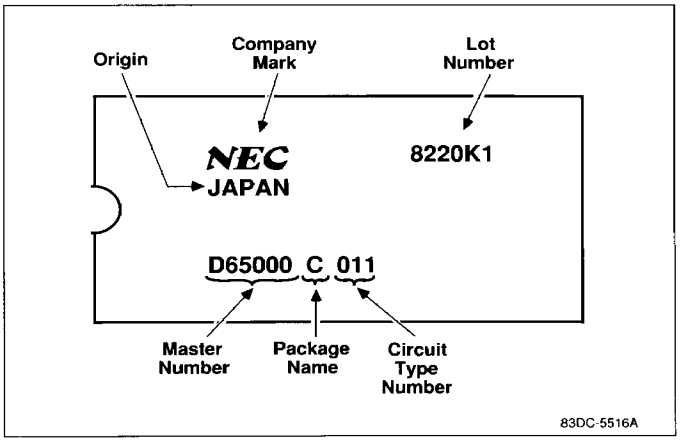
83DC-5853A

Package Plan

	μPD65xxx									
	630	636	640	646	650	654	658	664	672	676
Plastic Leaded Chip Carrier (PLCC)										
68-pin	X	X	X	X	X	X				
84-pin	X	X	X	X	X	X	X			
Plastic Flatpack (QFP)										
80-pin	X	X	X	X	X					
100-pin	X	X	X	X	X	X				
120-pin		X	X	X	X	X	X	X	X	X
136-pin				X	X	X	X	X	X	X
160-pin						X	X	X	X	X
208-pin									X	X
Ceramic Flatpack (CQFP)										
160-pin						X	X	X	X	X
208-pin								X	X	X
296-pin								X	X	X
Ceramic Pin Grid Array (CPGA)										
72-pin	X	X	X	X	X					
132-pin	X	X	X	X	X	X	X	X	X	
176-pin					X	X	X	X	X	X
208-pin							X	X	X	X
280-pin								X	X	X
364-pin									X	X
Surface-Mount CPGA, Butt Lead										
288-pin								X	X	X
528-pin									X	X

Important: NEC has begun qualification of the packages listed above and reserves the right to alter the package plan based on the results of qualification. All packages may not be immediately available. For current package availability, please contact your NEC Design Center.

Typical Package Marking



Block Library List

The CMOS-6 families offer a variety of blocks, including gates, flip-flop circuits, and shift registers. The functions of these blocks are designed to be compatible with those of the CMOS-4 and CMOS-5 families.

In addition, such memory blocks as RAM and ROM and low-power gates are provided. The low-power block, in particular, was designed with low fan-out taken into consideration; the number of cells is less than that of the standard block, contributing to low power consumption and high efficiency.

Block List

Interface Blocks

Block Name	Description	Cells
Inputs		
FI01	Input buffer (CMOS level)	3
FID1	Input buffer (CMOS level); 50 kΩ pulldown res.	3
FIU1	Input buffer (CMOS level); 50 kΩ pullup res.	3
FIW1	Input buffer (CMOS level); 5 kΩ pullup res.	3
FI02	Input buffer (TTL level)	3
FID2	Input buffer (TTL level); 50 kΩ pulldown res.	3
FIU2	Input buffer (TTL level); 50 kΩ pullup res.	3
FIW2	Input buffer (TTL level); 5 kΩ pullup res.	3
FIS1	Input buffer (CMOS-Schmitt level)	6
FDS1	Input buffer (CMOS-Schmitt level); 50 kΩ pulldown res.	6
FUS1	Input buffer (CMOS-Schmitt level); 50 kΩ pullup res.	6
FWS1	Input buffer (CMOS-Schmitt level); 5 kΩ pullup res.	6
FIS2	Input buffer (TTL-Schmitt level)	6
FDS2	Input buffer (TTL-Schmitt level); 50 kΩ pulldown res.	6
FUS2	Input buffer (TTL-Schmitt level); 50 kΩ pullup res.	6
FWS2	Input buffer (TTL-Schmitt level); 5 kΩ pullup res.	6
Outputs		
FO04	Input buffer (CMOS level); I_{OL} = 4.5 mA	2
FO01	Input buffer (CMOS level); I_{OL} = 9 mA	2
FO02	Input buffer (CMOS level); I_{OL} = 13.5 mA	4
FO03	Input buffer (CMOS level); I_{OL} = 18 mA	4
FT01	Input buffer (TTL level); I_{OL} = 9 mA	4
FT02	Input buffer (TTL level); I_{OL} = 18 mA	6
Three-State Outputs		
B00E	Output buffer (CMOS level); I_{OL} = 4.5 mA	5
B0DE	Output buffer (CMOS level); I_{OL} = 4.5 mA, 50 kΩ pulldown res.	5
B0UE	Output buffer (CMOS level); I_{OL} = 4.5 mA, 50 kΩ pullup res.	5
B0WE	Output buffer (CMOS level); I_{OL} = 4.5 mA, 5 kΩ pullup res.	5
B008	Output buffer (CMOS level); I_{OL} = 9 mA	5
B0D8	Output buffer (CMOS level); I_{OL} = 9 mA, 50 kΩ pulldown res.	5
B0U8	Output buffer (CMOS level); I_{OL} = 9 mA, 50 kΩ pulldown res.	5
B0W8	Output buffer (CMOS level); I_{OL} = 9 mA, 5 kΩ pulldown res.	5
B007	Output buffer (CMOS level); I_{OL} = 13.5 mA	6
B0D7	Output buffer (CMOS level); I_{OL} = 13.5 mA, 50 kΩ pulldown res.	6
B0U7	Output buffer (CMOS level); I_{OL} = 13.5 mA, 50 kΩ pulldown res.	6
B0W7	Output buffer (CMOS level); I_{OL} = 13.5 mA, 5 kΩ pulldown res.	6
B009	Output buffer (CMOS level); I_{OL} = 18 mA	6
B0D9	Output buffer (CMOS level); I_{OL} = 18 mA, 50 kΩ pulldown res.	6
B0U9	Output buffer (CMOS level); I_{OL} = 18 mA, 50 kΩ pulldown res.	6
B0W9	Output buffer (CMOS level); I_{OL} = 18 mA 5 kΩ pullup res.	6
BT08	Output buffer (TTL level); I_{OL} = 9 mA	6
BTU8	Output buffer (TTL level); I_{OL} = 9 mA, 50 kΩ pullup res.	6
BTW8	Output buffer (TTL level); I_{OL} = 9 mA, 5 kΩ pullup res.	6
BT09	Output buffer (TTL level); I_{OL} = 18 mA	9
BTU9	Output buffer (TTL level); I_{OL} = 18 mA, 50 kΩ pullup res.	9
BTW9	Output buffer (TTL level); I_{OL} = 18 mA, 5 kΩ pullup res.	9
Open Drain Outputs		
EXT1	Output buffer (N-ch); I_{OL} = 9 mA	2
EXT3	Output buffer (N-ch); I_{OL} = 9 mA, 50 kΩ pullup res.	2
EXW3	Output buffer (N-ch); I_{OL} = 9 mA, 5 kΩ pullup res.	2
EXT9	Output buffer (N-ch); I_{OL} = 13.5 mA	2
EXTB	Output buffer (N-ch); I_{OL} = 13.5 mA, 50 kΩ pullup res.	2
EXWB	Output buffer (N-ch); I_{OL} = 13.5 mA, 5 kΩ pullup res.	2
EXT5	Output buffer (N-ch); I_{OL} = 18 mA	2
EXT7	Output buffer (N-ch); I_{OL} = 18 mA, 50 kΩ pullup res.	2
EXW7	Output buffer (N-ch); I_{OL} = 18 mA, 5 kΩ pullup res.	2
EXT2	Output buffer (P-ch); I_{OH} = 9 mA	2
EXT4	Output buffer (P-ch); I_{OH} = 9 mA, 50 kΩ pulldown res.	2
EXTA	Output buffer (P-ch); I_{OH} = 13.5 mA	2
EXTC	Output buffer (P-ch); I_{OH} = 13.5 mA, 50 kΩ pulldown res.	2
EXT6	Output buffer (P-ch); I_{OH} = 18 mA, 50 kΩ pulldown res.	2
EXT8	Output buffer (P-ch); I_{OH} = 18 mA 50 kΩ pulldown res.	2

Interface Blocks (Cont.)

Block Name	Description	Cells
Three-State Bidirectional Buffers		
B00C	I/O buffer (CMOS in, CMOS out); I_{OL} = 4.5 mA	8
B0DC	I/O buffer (CMOS in, CMOS out); I_{OL} = 4.5 mA, 50 kΩ pulldown res.	8
B0UC	I/O buffer (CMOS in, CMOS out); I_{OL} = 4.5 mA, 50 kΩ pullup res.	8
B0WC	I/O buffer (CMOS in, CMOS out); I_{OL} = 4.5 mA, 5 kΩ pullup res.	8
B003	I/O buffer (CMOS in, CMOS out); I_{OL} = 9 mA	8
B0D3	I/O buffer (CMOS in, CMOS out); I_{OL} = 9 mA, 50 kΩ pulldown res.	8
B0U3	I/O buffer (CMOS in, CMOS out); I_{OL} = 9 mA, 50 kΩ pullup res.	8
B0W3	I/O buffer (CMOS in, CMOS out); I_{OL} = 9 mA, 5 kΩ pullup res.	8
B001	I/O buffer (CMOS in, CMOS out); I_{OL} = 13.5 mA	9
B0D1	I/O buffer (CMOS in, CMOS out); I_{OL} = 13.5 mA, 50 kΩ pulldown res.	9
B0U1	I/O buffer (CMOS in, CMOS out); I_{OL} = 13.5 mA, 50 kΩ pullup res.	9
B0W1	I/O buffer (CMOS in, CMOS out); I_{OL} = 13.5 mA, 5 kΩ pullup res.	9
B005	I/O buffer (CMOS in, CMOS out); I_{OL} = 18 mA	9
B0D5	I/O buffer (CMOS in, CMOS out); I_{OL} = 18 mA, 50 kΩ pulldown res.	9
B0U5	I/O buffer (CMOS in, CMOS out); I_{OL} = 18 mA, 50 kΩ pullup res.	9
B0W5	I/O buffer (CMOS in, CMOS out); I_{OL} = 18 mA, 5 kΩ pullup res.	9
B00D	I/O buffer (TTL in, CMOS out); I_{OL} = 4.5 mA	8
B0DD	I/O buffer (TTL in, CMOS out); I_{OL} = 4.5 mA, 50 kΩ pulldown res.	8
B0UD	I/O buffer (TTL in, CMOS out); I_{OL} = 4.5 mA, 50 kΩ pullup res.	8
B0WD	I/O buffer (TTL in, CMOS out); I_{OL} = 4.5 mA, 5 kΩ pullup res.	8
B004	I/O buffer (TTL in, CMOS out); I_{OL} = 9 mA	8
B0D4	I/O buffer (TTL in, CMOS out); I_{OL} = 9 mA, 50 kΩ pulldown res.	8
B0U4	I/O buffer (TTL in, CMOS out); I_{OL} = 9 mA, 50 kΩ pullup res.	8
B0W4	I/O buffer (TTL in, CMOS out); I_{OL} = 9 mA, 5 kΩ pullup res.	8
B002	I/O buffer (TTL in, CMOS out); I_{OL} = 13.5 mA	9
B0D2	I/O buffer (TTL in, CMOS out); I_{OL} = 13.5 mA, 50 kΩ pulldown res.	9
B0U2	I/O buffer (TTL in, CMOS out); I_{OL} = 13.5 mA, 50 kΩ pullup res.	9
B0W2	I/O buffer (TTL in, CMOS out); I_{OL} = 13.5 mA, 5 kΩ pullup res.	9
B006	I/O buffer (TTL in, CMOS out); I_{OL} = 18 mA	9
B0D6	I/O buffer (TTL in, CMOS out); I_{OL} = 18 mA, 50 kΩ pulldown res.	9
Three-State Bidirectional Buffers (Cont.)		
B0U6	I/O buffer (TTL in, CMOS out); I_{OL} = 18 mA, 50 kΩ pullup res.	9
B0W6	I/O buffer (TTL in, CMOS out); I_{OL} = 18 mA, 5 kΩ pullup res.	9
B00A	I/O buffer (TTL in, TTL out); I_{OL} = 9 mA	9
B0UA	I/O buffer (TTL in, TTL out); I_{OL} = 9 mA, 50 kΩ pullup res.	9
B0WA	I/O buffer (TTL in, TTL out); I_{OL} = 9 mA, 5 kΩ pullup res.	9
B00B	I/O buffer (TTL in, TTL out); I_{OL} = 18 mA	12
B0UB	I/O buffer (TTL in, TTL out); I_{OL} = 18 mA, 50 kΩ pullup res.	12
B0WB	I/O buffer (TTL in, TTL out); I_{OL} = 18 mA, 5 kΩ pullup res.	12
Schmitt-Input Bidirectional Buffers		
BSIC	I/O buffer (CMOS-S in, CMOS out); I_{OL} = 4.5 mA	11
BSDC	I/O buffer (CMOS-S in, CMOS out); I_{OL} = 4.5 mA, 50 kΩ pulldown res.	11
BSUC	I/O buffer (CMOS-S in, CMOS out); I_{OL} = 4.5 mA, 50 kΩ pullup res.	11
BSWC	I/O buffer (CMOS-S in, CMOS out); I_{OL} = 4.5 mA, 5 kΩ pullup res.	11
BSI3	I/O buffer (CMOS-S in, CMOS out); I_{OL} = 9 mA	11
BSD3	I/O buffer (CMOS-S in, CMOS out); I_{OL} = 9 mA, 50 kΩ pulldown res.	11
BSU3	I/O buffer (CMOS-S in, CMOS out); I_{OL} = 9 mA, 50 kΩ pullup res.	11
BSW3	I/O buffer (CMOS-S in, CMOS out); I_{OL} = 9 mA, 5 kΩ pullup res.	11
BSI1	I/O buffer (CMOS-S in, CMOS out); I_{OL} = 13.5 mA	12
BSD1	I/O buffer (CMOS-S in, CMOS out); I_{OL} = 13.5 mA, 50 kΩ pulldown res.	12
BSU1	I/O buffer (CMOS-S in, CMOS out); I_{OL} = 13.5 mA, 50 kΩ pullup res.	12
BSW1	I/O buffer (CMOS-S in, CMOS out); I_{OL} = 13.5 mA, 5 kΩ pullup res.	12
BSI5	I/O buffer (CMOS-S in, CMOS out); I_{OL} = 18 mA	12
BSD5	I/O buffer (CMOS-S in, CMOS out); I_{OL} = 18 mA, 50 kΩ pulldown res.	12
BSU5	I/O buffer (CMOS-S in, CMOS out); I_{OL} = 18 mA, 50 kΩ pullup res.	12
BSW5	I/O buffer (CMOS-S in, CMOS out); I_{OL} = 18 mA, 5 kΩ pullup res.	12
BSID	I/O buffer (TTL-S in, CMOS out); I_{OL} = 4.5 mA	11
BSDD	I/O buffer (TTL-S in, CMOS out); I_{OL} = 4.5 mA, 50 kΩ pulldown res.	11
BSUD	I/O buffer (TTL-S in, CMOS out); I_{OL} = 4.5 mA, 50 kΩ pullup res.	11
BSWD	I/O buffer (TTL-S in, CMOS out); I_{OL} = 4.5 mA, 5 kΩ pullup res.	11

Interface Blocks (Cont.)

Block Name	Description	Cells
Schmitt-Input Bidirectional Buffers (Cont.)		
BSI4	I/O buffer (TTL-S in, CMOS out); I_{OL} = 9 mA	11
BSD4	I/O buffer (TTL-S in, CMOS out); I_{OL} = 9 mA, 50 kΩ pulldown res.	11
BSU4	I/O buffer (TTL-S in, CMOS out); I_{OL} = 9 mA, 50 kΩ pullup res.	11
BSW4	I/O buffer (TTL-S in, CMOS out); I_{OL} = 9 mA, 5 kΩ pullup res.	11
BSI2	I/O buffer (TTL-S in, CMOS out); I_{OL} = 13.5 mA	12
BSD2	I/O buffer (TTL-S in, CMOS out); I_{OL} = 13.5 mA, 50 kΩ pulldown res.	12
BSU2	I/O buffer (TTL-S in, CMOS out); I_{OL} = 13.5 mA, 50 kΩ pullup res.	12
BSW2	I/O buffer (TTL-S in, CMOS out); I_{OL} = 13.5 mA, 5 kΩ pullup res.	12
BSI6	I/O buffer (TTL-S in, CMOS out); I_{OL} = 18 mA	12
BSD6	I/O buffer (TTL-S in, CMOS out); I_{OL} = 18 mA, 50 kΩ pulldown res.	12
BSU6	I/O buffer (TTL-S in, CMOS out); I_{OL} = 18 mA, 50 kΩ pullup res.	12
BSW6	I/O buffer (TTL-S in, CMOS out); I_{OL} = 18 mA, 5 kΩ pullup res.	12
BSIA	I/O buffer (TTL-S in, TTL out); I_{OL} = 9 mA	12
BSUA	I/O buffer (TTL-S in, TTL out); I_{OL} = 9 mA, 50 kΩ pullup res.	12
BSWA	I/O buffer (TTL-S in, TTL out); I_{OL} = 9 mA, 5 kΩ pullup res.	12
BSIB	I/O buffer (TTL-S in, TTL out); I_{OL} = 18 mA	15
BSUB	I/O buffer (TTL-S in, TTL out); I_{OL} = 18 mA, 50 kΩ pullup res.	15
BSWB	I/O buffer (TTL-S in, TTL out); I_{OL} = 18 mA, 5 kΩ pullup res.	15

Function Blocks

Block Name	Description	Cells
Inverters		
F101	Inverter, F/O = 17	1
L101	Inverter, low power, F/O = 3	1
F102	Inverter, F/O = 37	2
F103	Inverter, F/O = 60	3
F104	Inverter, F/O = 92	4
F108	Inverter, F/O = 160	12
Buffers		
F111	Buffer, F/O = 17	2
L111	Buffer, low power, F/O =3	1
F112	Buffer, F/O = 35	3
F113	Buffer, F/O = 54	4
F114	Buffer, F/O = 74	5
F118	Buffer, F/O = 180	11

Function Blocks (Cont.)

Block Name	Description	Cells
NOR Gates		
F202	2-Input NOR	2
L202	2-Input NOR, low power	1
F222	2-Input NOR, powered	4
F203	3-Input NOR	3
L203	3-Input NOR, low power	2
F223	3-Input NOR, powered	6
F204	4-Input NOR	4
L204	4-Input NOR, low power	2
F224	4-Input NOR, powered	8
F208	8-Input NOR	7
OR Gates		
F212	2-Input OR	2
L212	2-Input OR, low power	2
F213	3-Input OR	3
L213	3-Input OR, low power	2
F214	4-Input OR	3
L214	4-Input OR, low power	3
F232	2-Input OR, powered	3
F233	3-Input OR, powered	4
F234	4-Input OR, powered	4
NAND Gates		
F302	2-Input NAND	2
L302	2-Input NAND, low power	1
F322	2-Input NAND, powered	4
F303	3-Input NAND	3
L303	3-Input NAND, low power	2
F323	3-Input NAND, powered	6
F304	4-Input NAND	4
L304	4-Input NAND, low power	2
F324	4-Input NAND, powered	8
F305	5-Input NAND	5
L305	5-Input NAND, low power	3
F306	6-Input NAND	5
L306	6-Input NAND, low power	3
F308	8-Input NAND	6
AND Gates		
F312	2-Input AND	2
L312	2-Input AND, low power	2
F332	2-Input AND, powered	3
F313	3-Input AND	3
L313	3-Input AND, low power	2
F333	3-Input AND, powered	4
F314	4-Input AND	3
L314	4-Input AND, low power	3
F334	4-Input AND, powered	4

Function Blocks (Cont.)

Block Name	Description	Cells
AND-NOR Gates		
F421	2-Wide, 1-2-input AND-OR inverter	3
L421	2-Wide, 1-2-input AND-OR inverter, low power	2
F422	3-Wide, 1-1-2-input AND-OR inverter	4
L422	3-Wide, 1-1-2-input AND-OR inverter	2
F423	2-Wide, 1-3-input AND-OR inverter	4
L423	2-Wide, 1-3-input AND-OR inverter, low power	2
F424	2-Wide, 2-2-input AND-OR inverter	4
L424	2-Wide, 2-2-input AND-OR inverter, low power	2
F425	3-Wide, 2-2-2-input AND-OR inverter	6
L425	3-Wide, 2-2-2-input AND-OR inverter, low power	3
F426	2-Wide, 3-3-input AND-OR inverter	6
L426	2-Wide, 3-3-input AND-OR inverter, low power	3
F429	4-Wide 2-2-2-2-input AND-OR inverter	8
L429	4-Wide 2-2-2-2-input AND-OR inverter, low power	4
F442	2-Wide, 4-4-input AND-OR inverter	8
L442	2-Wide, 4-4-input AND-OR inverter, low power	4
F462	3-Wide 1-2-3-input AND-OR inverter	6
L462	3-Wide 1-2-3-input AND-OR inverter, low power	3
OR-NAND Gates		
F431	2-Wide, 1-2-input OR-AND inverter	3
L431	2-Wide, 1-2-input OR-AND inverter, low power	2
F432	3-Wide, 1-1-2-input OR-AND inverter	4
L432	3-Wide, 1-1-2-input OR-AND inverter, low power	2
F433	2-Wide, 1-3-input OR-AND inverter	4
L433	2-Wide, 1-3-input OR-AND inverter, low power	2
F434	2-Wide, 2-2-input OR-AND inverter	4
L434	2-Wide, 2-2-input OR-AND inverter, low power	2
F435	2-Wide, 2-3-input OR-AND inverter	5
L435	2-Wide, 2-3-input OR-AND inverter, low power	3
F436	2-Wide, 3-3-input OR-AND inverter	6
L436	2-Wide, 3-3-input OR-AND inverter, low power	3
F454	4-Wide, 2-2-2-2-input OR-AND inverter	8
L454	4-Wide, 2-2-2-2-input OR-AND inverter, low power	4
Drivers		
F501	Clock driver	2
F502	Dual clock driver	4
Exclusive-OR, Exclusive-NOR Gates		
F511	EX-OR	4
L511	EX-OR, low power	3
F512	EX-NOR	4
L512	EX-NOR, low power	3
Full Adders		
F521	1-Bit full adder	9
F523	4-Bit binary full adder	32
Three-State Buffers		
F531	Buffer	5
F532	Buffer with EN	5

Block Name	Description	Cells
Decoders		
F561	2-to-4 Decoder	10
L561	2-to-4 Decoder, low power	6
F981	2-to-4 Decoder with EN	13
L981	2-to-4 Decoder with EN, low power	8
F982	3-to-8 Decoder with EN	26
L982	3-to-8 Decoder with EN, low power	17
Multiplexers		
F569	8-to-1 Multiplexer	18
F570	4-to-1 Multiplexer	10
F571	2-to-1 Multiplexer	6
F572	Quad 2-to-1 Multiplexer	14
L572	Quad 2-to-1 Multiplexer, low power	10
Parity Generators		
F581	8-Bit odd	19
F582	8-Bit even	19
Latches		
F595	R-S latch	5
F596	Synchronous R-S F/F with Reset	11
F601	D latch	6
L601	D latch, low power	3
F602	D latch with Reset	6
L602	D latch with Reset, low power	4
F603	D latch with Reset	7
L603	D latch with Reset, low power	4
F604	D latch with Clock driver	6
L604	D latch with Clock driver, low power	3
F605	D latch with Clock driver, Reset	7
L605	D latch with Clock driver, Reset, low power	4
F901	4-Bit D latch	20
L901	4-Bit D latch, low power	10
F902	8-Bit D latch	38
L902	8-Bit D latch, low power	18
Flip-Flops		
F611	D F/F	8
L611	D F/F, low power	5
F614	D F/F with Set-Reset	10
L614	D F/F with Set-Reset, low power	7
F617	D F/F with Set-Reset	10
L617	D F/F with Set-Reset, low power	7
F631	D F/F with C	8
F631	D F/F with C, low power	5
F637	D F/F with C, Set-Reset	10
L637	D F/F with C, Set-Reset, low power	7
F641	D F/F, buffered out	8
F644	D F/F with Set-Reset; buffered out	10
F647	D F/F with Set-Reset; buffered out	10
F661	D F/F with C	8
F667	D F/F with C, Set-Reset; buffered out	10

Function Blocks (Cont.)

Block Name	Description	Cells
Flip-Flops (Cont.)		
F922	4-Bit D F/F with Reset	33
L922	4-Bit D F/F with Reset, low power	23
F924	4-Bit D F/F	28
L924	4-Bit D F/F, low power	18
Shift Registers		
F911	4-Bit register with Reset	33
L911	4-Bit register with Reset, low power	23
F912	4-Bit serial/parallel register	35
L912	4-Bit serial/parallel register, low power	23
F913	4-Bit parallel-in register with Reset, Load	39
L913	4-Bit parallel-in register with Reset, Load; low power	27
F914	4-Bit register	28
L914	4-Bit register, low power	18
Toggle Flip-Flops		
F714	Toggle with Set-Reset	9
L714	Toggle with Set-Reset, low power	7
F717	Toggle with Set-Reset	9
L717	Toggle with Set-Reset, low power	7
F737	Toggle with Set-Reset	9
L737	Toggle with Set-Reset, low power	7
F744	Toggle with Set-Reset; buffered out	9
F747	Toggle with Set-Reset; buffered out	9
F767	Toggle with Set-Reset; buffered out	9
F791	Toggle with Set-Reset Toggle Enable	12
F792	Toggle with Set-Reset Toggle Enable	12
J-K Flip-Flops		
F771	F/F, buffered out	10
F774	F/F with Set-Reset, buffered out	12
F777	F/F with Set-Reset	12
F781	F/F with C, buffered out	10
F787	F/F with C; Set-Reset, buffered out	12
Counters		
F961	4-Bit synchronous binary counter with Reset, Load	52
F962	4-Bit synchronous binary up, with Reset; buffered out	38
Comparators		
F985	4-Bit magnitude comparator	32
Scan Paths		
S000	D-F/F with Set, Reset	11
S002	D-F/F	9
S050	D-F/F with Set, Reset, Hold	14
S052	D-F/F with Hold	12
S100	JK F/F with Set, Reset	14
S102	JK F/F	12
S150	JK F/F with Set, Reset, Hold	17
S152	JK F/F with Hold	15
S201	D latch with Reset	12
S202	D latch	11
S999	2-to-1 Data selector	4

Block Name	Description	Cells
Delays		
F130	Delay block for monostable multivibrator	4
F131	Delay block	2
F132	Delay block	4
Special		
BUSA	Bus array	0
F091	H, L level generator	1
F093	Interface block for oscillator buffer	1
Oscillators (Note 1)		
OSI1	Oscillator input buffer	1
OSI2	Oscillator input buffer with Enable	1
OSO1	Oscillator output buffer with feedback res.; low freq.	1
OSO2	Oscillator output buffer with feedback res.; high freq.	1
OSO3	Oscillator output buffer; low freq.	1
OSO4	Oscillator output buffer; high freq.	1
OSO7	Oscillator output buffer with feedback and Enable; low freq.	1
OSO8	Oscillator output buffer with feedback and Enable; high freq.	1
Others (Note 1)		
OSF1	Feedback resistance for oscillator (R=500 k)	1
OSF2	Feedback resistance for oscillator (R=250 k)	1
OSF3	Feedback resistance for oscillator (R=500 k); with Enable	1
OSF4	Feedback resistance for oscillator (R=250 k); with Enable	1
SHT1	One-shot monostable multivibrator	1
FIB1	Input buffer for clock driver (CMOS-level input)	1
FIB2	Input buffer for clock driver (TTL-level input)	1

Note:

(1) Oscillator pins must be used in combination. Some valid combinations are:

OSI1 + OSO1	Low Frequency
OSI1 + OSO3 + OSF1	Low Frequency
OSI1 + OSO2	High Frequency
OSI2 + OSO7	Low Frequency with oscillator Enable
OSI2 + OSO3 + OSF3	Low Frequency with oscillator Enable
OSI2 + OSO8	High Frequency with oscillator Enable
OSI2 + OSO4 + OSF4	High Frequency with oscillator Enable

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12