NEC
NEC Electronics Inc.

CB-C8
3-VOLT, 0.5-MICRON CELL-BASED CMOS ASIC

July 1994

Description

NEC's 3-volt CB-C8 cell-based ASIC series are ultra-high performance sub-micron CMOS products built within the OpenCAD Design System™ of NEC. The family allows designing complex logic functions, up to 600,000 gates of user-defined logic, megafunction blocks and compiled memory, using 22 I/O pad ring step sizes of normal pad pitch. Fine pad pitch step sizes are available, enabling a higher I/O to gate count ratio. The CB-C8 technology is 0.5 µm drawn silicon-gate CMOS.

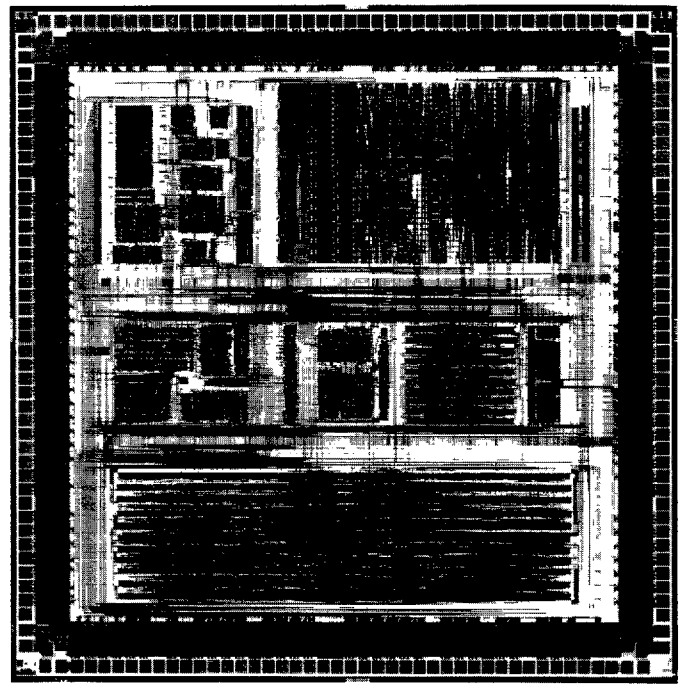
CB-C8 cell-based products are fully supported by the OpenCAD Design System™, a front-end to back-end unified design environment. This merges the best of today's most powerful CAD ASIC software design tools into a single environment. The design methodology incorporates new megafunction blocks that are commensurate with the latest technology advances. Also, memory compilation, floorplanning and hardware acceleration are available to ease design of the CB-C8 cell-based ASIC series.

The CB-C8 library includes basic macrocells as well as NEC's V30MX (16-bit microprocessors), 710XX series support peripherals, and Rambus™ ASIC Cell (RAC). Compilable ASIC RAM and ROM memory blocks are also offered in the library as well as over 300 macrocells and buffer choices of CMOS or TTL levels.

Features

- Advanced sub-micron drawn gate length CMOS technology with three-layer metalization
- Extensive macro library includes soft and hard megafunction blocks
- Internal gate delay of 0.22 ns (F/O = 2; L = 2 mm, power gate)
- Compiled RAM and ROM
- Up to 440 I/O pads
- Low power dissipation 1.25 µW/gate/MHz
- Library characterized at 3.3 V ± 0.3 V and 3 V ± 10%
- I/Os interface direstly 5 V logic
- Wide package selection: CPGA, QFP, PLCC

Figure 1. Typical CB-C8 Series Cell-Based ASIC



A Sample of Megafunctions in Library

Compatible Device	NEC Code	Description
8086	V30MX	16-bit Microprocessor
Z80	70008A	8-bit Microprocessor
8237A	71037	Programmable DMA Controller
8251A	71051	USART
8254	71054	Interval Timer
8255A	71055	Peripheral Interface
8259A	71059	Interrupt Controller
765	72065B	Floppy Disk Controller
4991A	4991A	Real Time Clock

Publications

This data sheet contains preliminary specifications, package information, and operational data for the CB-C8 cell-based CMOS ASIC. Additional design information is available in NEC's CB-C8 Block Library and CB-C8 Design Manual. Contact your local NEC Design Center or the NEC Literature Center for availability and further ASIC design information; see the back of this data sheet for locations and phone numbers.

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Step Sizes and Usable Gate Count

No.	Step Size	Std.I/O[1]	Total Raw Grids	Usable Grids		Usable Gates[2]	
				Two-Layer	Three-Layer	Two-Layer	Three-Layer
1	B18	88	54514	27257	38159	9085	12719
2	B57	104	78051	39025	54636	13008	18212
3	B97	120	105781	52890	74046	17630	24682
4	C37	136	137730	68865	96411	22955	32137
5	C76	152	174314	87157	122020	29052	40673
6	D16	168	214706	107353	150294	35784	50098
7	D55	184	259320	129660	181524	43220	60508
8	D75	192	281698	140849	197189	46949	65729
9	E15	208	333600	166800	233520	55600	77840
10	E54	224	388691	194345	272083	64781	90694
11	E94	240	439059	219529	307341	73176	102447
12	F34	256	500594	250297	350415	83432	116805
13	F74	272	565492	282746	395844	94248	131948
14	G14	288	635786	317893	445050	105964	148350
15	G53	304	708675	354337	496073	118112	165357
16	G93	320	759062	379531	531343	126510	177114
17	H33	336	838390	419195	586873	139731	195624
18	H72	352	920776	460388	644543	153462	214847
19	J32	376	1053685	526842	737579	175614	245859
20	J71	392	1143833	571916	800683	190638	266894
21	K11	408	1239796	619898	867857	206632	289285
22	K90	440	1440973	720486	1008681	240162	336227

Notes: 1. I/O pads may be configured as V_{DD}/ V_{SS}, subject to number and drive of output buffers.

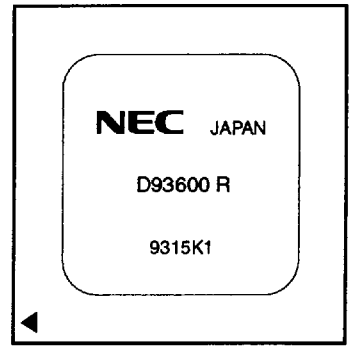
2. Usable gates, equivalent to 2-input NAND gate (L302 type macrocell, which is three grids in area) will vary depending on specific design. Gate/grid ratio is 2.7, based on actual conversion from CMOS gate array families.

Part Numbering System

The CB-C8 part numbering system is as follows:

Part Number	Description
µPD936XX	Contains logic only or logic plus RAM and/or ROM
µPD946XX	Contains the same as µPD936XX but with ROM code change
µPD956XX	Same as µPD936XX but contains megafunction blocks, such as a 710XXX or V20H /V30HL
µPD966XX	Same as µPD956XX but with a ROM code change

Typical CB-C8 Package Marking



NEC: Company Mark
JAPAN: Origin
D93600: Part Number
R: Package Code
9315K1: Lot Number
◀: Pin Number 1 Index

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On-Chip Compiled Memory

RAM and ROM blocks can be custom compiled in the CB-C8 design environment. Up to 64 Kbits of high-speed, synchronous single port RAMs (including built-in MUX circuits for reliable production testing) can be compiled. Up to 256 Kbits of ROM can be compiled. For a 512 x 8 synchronous RAM, the access time is 7 nanoseconds.

NEC's RAMGEN and ROMGEN software allows ASIC designers to generate memory blocks of specific size and performance to suit their exact system requirements quickly.

The table below summarizes features of compiled memory blocks. For compiled, high-speed RAM, the minimum word depth is 32 and the minimum bit width is one (1). The word depth can increase by 16 words in increments up to 2K and the bit width can increase by 1 bit up to a maximum of 32 bits. The other RAM and ROM configurations are determined in the same fashion.

Table of Compilable RAM and ROM Available for CB-C8

Compiled Memory (High-Speed RAM)	Compiled Memory (ROM)
– Single port, synchronous operation – Operating voltage: 2.7 to 3.6 V – Test MUX used for Address and Data bus to facilitate BIST (Built-in Self Test) and external test – Battery back-up mode – Built-in power bus ring – Compilable range • 1 to 32 bit (1 bit increment) • 32 to 2k word (16 word increment) – Access time (512 word x 8 bit) : 7 ns max.	– Single port, asynchronous operation – Operating voltage: 2.7 to 3.6 V – Test MUX used with Address bus to facilitate BIST and external test – Metal-1 programmable – Built-in power bus ring – Compilable range • 4 to 64 bit (2 bit increment) • 128 to 8k word (128 word increment) – Access time: 25 ns max. (2k word x 16 bit)

Rambus™ ASIC Cell

The Rambus ASIC Cell (RAC) is specially designed for high-speed Rambus channel by Rambus, Inc. Rambus channel is configured by RAC and Rambus DRAM (RDRAM™) that can acheive up to 500M byte/sec data transmission.

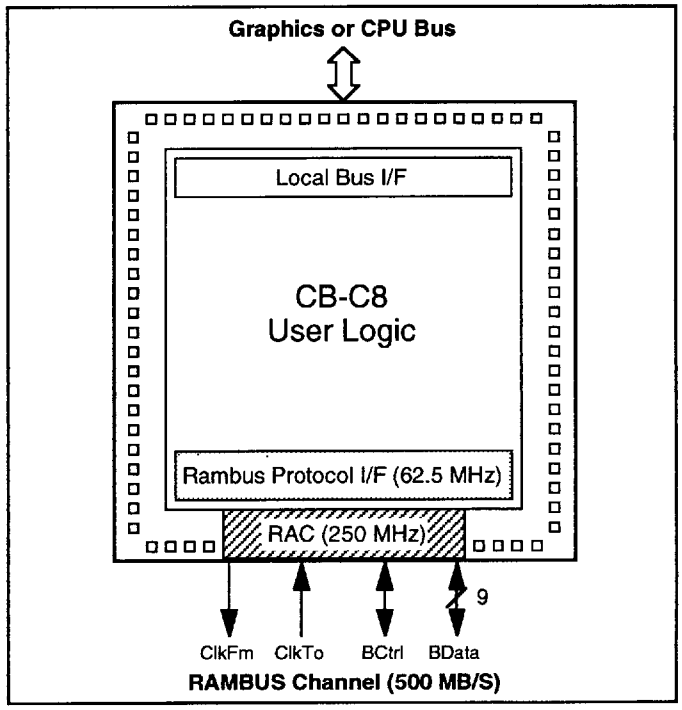
The RAC acts as an interface, or bridge between the system's microprocessor and the RDRAMs. Depending on the system architecture, designers can integrate up to four (4) RAC's into a CB-C8 design. The RAC interface on the ASIC requires only 32 pins.

The Rambus high-bandwidth solution can be used as high-end graphics, multimedia systems, ATM switching systems and PDAs.

Features:

- ❑ Highest memory bandwidth: 500M byte/sec/channel
- ❑ Minimum pin count: 32 pins per channel
- ❑ Reduced numbers of RDRAMs
- ❑ Fully integrated in CB-C8 design flow
- ❑ Built-in test capability

Figure 2. Rambus ASIC Cell



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Absolute Maximum Ratings

Power supply voltage, V_{DD}	–0.5 to +4.6 V
Input/output voltage, V_I / V_O	–0.5 V to V_{DD} + 0.5 V
Output current, I_O	
3.0-mA drive	10 mA
6.0-mA drive	20 mA
9.0-mA drive	30 mA
12.0-mA drive	40 mA
18.0-mA drive	60 mA
24.0-mA drive	80 mA
Operating temperature, T_{OPT}	–40 to +85°C
Storage temperature, T_{STG}	–65 to +150°C

Caution: Exposure to absolute maximum ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should not be operated outside the recommended operating conditions.

Input/Output Capacitance

$V_{DD} = V_I = 0$ V; f = 1 MHz

Terminal	Symbol	Typ	Max	Unit
Input	C_{IN}	10	20	pF
Output	C_{OUT}	10	20	pF
I/O	$C_{I/O}$	10	20	pF

Note:
(1) Values include package pin capacitance.

Power Consumption

Description	Limits (max)	Unit	Test Conditions
Internal cell	1.25	μW/MHz	F/O = 2; L = 2 mm
Input block	10	μW/MHz	F/O = 2; L = 2 mm
Output block	0.2	mW/MHz	C_L = 15 pF

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Power supply voltage	V_{DD}	3.0	3.6	V
Ambient temperature	T_A	–40	+85	°C
Low-level Input voltage (3 V Interface Block)	V_{IL}	0	0.3 V_{DD}	V
Low-level Input voltage (5 V Interface Block)	V_{IL}	0	0.8	V
High-level input voltage (3 V Interface Block)	V_{IH}	0.7 V_{DD}	V_{DD}	V
High-level input voltage (5 V Interface Block)	V_{IH}	2.2	5.5	V
Input rise or fall time	t_{RI}, t_{FI}	0	200	ns
Input rise or fall time, Schmitt	t_{RI}, t_{FI}	0	10	ms
Positive Schmitt-trigger voltage	V_P	1.2	2.4	V
Negative Schmitt-trigger voltage	V_N	0.6	1.8	V
Hysteresis voltage	V_H	0.3	1.5	V

Note: The rise/fall time given for a Schmitt trigger input buffer varies depending on the operating environment. Simultaneous switching of output buffers should be analyzed before deciding to use a Schmitt trigger input buffer.

AC Characteristics

V_{DD} = 3.3 V ± 0.3 V; T_A = –40 to +85°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Toggle frequency	f_{TOG}	175			MHz	D-F/F; F/O = 2
Delay time, internal gate	t_{PD}		0.13		ns	F/O = 1; L = 0 mm
Delay time, power gate			0.22		ns	F/O = 2; L = 2 mm
Delay time, buffer						
Input	t_{PD}		0.36		ns	F/O = 2; L = 2 mm
Output	t_{PD}		1.46		ns	C_L = 15 pF
Output rise time (FO01)	t_R		1.88		ns	C_L = 15 pF
Output fall time (FO01)	t_F		1.32		ns	C_L = 15 pF

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DC Characteristics

V_{DD} = 3.3 V ± 0.3 V; T_A = −40 to +85°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Static Current Consumption (**Note 1**)	I_{DDS}			200	μA	$V_I = V_{DD}$ or GND B18 to H33 (**Note 2**)
				300		H72 to K90 (**Note 2**)
Off-State Output Current	I_{OZ}			TBD	μA	$V_O = V_{DD}$ or GND
Input Clamp Voltage (**Note 3**)	V_{IC}	TBD			V	
Output Short Circuit Current (**Note 4**)	I_{OS}	TBD			mA	
Input Leakage Current						
Normal Input	I_I		10^{-5}	10	μA	$V_I = V_{DD}$ or GND
50 kΩ pull-up	I_I		−66		μA	V_I = GND
5 kΩ pull-up	I_I		−660		μA	V_I = GND
50 kΩ pull-down	I_I		66		μA	$V_I = V_{DD}$
Low-Level Output Current						
Normal Output						
3 mA	I_{OL}	3.0			mA	V_{OL} = 0.4 V
6 mA	I_{OL}	6.0			mA	V_{OL} = 0.4 V
9 mA	I_{OL}	9.0			mA	V_{OL} = 0.4 V
12 mA	I_{OL}	12.0			mA	V_{OL} = 0.4 V
18 mA	I_{OL}	18.0			mA	V_{OL} = 0.4 V
24 mA	I_{OL}	24.0			mA	V_{OL} = 0.4 V
5 V I/F BUFF						
3 mA	I_{OL}	3.0			mA	V_{OL} = 0.4 V
6 mA	I_{OL}	6.0			mA	V_{OL} = 0.4 V
9 mA	I_{OL}	9.0			mA	V_{OL} = 0.4 V
High-Level Output Current						
Normal Output						
3 mA	I_{OH}	−3.0			mA	V_{OH} = 2.4 V
6 mA	I_{OH}	−6.0			mA	V_{OH} = 2.4 V
9 mA	I_{OH}	−9.0			mA	V_{OH} = 2.4 V
12 mA	I_{OH}	−12.0			mA	V_{OH} = 2.4 V
18 mA	I_{OH}	−18.0			mA	V_{OH} = 2.4 V
24 mA	I_{OH}	−24.0			mA	V_{OH} = 2.4 V
5 V I/F BUFF						
3 mA	I_{OH}	−3.0			mA	V_{OH} = 2.4 V
6 mA	I_{OH}	−3.0			mA	V_{OH} = 2.4 V
9 mA	I_{OH}	−3.0			mA	V_{OH} = 2.4 V
Low-Level Output Voltage						
3 V Interface Block	V_{OL}			0.1	V	I_{OL} = 0 mA
5 V Interface Block	V_{OL}			0.1	V	I_{OL} = 0 mA
High-Level Output Voltage						
3 V Interface Block	V_{OH}	V_{DD}−0.1		0.1	V	I_{OH} = 0 mA
5 V Interface Block	V_{OH}	V_{DD}−0.2		0.1	V	I_{OH} = 0 mA

Notes: 1. When using interface blocks with pull-up/pull-down resistors or oscillation circuits, the static current consumption increases.

2. Step size.

3. Input clamp voltage V_{IC} means the voltage is clamped when the input signal is negative. In the case of under-shooting or ringing of input signal, input signal is clamped at this voltage.

4. Output short-circuit current should be within one (1) second, for one (1) pin of LSI.

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Package Options

Type	Pin #	Pitch (mm)	Body (mm)	B18 88	B57 104	B97 120	C37 136	C76 152	D16 168	D55 184	D75 192	E15 208	E54 224	E94 240	F34 256	F74 272	G14 288	G53 304	G93 320	H33 336	H72 352	J32 376	J71 392	K11 408	K90 440
QFP	44	0.8	10x10	A	A	A	P	P	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	52	1	14x14	P	P	P	P	P	P	P	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	64	1	14x20	P	P	A	A	P	P	P	P	A	P	P	P	-	-	-	-	-	-	-	-	-	-
	80	0.8	14x20	A	A	L	A	P	P	P	A	A	P	P	P	-	-	-	-	-	-	-	-	-	-
	100	0.65	14x20	-	A	A	A	A	A	A	P	P	A	P	P	-	-	-	-	-	-	-	-	-	-
	120	0.8	28x28	-	-	A	A	A	A	A	A	A	A	A	A	A	P	A	A	A	A	P	-	-	-
	136	0.65	28x28	-	-	P	A	A	P	A	A	A	A	A	P	A	A	P	A	A	A	A	-	-	-
	160	0.65	28x28	-	-	-	-	-	A	A	A	A	P	A	A	A	A	A	A	A	A	A	A	P	A
	160*	0.65	28x28	-	-	-	-	-	-	-	P	P	A	P	P	P	P	P	P	P	P	P	P	P	P
	184*	0.65	32x32	-	-	-	-	-	-	-	-	-	-	-	P	P	P	P	P	P	P	P	P	P	P
	208	0.65	40x40	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	A	A	P	A
QFP (FP)	100	0.5	14x14	-	A	P	A	A	A	A	A	A	A	A	P	A	-	-	-	-	-	-	-	-	-
	120	0.5	20x20	-	-	A	P	A	A	A	A	P	A	P	P	P	A	P	P	P	P	-	-	-	-
	144	0.5	20x20	-	-	-	P	P	A	A	A	A	A	A	P	P	A	P	A	A	P	-	-	-	-
	160	0.5	24x24	-	-	-	-	-	A	A	P	A	A	A	A	P	A	P	A	A	P	P	A	P	A
	176	0.5	24x24	-	-	-	-	-	P	P	A	A	A	P	P	P	P	P	P	P	P	P	P	P	P
	176*	0.5	24x24	-	-	-	-	-	-	-	-	-	P	P	P	P	P	P	P	P	P	P	P	P	P
	208	0.5	28x28	-	-	-	-	-	-	-	-	-	A	A	A	P	A	A	A	A	A	A	P	P	A
	208*	0.5	28x28	-	-	-	-	-	-	-	-	-	A	P	P	P	P	P	P	P	P	P	P	P	P
	240*	0.5	32x32	-	-	-	-	-	-	-	-	-	-	-	-	-	P	P	P	P	P	P	P	P	P
	256*	0.4	28x28	-	-	-	-	-	-	-	-	-	-	-	-	-	P	P	P	P	P	P	P	P	P
	272*	0.5	36x36	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	P	P	P	P
	304*	0.5	40x40	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	P	P
QFP (HS)	160*	0.65	28x28	-	-	-	-	-	-	-	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
	160*	0.5	24x24	-	-	-	-	-	-	-	P	P	P	P	P	P	P	P	P	P	P	-	-	-	-
	176*	0.5	24x24	-	-	-	-	-	-	-	-	-	P	P	P	P	P	P	P	P	P	-	-	-	-
	208*	0.5	28x28	-	-	-	-	-	-	-	-	-	-	-	-	-	P	P	P	P	P	P	P	P	P
	304*	0.5	40x40	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	A	P	P	P
TQFP	64*	0.5	10x10	P	P	P	P	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	80	0.5	12x12	P	P	A	P	P	P	P	A	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	100*	0.5	14x14	-	P	P	P	P	P	P	P	P	-	-	-	-	-	-	-	-	-	-	-	-	-
	120*	0.4	14x14	-	P	P	P	P	P	P	P	P	-	-	-	-	-	-	-	-	-	-	-	-	-
	144*	0.5	20x20	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PLCC	68	50	.95"x.95"	-	-	-	P	P	A	P	P	P	P	-	-	-	-	-	-	-	-	-	-	-	-
	84	50	1.05"x1.05"	-	-	-	P	P	P	P	P	A	A	-	-	-	-	-	-	-	-	-	-	-	-

A = Available P = Planned *Cu leadframe Note: Check with Design Center for availability.

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NEC's ASIC Design System

CB-C8 products are fully supported by the OpenCAD Design System™ of NEC, which merges the best of today's most powerful hardware and software design tools into a single unified ASIC design environment. This expanding design system integrates the industry-leading tools and NEC tools for complete front-end to back-end ASIC design. The tools perform schematic capture, logic synthesis, floorplanning, logic and timing simulation, layout, design and circuit rule check and memory compilation. By offering these tightly coupled and integrated CAD tools with a well developed design methodology, the time and expense usually associated with the development of semicustom devices is considerably reduced.

The design flow for the CB-C8 standard cell is shown below with the software tools needed for the major portions of the design process. All the tools are integrated under DEC's PowerFrame™. Schematic capture is provided by ViewLogic's ViewDraw™. Also, a high level behavioral language is offered in Synopsys' Design Compiler. Back-end place and route is performed by Cell3 Ensemble. One of the key benefits of the OpenCAD Design System™ is that post simulation sign-off can be accomplished at the customer's site because NEC offers designers use of three popular simulators, each with "golden simulator" status, namely Verilog®, System HILO®, and V-Sim™.

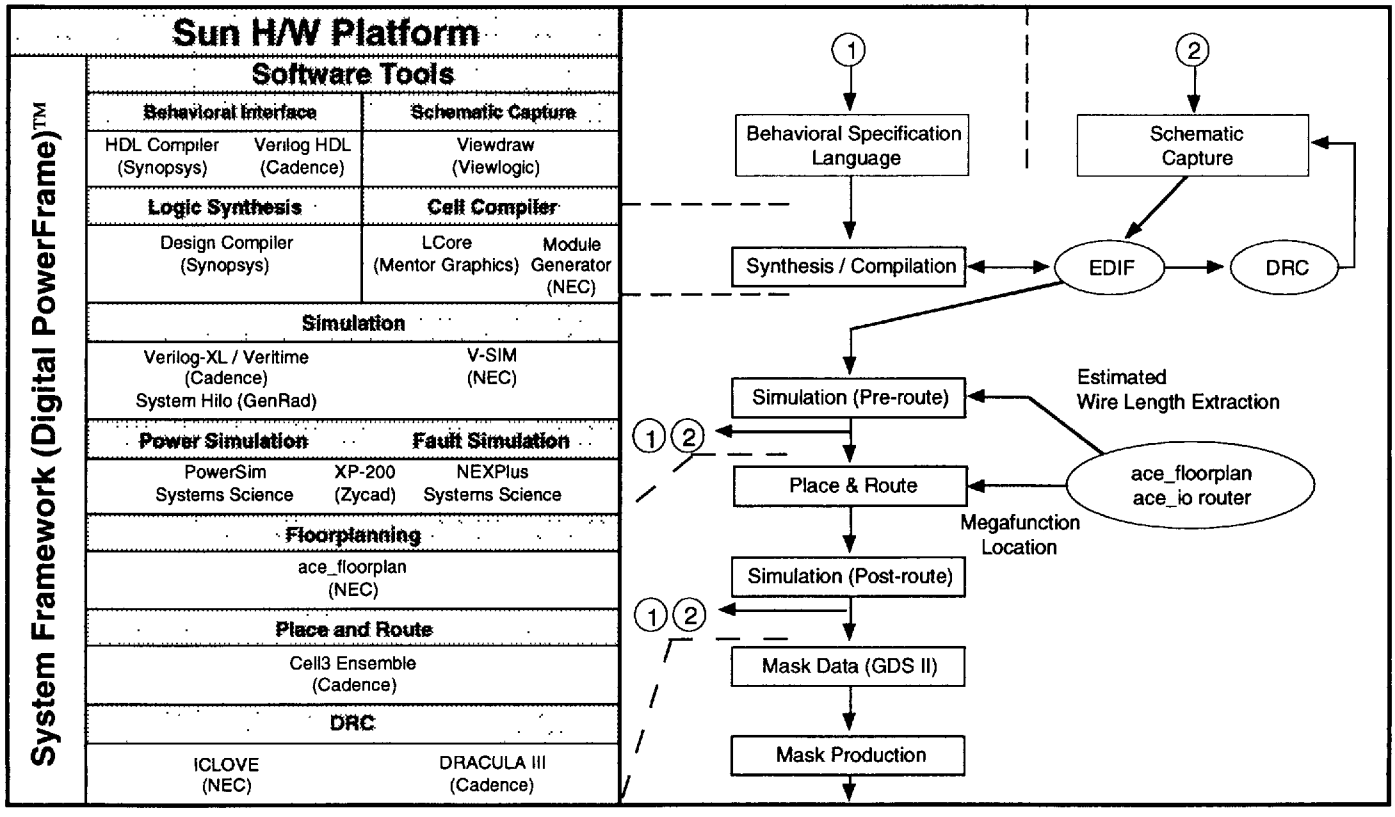
Simulation

Verilog gate level models are provided for each megafunction block, including the V20HL, V30HL CPU core for simulation purposes. An alternative for Verilog models is to use a hardware modeler simulation capability, where the actual stand-alone megafunction block, such as the V20HL, provides event-driven simulation in a variety of popular third-party CAE environments.

Testing

During the CB-C8 production test process, each megafunction used within a specfic customer design, is tested with NEC's production test vectors as well as test vectors provided by the customer. Each megafunction block must have one test input/output for each input/output or control pin on the megacell. These pins must all be accessible during production test. Compiled RAM and ROM use the same testing methodology.

Figure 3. CB-C8 Design Flow



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Cell Library List

The following is a preliminary list of the types of elements planned for the CB-C8 standard cell library. Many of the elements are in development and many more are planned. The names and functions of these blocks are designed to be compatible with those of the CB-C7 and CMOS-8/8L/8LCX families. Please contact your local NEC ASIC Design Center for the latest information on the availability of elements in the CB-C8 standard cell library.

Types of Primitive Cells

Function	High Speed	Low Power	High Density
Gate	43	18	24
Complex Gate	16	16	16
Parity	2	—	—
Adder	2	—	1
Decoder	3	3	1
Shift Register	4	3	—
Multiplexer	4	2	4
Latch	8	2	5
Flip-Flop	26	2	15
Counter	2	—	—
Comparator	1	—	—

I/O Buffers

	Interface Voltage	Input Type	Output Type	Output Drive (mA)	Pull-Up/Pull-Down	
Input	3 V	CMOS, CMOS-S	—	—	√	√
	5 V-Protected	CMOS, CMOS-S	—	—	√	√
Output	3 V	—	CMOS, CMOS-3S, Open-Drain	3, 6, 9, 12, 18, 24	√	√
	5 V-Protected	—	CMOS, CMOS-3S, Open-Drain	1, 2, 3, 6, 9	√	√
I/O	3 V	CMOS, CMOS-S	CMOS, CMOS-3S	3, 6, 9, 12, 18, 24	√	√
	5 V-Protected	CMOS, CMOS-S	CMOS, CMOS-3S	1, 2, 3, 6, 9	√	√

-S = Schmitt -3S = State

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