R/W Preamplifier for 3 Terminal Recording Heads, 2, 4, or 6 Channels

GENERAL DESCRIPTION

The XR-117 is a high speed head interface integrated circuit for hard disk drives, performing both read and write functions. The XR-117 is compatible with 3 1/2" to 14" single and multiple platter drives, and features high bandwidth, large dynamic range, and low noise. Several packaging options extend usefulness to applications requiring two, four, or six center-tapped read/write heads; multiple devices are easily cascaded for drives with more heads.

The XR-117R includes internal damping resistors, facilitating use in circuits requiring minimum external complexity and mass.

The XR-117, manufactured with a high speed bipolar process, operates on +5V and +12V.

FEATURES

Complete Head Interfacing Functions, Read and Write
High Bandwidth and Dynamic Range
Low Noise
Available in Two, Four, and Six Head Versions
Easily Cascaded for Larger Systems
Power Monitor
TTL Compatible Inputs

APPLICATIONS

Hard Disk Drives with MZG, ferrite, or composite heads

ABSOLUTE MAXIMUM RATINGS

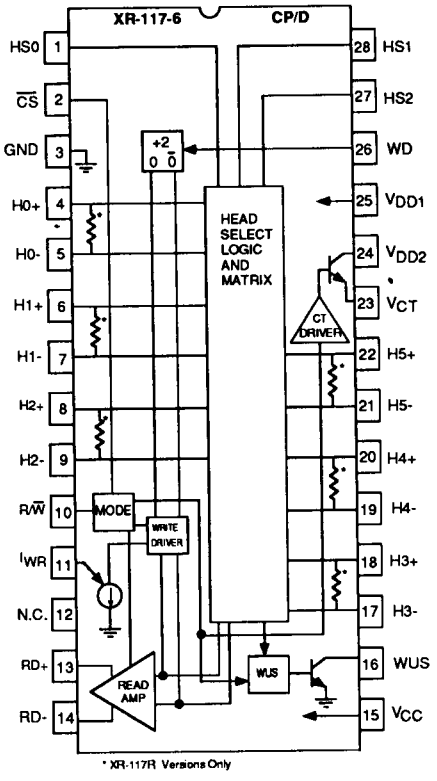
V_{DD1} and V_{DD2}	15 V
V_{CC}	6V
Digital Inputs	-0.3 V to V_{CC} +0.3 V
Write Current	60 mA
Junction Temperature	150°C
Storage Temperature	-65°C to +15°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-117-2CP	18 Pin Plastic	0°C to 70°C
XR-117-4CP	22 Pin Plastic	0°C to 70°C
XR-117-6CP	28 Pin Plastic	0°C to 70°C
XR-117-xD	Surface Mount	0°C to 70°C
XR-117-6CJ	28 Pin PLCC	0°C to 70°C
XR-117R-xCP	Plastic	0°C to 70°C
XR-117R-xD*	Surface Mount	0°C to 70°C
XR-117R-6CJ	28 Pin PLCC	0°C to 70°C

x = 2, 4 or 6, depending on number of heads required
** = contact factory for availability*

PIN ASSIGNMENT



SYSTEM DESCRIPTION

Four major blocks comprise the XR-117: a multiplexer for head selection, write data control circuitry, read signal amplifiers and buffers. Designed for six read/write heads, the XR-117 is also available in smaller packages for systems requiring only two or four heads. The 30 MHz minimum bandwidth facilitates data rates exceeding 25 Mbits per second.

Less than 1.3 nV/√Hz (typical) noise allows error free operation with small input signals. Up to 50 mA of write current output (user selectable) are available.

Cascading multiple XR-117s is accomplished by alternately enabling and disabling devices via the chip select ($\overline{CS}$) pin. Guaranteed write current tolerances allows close write matching between devices.

ELECTRICAL CHARACTERISTICS

Test Conditions: TA = 25°C VDD =12 V, VCC =5V, R_{IW} = 3.1 kΩ, L_h = 10µH, R_d =750Ω, CL (R_{D+},R_{D-}), ≤20_pF, 20 pF, Data Rate = 5 MHz, unless specified otherwise.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
DC CHARACTERISTICS						
I_{CC}	Supply Current			25 30	mA mA	V_{CC} = 5.5 V, Read or Idle Mode V_{CC} = 5.5 V, Write Mode
I_{DD}	Supply Current			25 50 30	mA mA mA	V_{DD} = 13.2 V, Idle Mode V_{DD} = 13.2 V, Read Mode V_{DD} = 13.2 V, Write Mode, I_W = 0 mA
P_D	Power Dissipation			400 600 700 1050	mW mW mW mW	V_{CC} - 5.5 V, V_{DD} = 13.2 V, Idle Mode Read Mode Write Mode, I_W = 50 mA, RCT = 130Ω Write Mode, I_W = 50 mA, RCT = 0Ω
V_{CT}	Center Tap Voltage		4.0 6.0		V V	Read Mode Write Mode
WUS V_{OL} I_{OH}	Write Unsafe Output Saturation Voltage Leakage Current		0.2	0.5 100	V µA	IOL = 8mA V_{OH}= 5 V
DIGITAL INPUTS						
V_{IL}	Input "Low" Voltage			0.8	V	
V_{IH}	Input "High" Voltage	2.0			V	
I_{IL}	Input Current, Low	-0.4			mA	
I_{IH}	Input Current, High			100	µA	
WRITE CHARACTERISTICS						
	Write Current Accuracy	-5		+5	%	Note 1
I_W	Recommended Write Current Range	10	45	50	mA	
	Differential Head Voltage Swing	5.7			Vpeak	
	Unselected Differential Head Current			2	mApeak	
C_O	Differential Output Capacitance			15	pF	
R_O	Differential Output Resistance	10 635	750	865	KΩ Ω	XR-117 XR-117R
	WD Rate (Transition Frequency)	125	500	625	kHz	WUS = Unsafe
K_1	Current Source Factor		20			K_1=I_W/(Current Through R_W)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
READ CHARACTERISTICS						
A_V	Differential Voltage Gain	80	100	120	V/V	V_{in} = 1 mVp-p @ 300 kHz $R_L+ = R_L- = 1K\Omega$
	Dynamic Range	-2		2	mV	DC input voltage where gain drops 10%. $V_{in} = V_i + 0.5$ mVp-p @ 300 kHz.
R_{in}	Differential Input Resistance	2	8		KΩ	XR-117
		500	675	850	Ω	XR-117R
C_{in}	Differential Input Capacitance			23	pF	f = 5 MHz
e_{ni}	Input Noise Voltage		1.3	2.1	nV/√Hz	L_h = 0, R_h = 0, BW = 15 MHz
BW	Bandwidth	30	60		MHz	-3dB point |Zs|< 5Ω, V_{in} = 1 mVp-p
I_B	Input Bias Current		10	45	µA	
CMRR	Common Mode Rejection Ratio	50	60		dB	$V_{CM} = V_{CT}$ + 100 mVp-p at 5 MHz
PSRR	Power Supply Rejection Ratio	45	60		dB	100 mVp-p at 5 MHz Superimposed on V_{DD1}, V_{DD2} or V_{CC}
	Channel Separation	45	60		dB	Unselected Channel: Vin = 100 mVp-p at 5 MHz. Selected Channel V_{in} = 0 V
	Output Offset Voltage	-480	±50	480	mV	
V_{CM}	Common Mode Output Voltage	5	6	7	V	
SWITCHING CHARACTERISTICS						
R/W	Read to Write		0.1	1	µs	Note 2 Write to Read
	Write to Read		0.1	1	µs	Note 3, Note 4
CS	Start-Up Delay		0.1	1	µs	Delay to 90% of IW or to 90% of 100 mV 10 MHz read signal envelope.
	Inhibit Delay		0.1	1	µs	Note 4
	Head Switching Delay		0.1	1	µs	Note 3, Switching between any heads.
WUS	Write Unsafe					
	Safe to Unsafe	1.6	2.5	8.0	µs	IW = 50 mA, See Figure 1, TD1
	Unsafe to Safe		0.2	1	µs	IW = 20 mA, See Figure 2, TD2
IW	Head Current					
	Propagation Delay		4	25	ns	L_h = 0µH, R_h = 0Ω, Note 5
	Asymmetry			2	ns	Note 6. See Figure 1, TD3
	Rise or Fall Time		9	20	ns	10% to 90% or 90% to 10% points

Note 1: Error from $I_W = \frac{140}{R_W} \frac{V}{(\Omega)}$

Note 2: Delay to 90% of I_W

Note 3: Delay to 90% of 100 mVp-p 10 MHz read single envelope

Note 4: Delay to 90% decay of I_W

Note 5: From 50% points

Note 6: Input WD has 50% duty cycle and 1 nS rise and fall times.

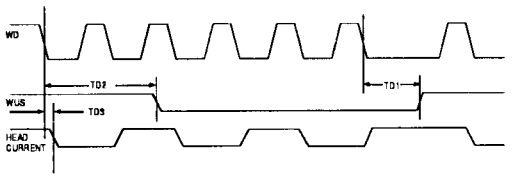


Figure 1. Write Mode Timing Diagram

CAUTION: This device may be damaged by electrostatic discharge. ESD precautions should be taken.

PRINCIPLES OF OPERATION

Write Mode

Before writing may begin, both chip select ($\overline{CS}$) and Read/Write (R/$\overline{W}$) must be pulled low. The desired head, selected by HS0 to HS2, is driven by a differential current sink of magnitude I_W set by R_{IW}. Input data is applied to a falling edge triggered toggle flip-flop, which in turn selects the active side of the center tapped write head.

Current is sourced through the center tap driver, V_{CT}, which is "high" in the write mode. Write unsafe (WUS) signals the disk controller whenever one of six error conditions exist and writing should be discontinued. The six faults are: open head, open center tap, no write current, write data frequency too low, device unselected, and writing attempted while the device is in the read mode.

Read Mode

Pulling R/$\overline{W}$ high enables the data readback mode. The head signal is amplified by a low noise differentiated stage and output by low impedance drivers.

APPLICATIONS INFORMATION

As with all high frequency, high gain systems, layout is critical. Lead lengths should be minimized and supplies should be well bypassed. The XR-117 is available in small outline surface mount and PLCC packages, facilitating installation near the drive heads. The XR-117R option has 750Ω internal damping resistors across each head input, further aiding the goal of short lead lengths by eliminating the need for external resistors. The XR-117R option is especially convenient when the device is mounted on the flexible cable connecting the heads, as internal damping resistors reduce layout complexity, parts counts, and mass.

The high frequency characteristics of the XR-117 lead to a certain degree of electrostatic discharge (ESD) susceptability, so static reducing precautions should be taken.

Write Mode Design Considerations

Write current, I_W, typically between 20 mA and 50 mA, is determined by a single resistor, R_{IW}.

$$R_{IW} = \frac{140{,}000}{I_W}$$

where I_W Is in mA and R_{IW} is in ohms.

The V_{CC} supply monitor disables writing when. V_{CC} drops below about 4V.

Device power dissipation is reduced by a resistor, R_{CT} connecting V_{DD2} to the +12 V supply. Some of the center tap driver voltage drop then is across the resistor.

With the nominal 12 V supply, R_{CT}, is calculated as

$$RCT = 130\left(\frac{55}{I_W}\right)$$

where R_{CT} is in ohms and I_W is in milliamperes.

Internal dissipation reduction is primarily a consideration with high write current levels and small outline packages. For low write currents, R_{CT} may be deleted, with V_{DD2} directly connected to the supply.

Write center tap circuitry is designed for higher stability than similar devices from other manufacturers. If extreme conditions exist, a ferrite bead around the V_{CT} line to the heads will reduce or eliminate overshoot and ringing.

Write unsafe (WUS) pulls high whenever one or more of six write error conditions exist. Four conditions; open head, open center tap, no write current and write data transition rate too low, are detected with a differential capacitor charge/discharge circuit. Device unselected and read mode digital conditions also force WUS high.

After removal of the fault condition, two negative write data transitions are required to clear WUS. This output is for indication only, intended for signaling a controller, and does not directly impede device operation. A pull-up resistor of about 2 KΩ to 10 KΩ is necessary for operation of this open collector output.

Read Mode Design Considerations

The read amp is fully differential input and output and provides approximately 100 V/V gain. Its 60 MHz bandwidth and low noise characteristics (1.3nV/ √Hz typical) provide substantial margins in most drives. The output should be AC coupled to delete the approximately 6 V output common mode voltage. Best results are obtained by limiting load capacitance to 20 pF and load current to 100 µA.

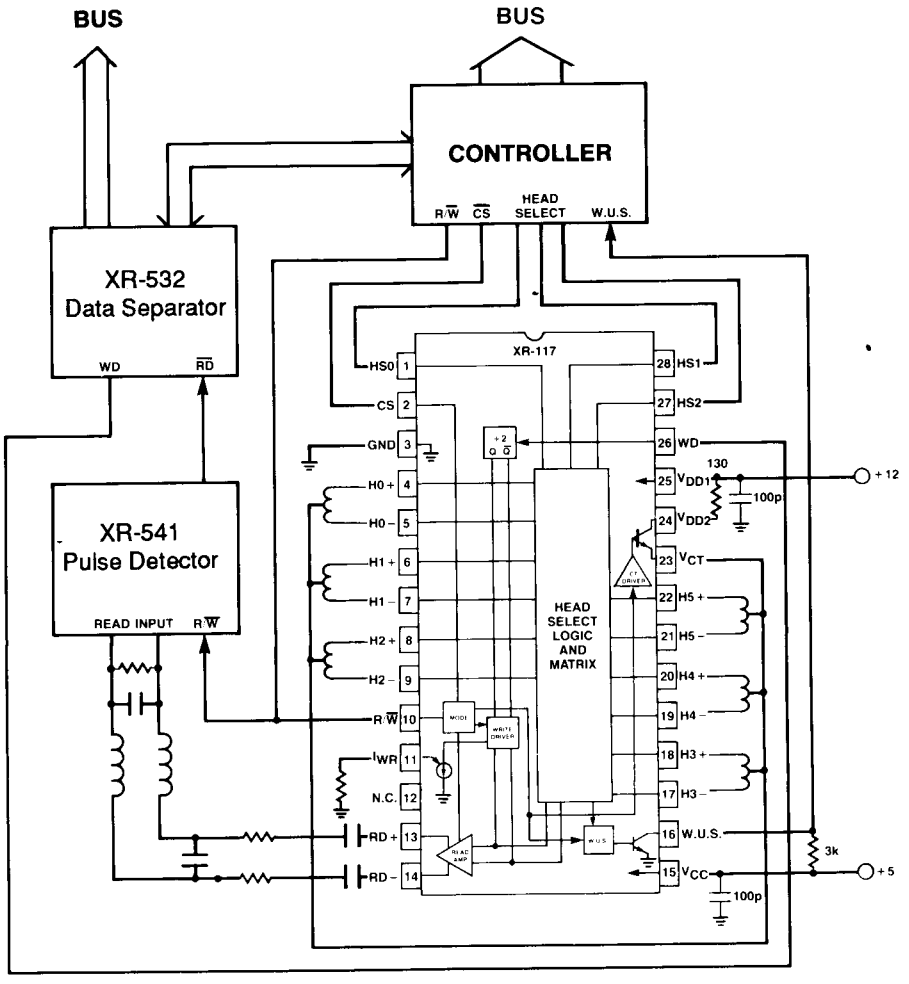


Figure 2. Hard Disk Read/Write Applications Circuit
Note: Circuit shown for XR-117R. Non-R versions require damping resistors across each head.

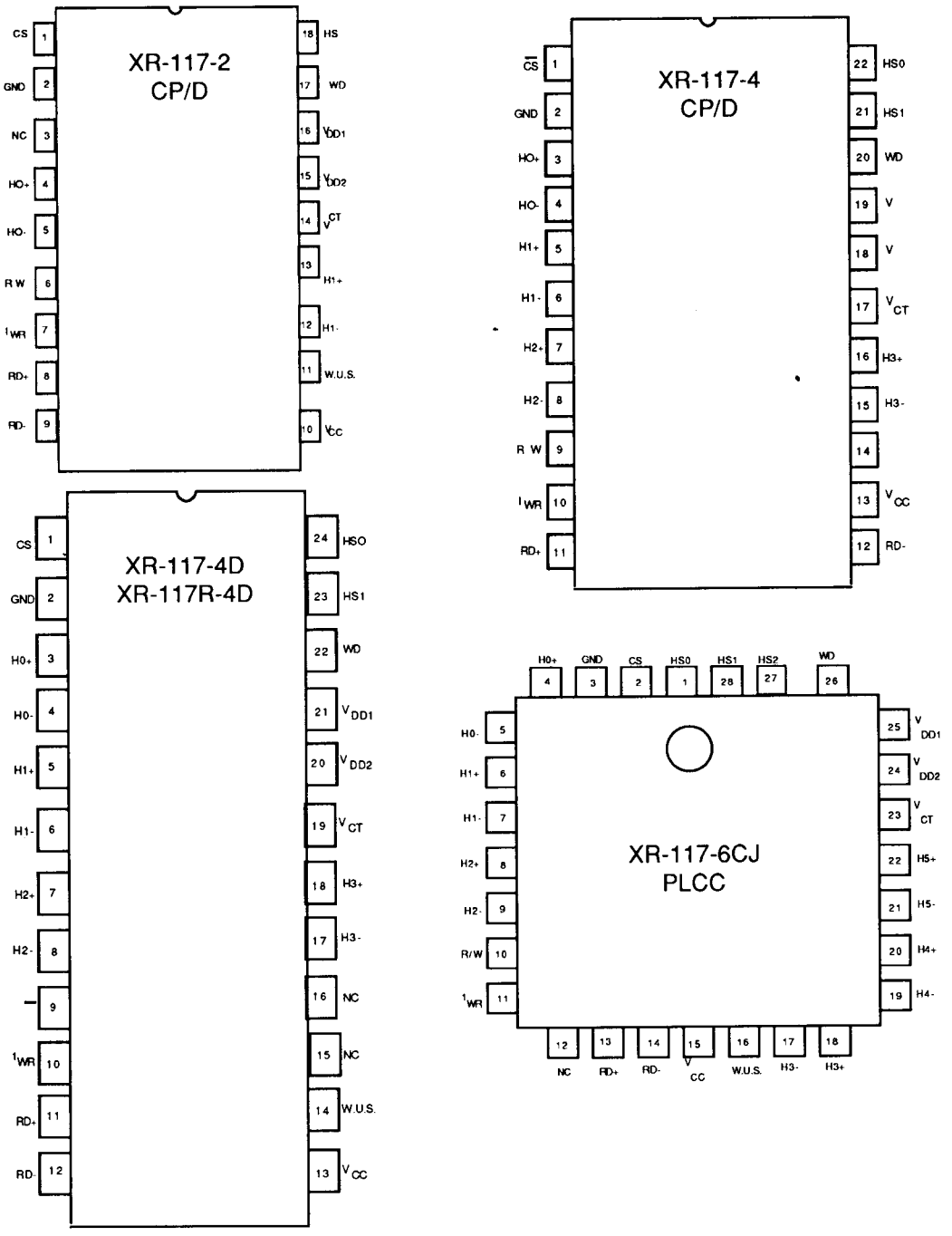


Figure 3. Additional Packages for XR-117(Six head DIP shown in Functional Block Diagram, page 1)