MOTOROLA

32K x 8 Bit Fast Static Random Access Memory:

ELECTRICALLY TESTED PER:
5962-88662

The 6206 is a 262,144 bit static random access memory organized as 32,768 words of 8 bits, fabricated using Motorola's third-generation high-performance silicon-gate CMOS (HCMOS IV) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

Chip enable ($\overline{E}$) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. In less than a cycle time after $\overline{E}$ goes high, the part automatically reduces its power requirements and remains in this low-power standby mode as long as $\overline{E}$ remains high. This feature provides significant system-level power savings.

The 6206 is packaged in a 600 mil, 28 pin ceramic dual-in-line package, and a 740 x 520 mil, 28 pin Flat Pack.

- Single 5.0 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Time — 35 ns Max.
- Low Power Dissipation
- Two Chip Controls: $\overline{E}$ for Automatic Power Down; $\overline{G}$ for Fast Access to Data
- Three State Outputs
- Fully TTL Compatible

6206

Commercial Plus and Mil/Aero Applications

AVAILABLE AS

1) JAN: N/A
2) SMD: 5962-88662
3) 883: 6206 - XX/BXAJC
X = CASE OUTLINE AS FOLLOWS:
PACKAGE: DIL: X
FP: Y

XX = Speed In ns
(35, 45, 55, 70, 100)

BURN-IN CONDITIONS:

V_{CC} = 5.0 V(min)/ 6.0 V(max), R_1 = 39.2 kΩ ± 20%, C_1 = 0.1 µF ± 20%,
V_H = 3.0 V(min)/5.0 V(max), V_L = – 0.5 V(min)/0.0 V(max),

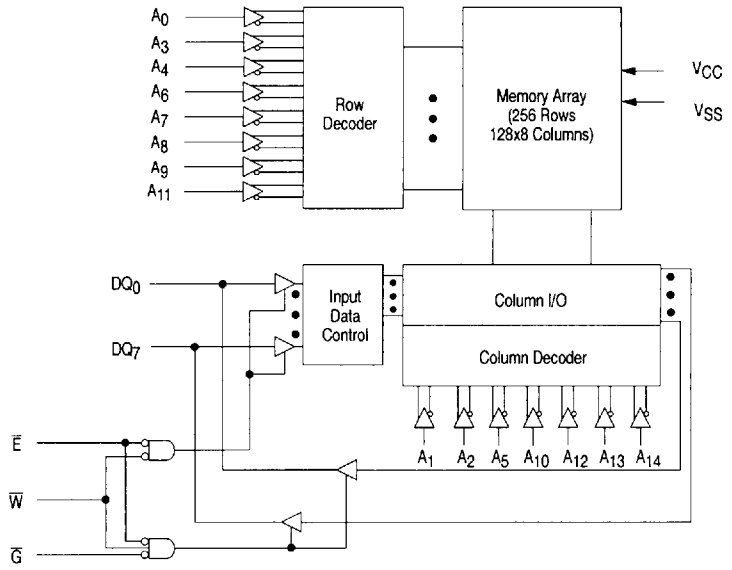
CP1:	100 KHz	CP6:	3.125 KHz	CP11:	97.66 Hz	CP16:	3.052 Hz
CP2:	50 KHz	CP7:	1.563 KHz	CP12:	48.83 Hz	CP17:	1.526 Hz
CP3:	25 KHz	CP8:	0.781 KHz	CP13:	24.41 Hz	CP18:	0.763 Hz
CP4:	12.5 KHz	CP9:	0.391 KHz	CP14:	12.21 Hz	CP19:	0.382 Hz
CP5:	6.25 KHz	CP10:	0.195 KHz	CP15:	6.104 Hz	CP20:	0.191 Hz

PIN NAME and FUNCTIONS

$A_0 - A_{14}$	Address Inputs
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$DQ_0 - DQ_7$	Data Input/Output
V_{CC}	+ 5.0 V Power Supply
V_{SS}	Ground
N.C.	No Connection

PIN ASSIGNMENTS			
Function	**DIL Case 719-01**	**FP Case 876-01**	**Burn-In (Condition-D)**
A_{14}	1	1	CP17
A_{12}	2	2	CP4
A_7	3	3	CP5
A_6	4	4	CP6
A_5	5	5	CP7
A_4	6	6	CP8
A_3	7	7	CP9
A_2	8	8	CP10
A_1	9	9	CP11
A_0	10	10	CP12
DQ_2	11	11	CP18 to R_1
DQ_1	12	12	CP18 to R_1
DQ_0	13	13	CP18 to R_1
V_{SS}	14	14	GND
DQ_3	15	15	CP18 to R1
DQ_4	16	16	CP18 to R1
DQ_5	17	17	CP18 to R_1
DQ_6	18	18	CP18 to R_1
DQ_7	19	19	CP18 to R_1
$\overline{E}$	20	20	CP2
A_{10}	21	21	CP13
$\overline{G}$	22	22	CP1
A_{11}	23	23	CP14
A_9	24	24	CP15
A_8	25	25	CP16
A_{13}	26	26	CP3
$\overline{W}$	27	27	CP1
V_{CC}	28	28	V_{CC}, C_1 to GND

BLOCK DIAGRAM



TRUTH TABLE					
$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	Supply	I/O Pin
H	X	X	Not Selected	I_{SB}	High Z
L	H	H	Output Disabled	I_{CC}	High Z
L	L	H	Read	I_{CC}	D_{OUT}
L	X	L	Write	I_{CC}	D_{IN}

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS: (See Note)			
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to +7.0	V
Voltage Relative to V_S for Any Pin Except V_{CC}	V_{IN}, V_{OUT}	– 0.5 to V_{CC} +5.0	V
Output Current (per I/O)	I_{OUT}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	–55 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Temperature Range	T_A	–55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = –55°C to +125°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS					
Parameters	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	–0.5*	—	0.8	V

* V_{IL} (min) = – 0.5 Vdc; V_{IL} (min) = – 2.0 Vac (pulse width ≤ 20 ns)

** V_{IH} (max) = V_{CC} + 0.3 Vdc; V_{IH} (max) = V_{CC} + 2.0 Vdc (pulse width ≤ 20 ns)

DC CHARACTERISTICS				
Parameters	**Symbol**	**Min**	**Max**	**Unit**
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	±10.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, or $\overline{G}$ = V_{IH}, V_{OUT} = 0 to 5.5 V)	$I_{lkg(O)}$	—	±10.0	µA
Power Supply Current ($\overline{E}$ = V_{IL}, V_{IN} = V_{IH}, or V_{IL}, I_{OUT} = 0), F = $1/t_{AVAV}$,				
35, 45, 55 µs	I_{CC}	—	150	mA
70, 100 µs	I_{CC}	—	105	mA
Standby Current ($\overline{E}$ = V_{IH}) (TTL Levels)	I_{SB1}	—	20	mA
Standby Current ($\overline{E}$ ≥ V_{CC} – 2.0 V) (CMOS Levels)	I_{SB2}	—	20	mA
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)				
Characteristics	**Symbol**	**Typ**	**Max**	**Unit**
Input Capacitance	C_{in}	6.0	11	pF
I/O Capacitance	$C_{I/O}$	8.0	11	pF

AC TEST LOADS OR EQUIVALENT

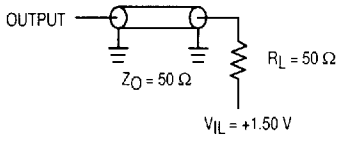


Figure 1A.

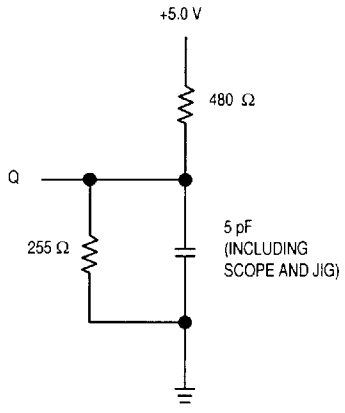


Figure 1B.

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = – 55°C to + 125°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level	1.5 V
Input Pulse levels	0 to 3.0 V
Input Rise/Falls Time	5.0 ns
Output Timing Measurement Reference Level	1.5 V
Output Load	See Figure 1

READ CYCLE 1 & 2 (See Note 1)

Parameters	Symbol	Alternate Symbol	6206-35		6206-45		6206-55		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	35	—	45	—	55	—	ns	—
Address Access Time	t_{AVQV}	t_{AA}	—	35	—	45	—	55	ns	—
$\overline{E}$ Access Time	t_{ELQV}	t_{AC}	—	35	—	45	—	55	ns	—
$\overline{G}$ Access Time	t_{GLQV}	t_{OE}	—	35	—	35	—	35	ns	—
Output Hold from Address Change	t_{AXQX}	t_{OH}	3	—	3	—	3	—	ns	2
Chip Enable to Output Low-Z	t_{ELQX}	t_{CLZ}	3	—	3	—	3	—	ns	2, 3
Output Enable to Output Low-Z	t_{GLQX}	t_{OLZ}	2	—	0	—	0	—	ns	2, 3
Chip Enable to Output High-Z	t_{EHQZ}	t_{CHZ}	0	35	0	35	0	35	ns	2, 3
Output Enable to Output High-Z	t_{GHQZ}	t_{OHZ}	0	35	0	35	0	35	ns	2, 3

READ CYCLE 1 & 2 (See Note 1)

Parameters	Symbol	Alternate Symbol	6206-70		6206-100		Unit	Notes
			Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	70	—	100	—	ns	—
Address Access Time	t_{AVQV}	t_{AA}	—	70	—	100	ns	—
$\overline{E}$ Access Time	t_{ELQV}	t_{AC}	—	70	—	100	ns	—
$\overline{G}$ Access Time	t_{GLQV}	t_{OE}	—	35	—	60	ns	—
Output Hold from Address Change	t_{AXQX}	t_{OH}	3	—	3	—	ns	2
Chip Enable to Output Low-Z	t_{ELQX}	t_{CLZ}	3	—	3	—	ns	2, 3
Output Enable to Output Low-Z	t_{GLQX}	t_{OLZ}	0	—	0	—	ns	2, 3
Chip Enable to Output High-Z	t_{EHQZ}	t_{CHZ}	0	35	0	35	ns	2, 3
Output Enable to Output High-Z	t_{GHQZ}	t_{OHZ}	0	35	0	35	ns	2, 3

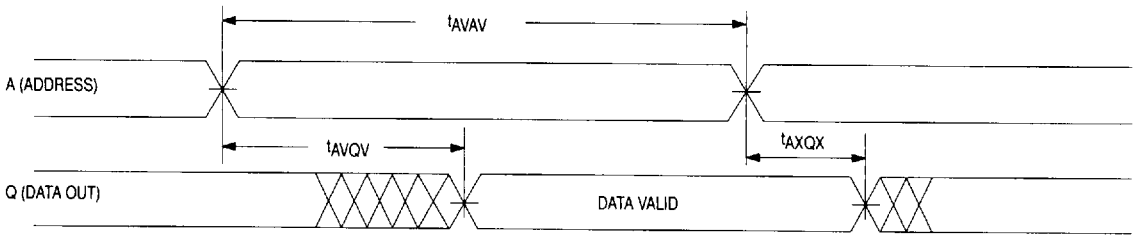
NOTES:
1. $\overline{W}$ is high at all times for read cycles.
2. All high-Z and low-Z parameters are considered in a high or low state when the output has made a 500 mV transition from the previous steady state voltage.
3. These parameters are periodically sampled and not 100% tested.

WRITE CYCLE 1 & 2 (See Note 1)										
Parameters			6206-35		6206-45		6206-55		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	35	—	45	—	55	—	ns	—
Address Setup to Write Low Address Setup to Enable Low	t_{AVWL} t_{AVEL}	t_{AS}	0	—	0	—	0	—	ns	2
Address Valid to Write High Address Valid to Enable High	t_{AVWH} t_{AVEH}	t_{AW}	30	—	40	—	50	—	ns	—
Data Valid to Write High Data Valid to Enable High	t_{DVWH} t_{DVEH}	t_{DW}	35	—	35	—	35	—	ns	—
Data Hold from Write High Data Hold from Enable High	t_{WHDX} t_{EHDX}	t_{DH}	3	—	3	—	3	—	ns	—
Write Recovery Time Enable Recovery Time	t_{WHAX} t_{EHAX}	t_{WR}	7	—	7	—	7	—	ns	2
Chip Enable to End of Write Enable Low to Enable High	t_{ELWH} t_{ELEH}	t_{CW}	30	—	40	—	50	—	ns	1
Write Pulse Width	t_{WLWH}	t_{WP}	30	—	35	—	40	—	ns	3
Write Low to Output High-Z	t_{WLQZ}	t_{WHZ}	—	35	—	35	—	35	ns	4, 5
Write High to Output Low-Z	t_{WHQX}	t_{WLZ}	3	—	3	—	3	—	ns	4, 5

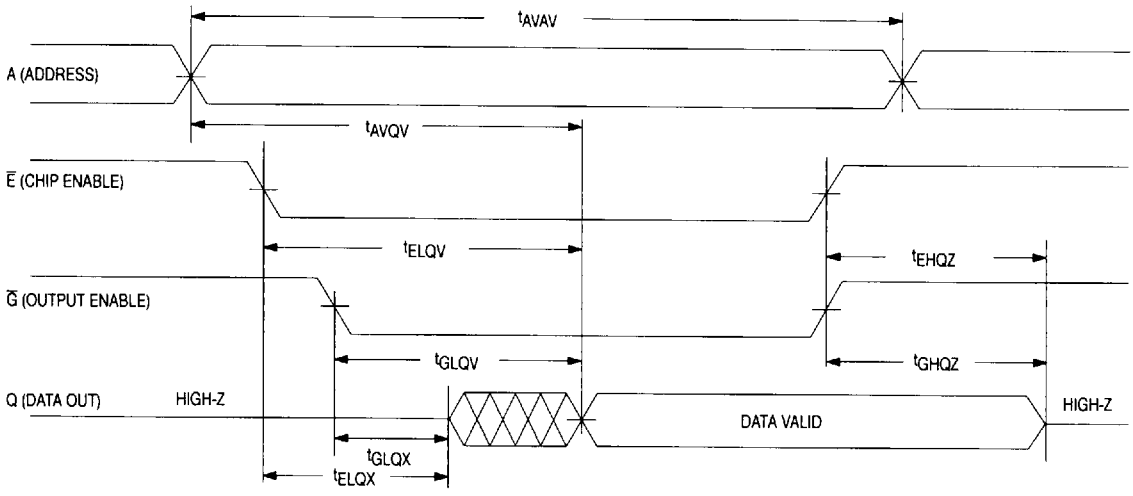
NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E}$ or low $\overline{W}$. A write cycle ends at the earliest transition of a high $\overline{E}$ or high $\overline{W}$.
2. $\overline{W}$ must be high during all address transitions.
3. If $\overline{G}$ is enabled, allow, an additional 15 ns t_{WLWH} to avoid bus contention.
4. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
5. These parameters are periodically sampled and not 100% tested.

WRITE CYCLE 1 & 2 (See Note 1)								
Parameters			6206-70		6206-100		Unit	Notes
			Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	70	—	100	—	ns	—
Address Setup to Write Low Address Setup to Enable Low	t_{AVWL} t_{AVEL}	t_{AS}	0	—	0	—	ns	2
Address Valid to Write High Address Valid to Enable High	t_{AVWH} t_{AVEH}	t_{AW}	60	—	85	—	ns	—
Data Valid to Write High Data Valid to Enable High	t_{DVWH} t_{DVEH}	t_{DW}	35	—	35	—	ns	—
Data Hold from Write High Data Hold from Enable High	t_{WHDX} t_{EHDX}	t_{DH}	3	—	3	—	ns	—
Write Recovery Time Enable Recovery Time	t_{WHAX} t_{EHAX}	t_{WR}	7	—	7	—	ns	2
Chip Enable to End of Write Enable Low to Enable High	t_{ELWH} t_{ELEH}	t_{CW}	60	—	90	—	ns	1
Write Pulse Width	t_{WLWH}	t_{WP}	45	—	55	—	ns	3
Write Low to Output High-Z	t_{WLQZ}	t_{WHZ}	—	35	—	50	ns	4, 5
Write High to Output Low-Z	t_{WHQX}	t_{WLZ}	3	—	3	—	ns	4, 5

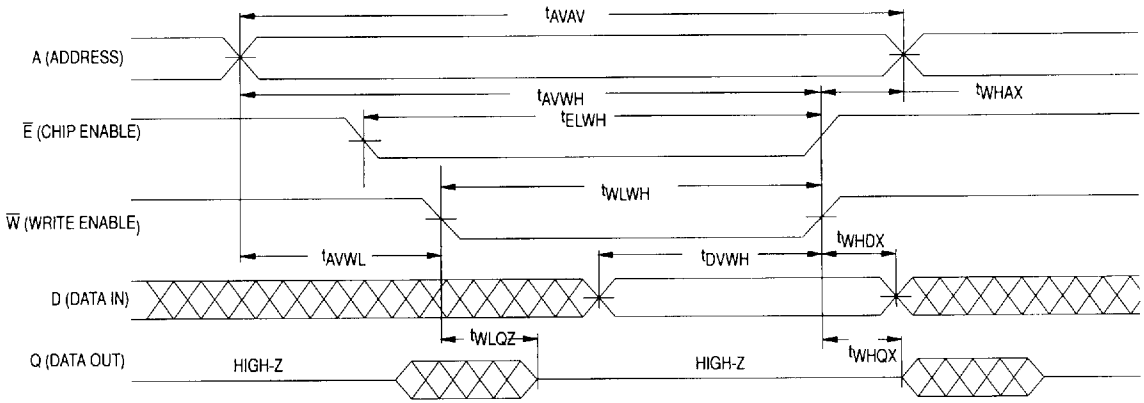
READ CYCLE 1 ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL})



READ CYCLE 2



WRITE CYCLE 1 ($\overline{W}$ Controlled)



WRITE CYCLE 2 ($\overline{E}$ Controlled)