PRODUCT BRIEF*

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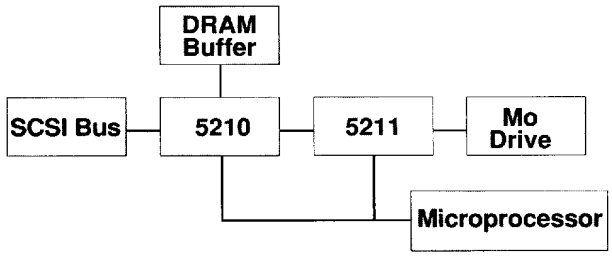
# AHA5210/5211

## MAGNETO-OPTICAL FORMATTER/CONTROLLER

The AHA5210/5211 provide a highly integrated, efficient chip set optimized for embedded controller applications for implementing an ISO JTC1/SC23 CD10090 (90mm) 3.5 inch Optical Drive. The controller fully supports the ANSI and ISO industry standard optical disk formats for CCS (Continuous Composite Servo). The high level of integration and the optimized pinout of the AHA5210/5211 make it suitable for embedded controller applications especially for 90mm drives where only limited board space is available.

The AHA5210 contains an NCR53C90A compatible SCSI block, full hardware "on-the-fly" error detection and correction, DRAM interface, a complete DMA controller, and 8 bit plus parity DMA like 4 Mbytes/second interface to the AHA5211. The AHA5211 contains the format specific circuitry for complete ISO compatibility. The AHA5211 will be folded into the AHA5210 in the next generation product. The AHA5210 and AHA5211, along with buffer memory, a data separator, and a local microprocessor with system ROM and RAM, provide a complete optical disk controller subsystem with high performance at a low cost. In addition it is possible to dramatically lower system power consumption by using the power down modes in the AHA5210/5211 chip set.




## FEATURES

- 3.5 inch MO disk ISO/ANSI standard support
- Full "on-the-fly" Reed Solomon error correction
- Addresses up to 4 Mbytes of DRAM
- Provides DRAM refresh, DRAM parity, and DRAM access from microprocessor
- Prearmable DMA controller
- Built-in single-ended bus transceiver (direct connection to SCSI bus)
- Integrated 48mA SCSI drivers
- Built-in parity checking and generation
- Programmable transfer counts
- Synchronous/asynchronous data transfers (synchronous transfer offset is programmable)
- SCSI-2 command support
- 16-byte SCSI FIFO
- Sustained data rates of 5.3 Mbytes/second for both synchronous and asynchronous modes
- NCR53C90A compatible SCSI controller
- Performs ISO 90mm (3.5 inch) compatible RLL (2,7) encoding/decoding and formatting
- Vendor unique bytes fully supported
- Max 32 MHz clock rate
- SYNC-RESYNC detection
- Preformatted ID reading
- Low power modes

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*Request the *AHA5210* Product Specification for complete details

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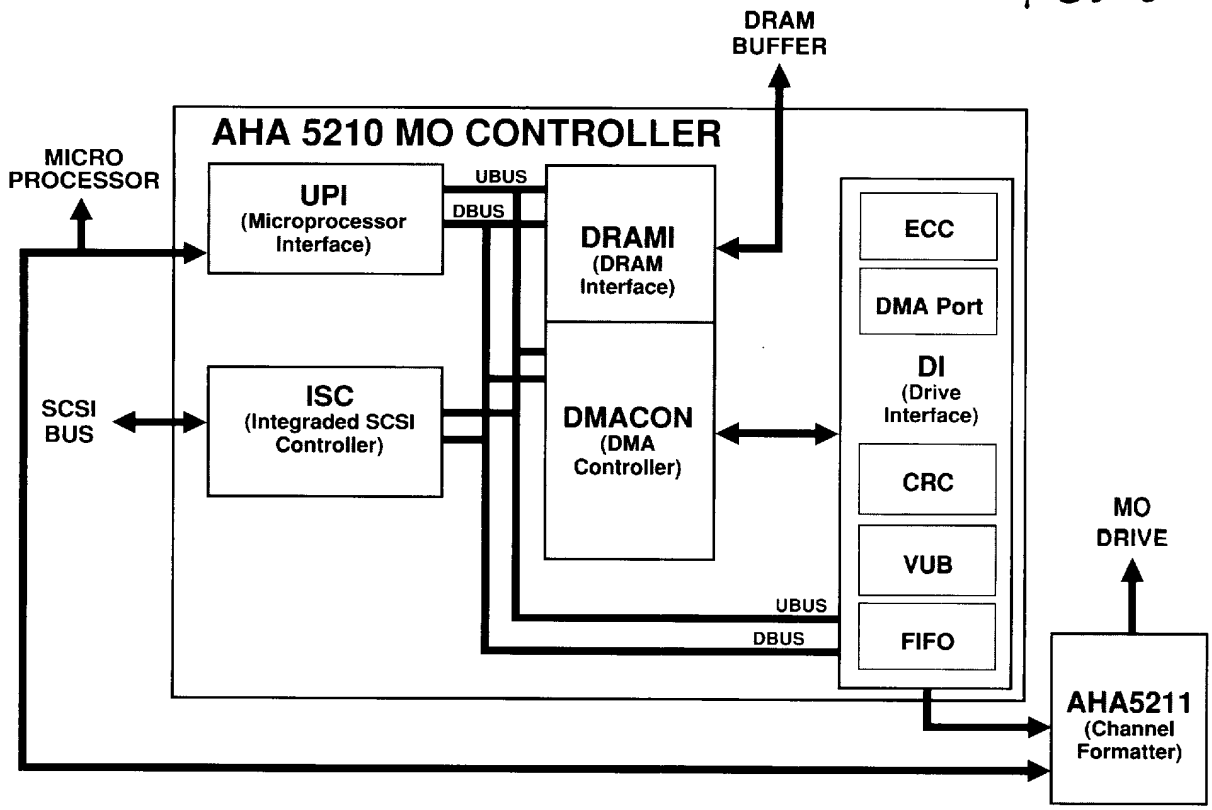


## FUNCTIONAL DESCRIPTION

The AHA5210/5211 are typically used in a system including 5210/5211, a data separator, buffer memory, and a local microprocessor with system ROM and RAM. The microprocessor may either be memory mapped or in the I/O space of the microprocessor. It communicates with the microprocessor via a multiplexed address and data path similar to that provided by Intel 80188 class of microprocessors. All controller functions are programmable by the microprocessor via read/write registers. This provides the maximum firmware control over drive operation to allow for various retry methods and other vendor unique requirements. Interrupts are designed for ease of access and simplified interrogation from the microprocessor.

An on-board SCSI interface is compatible with the NCR53C90A SCSI Controller and provides several speed enhancements to the NCR IC. All of the SCSI functions defined in the ANSI SCSI-2 standard are supported. Each of the SCSI operations are performed by the external microprocessor. Most of the common SCSI sequences are performed by a single microprocessor command. Each of the commands can be programmed to transfer data either between the SCSI bus, DRAM buffer, or to the microprocessor. In addition to SCSI-2 commands, the AHA5210 supports a 5.3 Mbyte/second SCSI data rate in both synchronous and asynchronous modes.

The on-board DRAM interface allows the AHA5210 to address up to 4 Megabytes of DRAM or SRAM and provides a low power mode that optionally allows the DRAM to continue to be refreshed. The AHA5210 can use 80ns/100ns/120ns DRAMS with very flexible programmable waveforms. The DRAM can be accessed via a microprocessor accessible register using an auto-increment address function.

The Reed Solomon error correction block works transparently to the microprocessor and performs all detection and correction of errors and provides statistics to the microprocessor via register access. It provides "on-the-fly" correction of all sector errors (including worst case errors) without loss of disk revolutions. This block capitalizes on the world leadership of AHA in high speed Reed Solomon error correction.

The internal DMA controller/buffer manager performs all calculations for internal DMAs. The internal DMA bus uses a token passing arbitration scheme to provide maximum DRAM buffer bandwidth utilization in addition to providing DRAM

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refreshes. The internal DMA subsystem is fully buffered allowing efficient transfer of data from the SCSI bus to and from DRAM, data transfers from the MO drive, error correction data from the ECC block to the DRAM, and microprocessor access to the DRAM.

The AHA5210 and the AHA5211 represent the first in a line of MO controller devices from AHA. AHA will continue to develop additional MO controllers, QIC formatters and controllers, data compression devices, SCSI controllers, and error correction devices that optimize firmware compatibility, maximize integration and minimize system cost. Custom versions can be provided.

AHA has a full line of Data Compression Devices, Reed Solomon CODECS, QIC (Quarter Inch Cartridge) formatters/controllers, and MO Controllers as well as a full complement of Full Custom VLSI designers.

## AHA5210 REGISTER ADDRESS MAP

| ADDRESS | REGISTER |
|---|---|
| 00X0 | SAA0-SCSI Active Address |
| 0x01 | SAA1-SCSI Active Address |
| 0x02 | SAA2-SCSI Active Address |
| 0x03 | DMAC-DMA Control |
| 0x04 | SAC0-SCSI Active Transfer Count |
| 0x05 | SACI-SCSI Active Transfer Count |
| 0x06 | SAC2-SCSI Active Transfer Count |
| 0x07 | DMAI-DMA Interrupts |
| 0x08 | SPA0-SCSI Pre-arm Address |
| 0x09 | SPA1-SCSI Pre-arm Address |
| 0x0A | SPA2-SCSI Pre-arm Address |
| 0x0B | UPC-Microprocessor Control |
| 0x0C | SPC0-SCSI Pre-arm Transfer Count |
| 0x0D | SPC1-SCSI Pre-arm Transfer Count |
| 0x0E | SPC2-SCSI Pre-arm Transfer Count |
| 0x0F | DMAM-DMA Interrupt Mask |
| 0x10 | DAA0-Drive Active Address |
| 0x11 | DAA1-Drive Active Address |
| 0x12 | DAA2-Drive Active Address |
| 0x13 | DWS-DRAM Wait States |
| 0x14 | DAC0-Drive Active Transfer Count |
| 0x15 | DAC1-Drive Active Transfer Count |
| 0x16 | DAC2-Drive Active Transfer Count |
| 0x17 | RC-DRAM Refresh Count |
| 0x18 | DPA0-Drive Pre-arm Address |
| 0x19 | DPA1-Drive Pre-arm Address |
| 0x1A | DPA2-Drive Pre-arm Address |
| 0x1B | RIC-Interface Configuration |
| 0x1C | DPC0-Drive Pre-arm Transfer Count |
| 0x1D | DPC1-Drive Pre-arm Transfer Count |

| ADDRESS | REGISTER |
|---|---|
| 0x1E | DPC2-Drive Pre-arm Transfer Count |
| 0x1F | RESERVED |
| 0x20 | UA0-Microprocessor Address |
| 0x21 | UA1-Microprocessor Address |
| 0x22 | UA2-Microprocessor Address |
| 0x23 | Microprocessor DMA Data |
| 0x24 | EC0-Error Threshold/Count Per Sector |
| 0x25 | EC1-Error Threshold/Count Per Interleave |
| 0x26 | Reserved |
| 0x27 | Reserved |
| 0x28 | VU0-Vendor Unique Byte 0 |
| 0x29 | VU1-Vendor Unique Byte 1 |
| 0x2A | VU2-Vendor Unique Byte 2 |
| 0x2B | VU3-Vendor Unique Byte 3 |
| 0x2C-2D | DICTRO,1-Drive Interface Control |
| 0x2E | DII-Drive Interface Interrupts |
| 0x2F | DIM-Drive Interface Interrupt Mask |
| 0x30 | RESERVED |
| 0x31 | RESERVED |
| 0x32 | ISCFIFO-FIFO Address for uP |
| 0x33 | ISCCOM-SCSI Command Register |
| 0x34 | ISCSTAT-SCSI Status/Destination ID |
| 0x35 | ISCINTR-SCSI Interrupt/Timeout Value |
| 0x36 | ISCSEQ-SCSI Sequencer/Sync. Period |
| 0x37 | ISCFFLG-SCSI FIFO Flag/Sync. Offset |
| 0x38 | ISCCNPQ1-SCSI Configuration1 |
| 0x39 | ISCCLKR-SCSI Clock Conversion Setter |
| 0x3A | ISCTEST-SCSI Test Mode Control |
| 0x3B | ISCCNFG2-SCSI Configuration 2 |
| 0x3C | Reserved |
| 0x3D | Reserved |
| 0x3E | Reserved |
| 0x3F | Full Powder Select |

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## AHA5211 PRELIMINARY REGISTER ADDRESS MAP

| ADDRESS | REGISTER |
|---|---|
| 0x40 | Command |
| 0x41 | Status1 |
| 0x42 | Status2 |
| 0x43 | Interrupt Mask |
| 0x44 | Start track number high |
| 0x45 | Start track number low |
| 0x46 | Start sector number |
| 0x47 | Transfer count |
| 0x48 | Current track number high |
| 0x49 | Current track number low |
| 0x4A | Current sector number |
| 0x4B | Transfer counter |
| 0x4C | Identify results |
| 0x4D | ID1 byte 1 |
| 0x4E | ID1 byte 2 |

| ADDRESS | REGISTER |
|---|---|
| 0x4F | ID1 byte 3 |
| 0x50 | ID1 byte 4 |
| 0x51 | ID1 byte 5 |
| 0x52 | ID2 byte 1 |
| 0x53 | ID2 byte 2 |
| 0x54 | ID2 byte 3 |
| 0x55 | ID2 byte 4 |
| 0x56 | ID2 byte 5 |
| 0x57 | ID3 byte 1 |
| 0x58 | ID3 byte 2 |
| 0x59 | ID3 byte 3 |
| 0x5A | ID3 byte 4 |
| 0x5B | ID3 byte 5 |
| 0x5C | Configuration 1 |
| 0x5D | Configuration 2 |

## TECHNICAL PUBLICATION

| DOCUMENT # | DESCRIPTION |
|---|---|
| PS5210 | AHA5210/5211 Product Specification |
| PS5101 | AHA5101 Product Specification |
| PS5121 | AHA5121 Product Specification |
| ANMO01 | MO Controller Design Techniques Using the AHA5210/5211 |
| ANMO02 | Programming the AHA5210/5211 |
| ANMO03 | Customizing the AHA5210 for ISO Applications |
| GLGEN1 | General Glossary of Terms |

## ORDERING INFORMATION

| PART NUMBER | DESCRIPTION |
|---|---|
| AHA5210A-032 PQC | Magneto Optical Formatter/Controller |
| AHA5211A-032 PQC | Encoder/Decoder |

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