Integrated Device Technology, Inc.

32K x 18
16K x 18
CEMOS™ PARALLEL
IN-OUT FIFO MODULE

IDT7MP2009
IDT7MP2010

FEATURES:

- First-In/First-Out memory module
- 32K x 18 organization (IDT7MP2009)
- 16K x 18 organization (IDT7MP2010)
- High speed: 15ns (max.) access time
- Separate upper and lower 9-bit XI and XO
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- MASTER/SLAVE multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and Full warning-flags
- High-performance CEMOS™ technology
- Single 5V (±10%) power supply

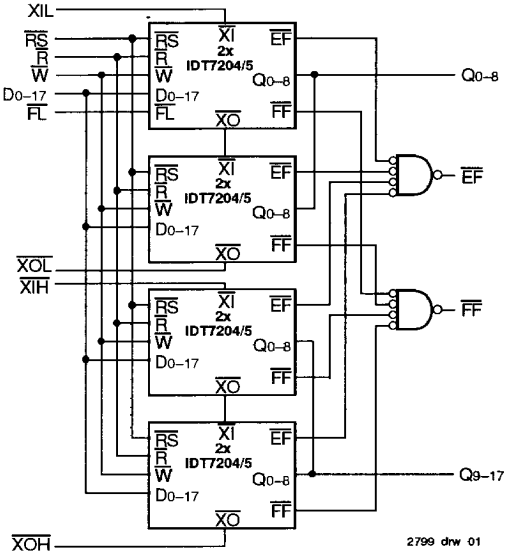
DESCRIPTION:

IDT7MP2009/7MP2010 are FIFO memory modules constructed on multi-layered epoxy laminate (FR-4) substrate by mounting eight IDT7205 (8K x 9) or IDT7204 (4K x 9) FIFOs in plastic leaded chip carriers. Extremely high speeds are achieved in this fashion due to the use of IDT7205s and IDT7204s fabricated in IDT's high performance CEMOS technology. These devices utilize a algorithm that loads and empties data on a first-In/first-out basis. The device uses Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

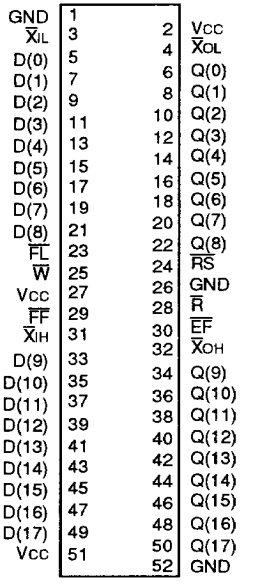
The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the WRITE (W) and READ (R) pins. The devices have a read/write cycle time of 25ns (min.) for commercial temperature ranges.

The devices utilize a 18-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



ZIP
TOP VIEW

2799 drw 02

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PIN NAMES

$\overline{W}$	Write
$\overline{R}$	Read
$\overline{RS}$	Reset
$\overline{FL}$	First Load
D_{0-17}	$DATA_{IN}$
Q_{0-17}	$DATA_{OUT}$
$\overline{X}IH$, $\overline{X}IL$	Expansion In (High Bit, Low Bit)
$\overline{X}OH$, $\overline{X}OL$	Expansion Out (High Bit, Low Bit)
$\overline{FF}$	Full Flag
$\overline{EF}$	Empty Flag
V_{CC}	Power
GND	Ground

2799 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH} (1)	Input High Voltage Commercial	2.0	—	—	V
V_{IL} (1)	Input Low Voltage Commercial	—	—	0.8	V

NOTE: 2799 tbl 03
1. 1.5V undershoots are allowed for 10ns once per cycle.

CAPACITANCE (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	80	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	120	pF

NOTE: 2799 tbl 02
1. This parameter is guaranteed by design but not tested.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 2799 tbl 01
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	IDT7MP2010 Min.	IDT7MP2010 Max.	IDT7MP2009 Min.	IDT7MP2009 Max.	Unit
$\|I_{LI}\|$(1)	Input Leakage Current (Any Input)	—	20	—	20	µA
$\|I_{OL}\|$(2)	Output Leakage Current	—	80	—	80	µA
V_{OH}	Output Logic "1" Voltage I_{OUT} = –2mA	2.4	—	2.4	—	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 8mA	—	0.4	—	0.4	V
I_{CC1}(3)	Operating Current	—	1280	—	1200	mA
I_{CC2}(3)	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}$/$\overline{RT}$ = V_{IH})	—	125	—	115	mA
I_{CC3}(3)	Power Down Current (All Input = V_{CC} – 0.2V)	—	65	—	65	mA

2799 tbl 05

NOTES:
1. Measurements with 0.4 ≤ VIN ≤ VOUT.
2. R ≥ VIH, 0.4 ≤ VOUT ≤ VCC.
3. Icc measurements are made with outputs open.

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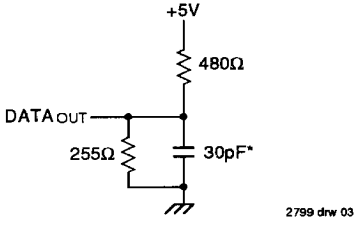
AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1 & 2

2799 tbl 06



* Includes scope and jig capacitances.

Figure 1. Output Load
*** Includes scope and jig capacitances.**

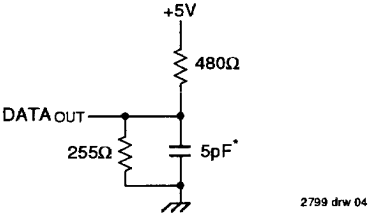


Figure 2. Output Load
(for tRLZ, tWLZ, and tRHZ)

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

		7MP2009SxxZ, 7MP2010SxxZ										
		-15[3]		-20[3]		-25		-30		-35		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
tRC	Read Cycle Time	25	—	30	—	35	—	40	—	45	—	ns
tA	Access Time	—	15	—	20	—	25	—	30	—	35	ns
tRR	Read Recovery Time	10	—	10	—	10	—	10	—	10	—	ns
tRPW[1]	Read Pulse Width	15	—	20	—	25	—	30	—	35	—	ns
tRLZ[2]	Read Pulse Low to Data Bus at Low Z	5	—	5	—	5	—	5	—	5	—	ns
tWLZ[2]	Write Pulse High to Data Bus at Low Z	5	—	5	—	5	—	10	—	10	—	ns
tDV	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	5	—	ns
tRHZ[2]	Read Pulse High to Data Bus at High Z	—	15	—	13	—	20	—	20	—	20	ns
tWC	Write Cycle Time	25	—	30	—	35	—	40	—	45	—	ns
tWPW[1]	Write Pulse Width	15	—	20	—	25	—	30	—	35	—	ns
tWR	Write Recovery Time	10	—	10	—	10	—	10	—	10	—	ns
tDS	Data Set-up Time	11	—	15	—	18	—	18	—	20	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tRSC	Reset Cycle Time	25	—	30	—	35	—	40	—	45	—	ns
tRS[1]	Reset Pulse Width	15	—	20	—	25	—	30	—	35	—	ns
tRSR	Reset Recovery Time	10	—	10	—	10	—	10	—	10	—	ns
tEFL	Reset to Empty Flag Low	—	25	—	30	—	35	—	40	—	45	ns
tREF	Read Low to Empty Flag Low	—	17	—	20	—	25	—	30	—	35	ns
tRFF	Read High to Full Flag High	—	20	—	23	—	25	—	30	—	35	ns
tWEF	Write High to Empty Flag High	—	20	—	23	—	25	—	30	—	35	ns
tWFF	Write Low to Full Flag Low	—	17	—	20	—	25	—	30	—	35	ns

2799 tbl 07

NOTES:
1. Pulse widths less than minimum value are not allowed.
2. This parameter is guaranteed by design but not tested.
3. Preliminary specifications only.

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AC ELECTRICAL CHARACTERISTICS

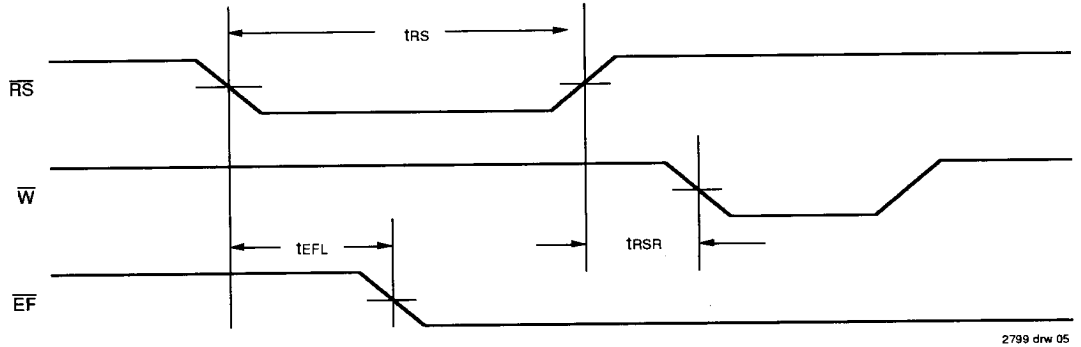
(V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	7MP2009SxxZ, 7MP2010SxxZ								Unit
		-40		-50		-60		-70		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	50	—	65	—	75	—	85	—	ns
t_A	Access Time	—	40	—	50	—	60	—	70	ns
t_{RR}	Read Recovery Time	10	—	15	—	15	—	15	—	ns
t_{RPW}[1]	Read Pulse Width	40	—	50	—	60	—	70	—	ns
t_{RLZ}[2]	Read Pulse Low to Data Bus at Low Z	5	—	10	—	10	—	10	—	ns
t_{WLZ}[2]	Write Pulse High to Data Bus at Low Z	10	—	15	—	15	—	15	—	ns
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	ns
t_{RHZ}[2]	Read Pulse High to Data Bus at High Z	—	25	—	30	—	30	—	30	ns
t_{WC}	Write Cycle Time	50	—	65	—	75	—	85	—	ns
t_{WPW}[1]	Write Pulse Width	40	—	50	—	60	—	70	—	ns
t_{WR}	Write Recovery Time	10	—	15	—	15	—	15	—	ns
t_{DS}	Data Set-up Time	20	—	30	—	30	—	30	—	ns
t_{DH}	Data Hold Time	0	—	5	—	5	—	10	—	ns
t_{RSC}	Reset Cycle Time	50	—	65	—	75	—	85	—	ns
t_{RS}[1]	Reset Pulse Width	40	—	50	—	60	—	70	—	ns
t_{RSR}	Reset Recovery Time	10	—	15	—	15	—	15	—	ns
t_{EFL}	Reset to Empty Flag Low	—	50	—	65	—	75	—	85	ns
t_{REF}	Read Low to Empty Flag Low	—	40	—	50	—	60	—	70	ns
t_{RFF}	Read High to Full Flag High	—	40	—	50	—	60	—	70	ns
t_{WEF}	Write High to Empty Flag High	—	40	—	50	—	60	—	70	ns
t_{WFF}	Write Low to Full Flag Low	—	40	—	50	—	60	—	70	ns

2799 tbl 08

NOTES:
1. Pulse widths less than minimum value are not allowed.
2. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF RESET CYCLE[1,2]



2799 drw 05

NOTES:
1. $t_{RSC} = t_{RS} + t_{RSR}$
2. $\overline{W}$ and $\overline{R}$ = V_{IH} during RESET.

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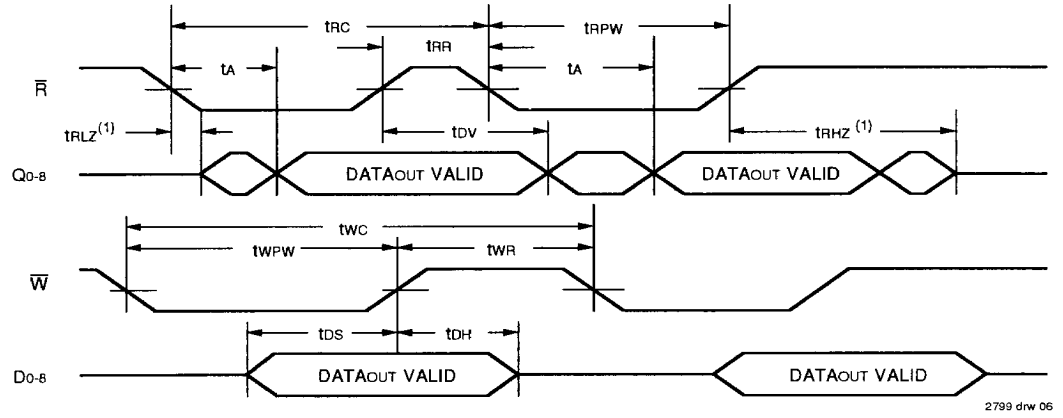
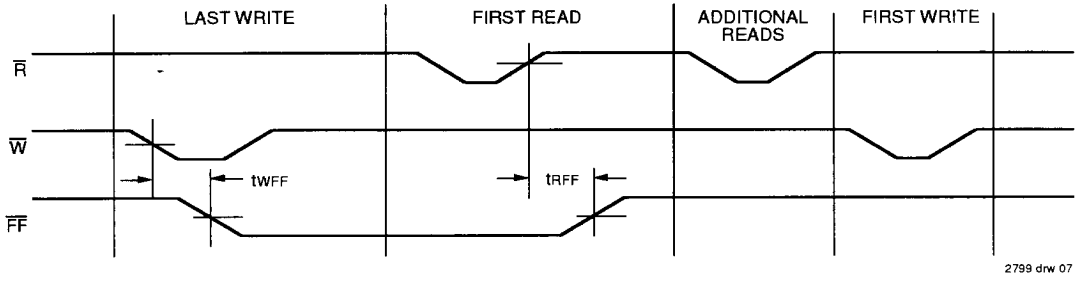
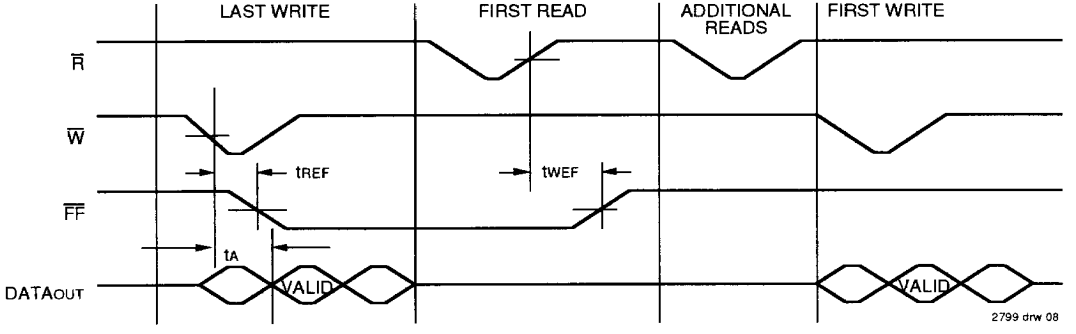
TIMING WAVEFORM OF ASYNCHRONOUS WRITE AND READ OPERATION



TIMING WAVEFORM FOR THE FULL FLAG FROM LAST WRITE TO FIRST READ



TIMING WAVEFORM FOR THE EMPTY FLAG FROM LAST READ TO FIRST WRITE(1)



NOTE:
1. This parameter is guaranteed by design but not tested.

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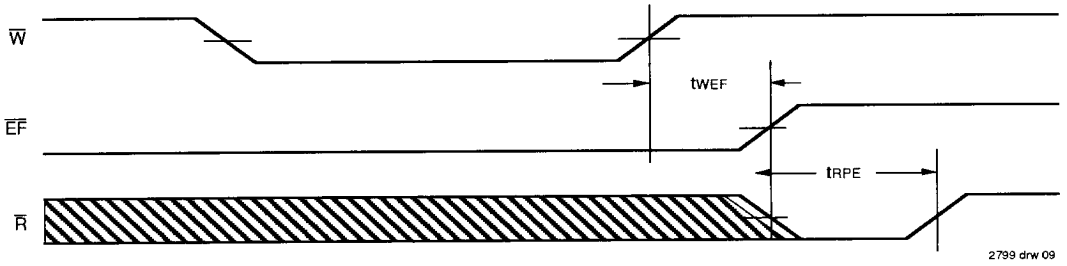
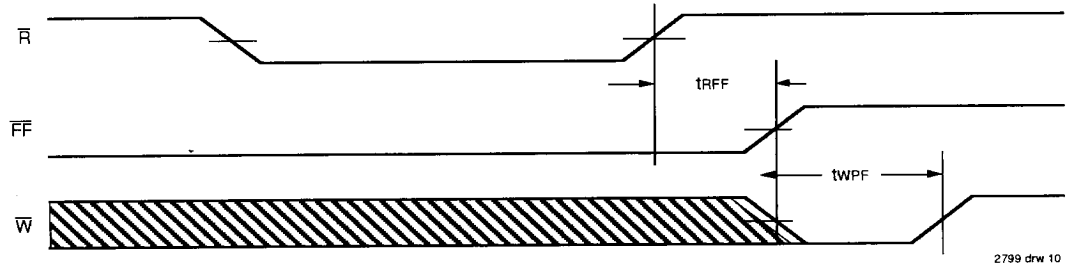
TIMING WAVEFORM OF THE EMPTY FLAG CYCLE(1)



NOTE:
1. (tRPE = tRPW)

TIMING WAVEFORM OF THE FULL FLAG CYCLE



NOTE:
1. (tWPF = tWPW)

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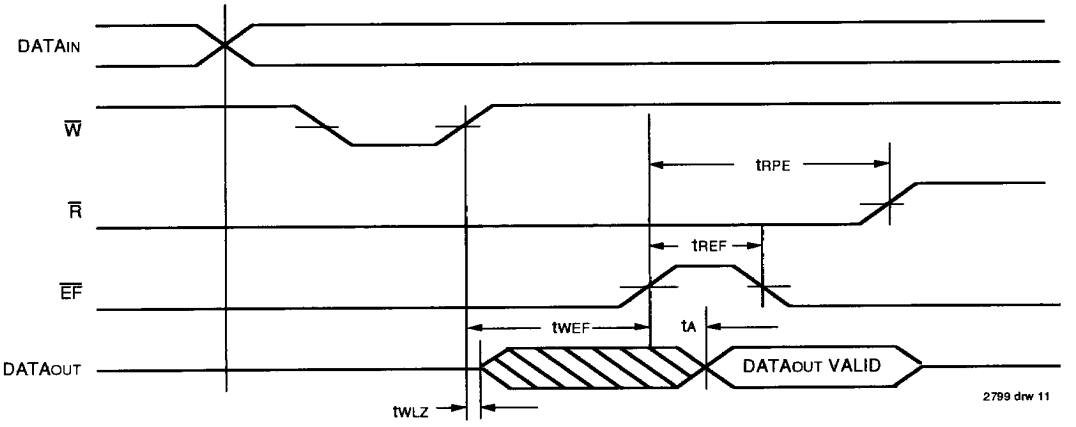
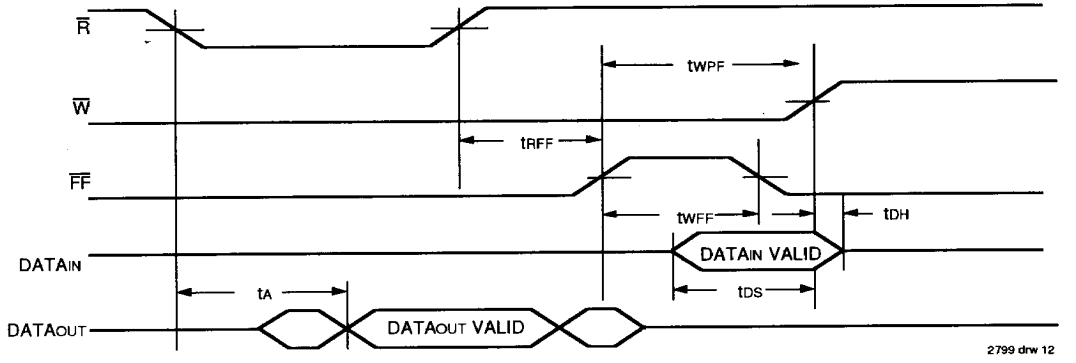
TIMING WAVEFORM OF READ DATA FLOW-THROUGH MODE



TIMING WAVEFORM OF WRITE DATA FLOW-THROUGH MODE



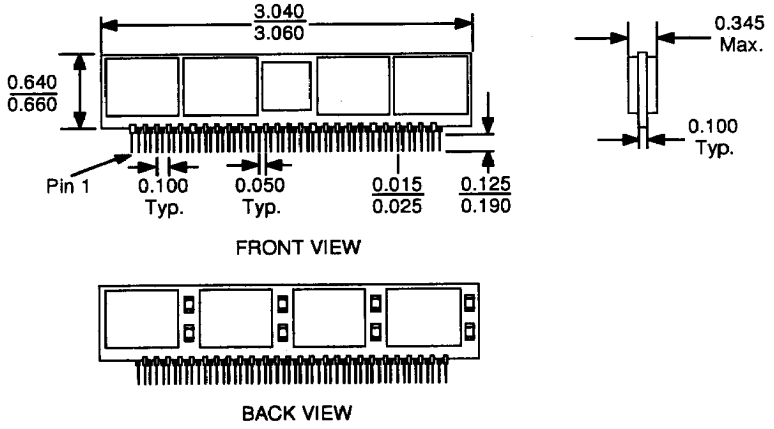
DEPTH/WIDTH EXPANSION & DATA FLOW-THROUGH MODES:

For more details on expanding FIFO modules in depth and/or width, please refer to the IDT7204 or IDT7205 data sheets.

For more details on data flow-through modes (read data fall-through and write data fall-through), please refer to the IDT7204 or IDT7205 data sheets.

1-12-9

PACKAGE DIMENSIONS



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