P3C3147
SUPER FAST 4K x 1
STATIC CMOS RAM (SCRAM)

PRELIMINARY

FEATURES

- **High Speed**
  - **6/7/8 ns (Address Access)**
  - **4/5/6 ns (Chip Select Access)**
- **Single 3.3V ± 0.2V Power Supply**
- **Low Power Operation**
  - **455 mW (Maximum)**
- **Full CMOS, 6T Cell**
- **Separate Data I/O**
- **Three-State Output**
- **TTL Logic Level Inputs and Output**
- **Produced with PACE III Technology™**
- **Compact Pinout**
  - **20-Pin 300 mil SOIC**

DESCRIPTION

The P3C3147 is a 4,096-bit super fast static RAM organized as 4K x 1 with separate data I/O and center-pin power and ground. This SCRAM belongs to a new category of static RAMs which offer speeds comparable with ECL and GaAs devices, but dissipate only a fraction of the power. The CMOS memory requires no clocks or refreshing. Inputs and outputs are compatible with TTL logic levels. The RAM operates from a single 3.3V ± 0.2V tolerance power supply.

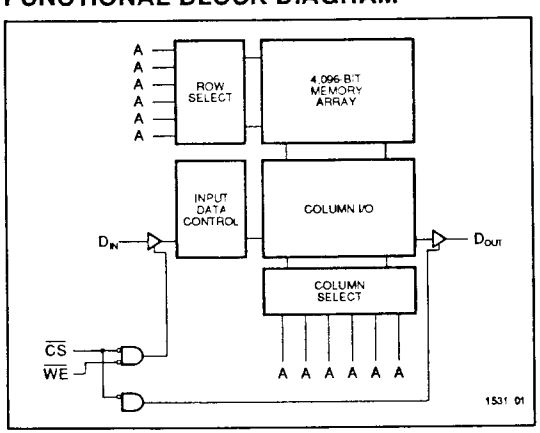
Cycle times as fast as 6 nanoseconds permit greatly enhanced system operating speeds. The P3C3147 also features a Chip Select control with data access as fast as 4 ns. CMOS is used to reduce power dissipation to a low 455 mW (maximum) while cycling at the highest frequency with 6 ns cycle time. During the write operation, the data output lines track the input data.

The P3C3147 is manufactured with PACE III Technology™ which is Performance Advanced CMOS Engineered with two-level metal and epitaxial substrates to use 0.4 micron effective channel lengths giving 250 picosecond loaded* internal gate delays. The nominal supply voltage is reduced from the conventional 5.0V to 3.3V, thus reducing output swings dramatically. This, together with the (lower inductance) center power and ground pins, and the extra power and extra ground pins, significantly reduces noise and ground bounce that would otherwise occur for very high speed circuitry.

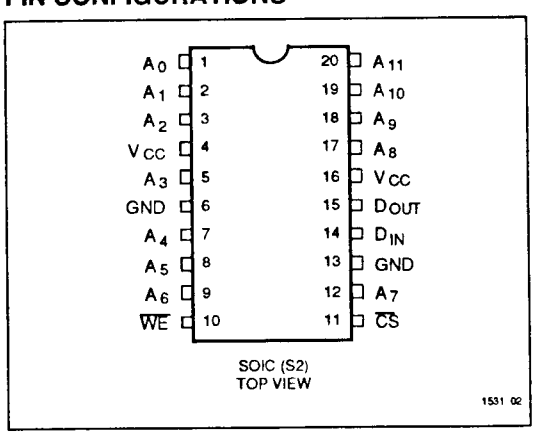
The P3C3147 is available in a 20-pin 300 mil SOIC package providing excellent board level densities.

*For a fan-in/fan-out of 4 at 85°C junction temperature and 3.3V supply.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



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MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Pin with Respect to GND	–0.5 to +5.0	V
V_{TERM}	Terminal Voltage with Respect to GND (up to 5.0V)	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	–55 to +125	°C

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Symbol	Parameter	Value	Unit
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

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RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade[2]	Ambient Temperature	GND	V_{CC}
Commercial	0°C to +70°C	0V	3.1V to 3.5V

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating temperature and supply voltage[2]

Symbol	Parameter	Test Conditions	P3C3147		Unit
			Min	Max	
V_{IH}	Input High Voltage		2.2	V_{CC}+0.5[3]	V
V_{IL}	Input Low Voltage		–0.5[3]	0.8	V
V_{CD}	Input Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA		–1.2	V
V_{OL}	Output Low Voltage (TTL Load)	I_{OL} = +8 mA, V_{CC} = Min.		0.4	V
V_{OLC}	Output Low Voltage (CMOS Load)	I_{OLC} = +100 µA, V_{CC} = Min.		0.2	V
V_{OH}	Output High Voltage (TTL Load)	I_{OH} = –4 mA, V_{CC} = Min.	2.4		V
V_{OHC}	Output High Voltage (CMOS Load)	I_{OHC} = –100 µA, V_{CC} = Min.	V_{CC}–0.2		V
I_{LI}	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	–10	+10	µA
I_{LO}	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT}= GND to V_{CC}	–50	+50	µA

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POWER DISSIPATION CHARACTERISTICS

Symbol	Parameter	Test Condition	-6	-7	-8	Unit
I_{CC}	Dynamic Operating Current	V_{CC} = Max., f = Max., Output Open, $V_{IN} \le V_{IL}$ or $V_{IN} \ge V_{IH}$	130	120	110	mA

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CAPACITANCES[4]

(V_{CC} = 3.3V, T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF

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Symbol	Parameter	Conditions	Typ.	Unit
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

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Notes:

1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
2. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
3. Transient inputs with V_L and I_L not more negative than –3.0V and –100mA, respectively, are permissible for pulse widths up to 20ns. Input voltages exceeding V_{CC} + 0.5 will cause extremely large currents to flow into the input pins.
4. This parameter is sampled and not 100% tested.

AC CHARACTERISTICS—READ CYCLE

Over recommended operating temperature and supply voltage[2]

Symbol	Parameter	-6		-7		-8		Unit
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	6		7		8		ns
t_{AA}	Address Access Time		6		7		8	ns
t_{AC}	Chip Enable Access Time		4		5		6	ns
t_{OH}	Output Hold from Address Change	1		1		1		ns
t_{LZ}	Chip Enable to Output in Low Z	1		1		1		ns
t_{HZ}	Chip Disable to Output in High Z		4		5		6	ns

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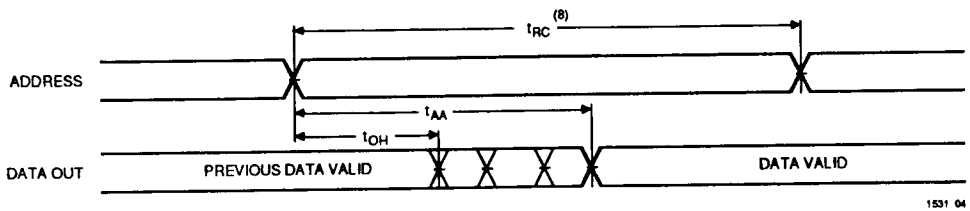
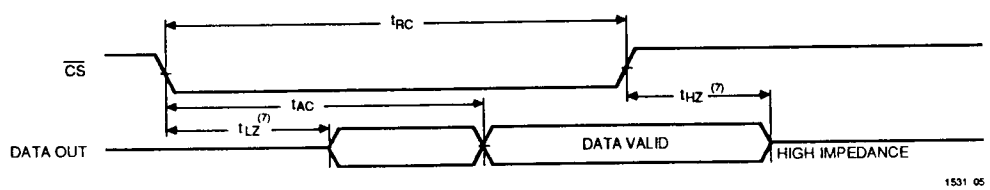
TIMING WAVEFORM OF READ CYCLE NO. 1 [5]



TIMING WAVEFORM OF READ CYCLE NO. 2 [6]



Notes:

5. $\overline{CS}$ isLOW and $\overline{WE}$ is HIGH for READ cycle.
6. $\overline{WE}$ is HIGH, and address must be valid prior to or coincident with $\overline{CS}$ transition LOW.
7. Transition is measured ±200mV from steady state voltage prior to change with specified loading in Figure 1. This parameter is sampled and not 100% tested.
8. Read Cycle Time is measured from the last valid address to the first transitioning address.

AC CHARACTERISTICS—WRITE CYCLE

Over recommended operating temperature and supply voltage[2]

Symbol	Parameter	-6		-7		-8		Unit
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	6		7		8		ns
t_{CW}	Chip Enable Time to End of Write	5		6		7		ns
t_{AW}	Address Valid to End of Write	5		6		7		ns
t_{AS1}	Address Set-up Time ($\overline{WE}$ controlled cycle)	1		1		1		ns
t_{AS2}	Address Set-up Time ($\overline{CS}$ controlled cycle)	0		0		0		ns
t_{WP}	Write Pulse Width	4		5		6		ns
t_{AH}	Address Hold Time	1		1		1		ns
t_{DW}	Data Valid to End of Write	3		4		5		ns
t_{DH}	Data Hold Time	1		1		1		ns
t_{AWE}	Write Enable to Data-out Valid		5		6		7	ns
t_{ADV}	Data-in Valid to Data-out Valid		5		6		7	ns

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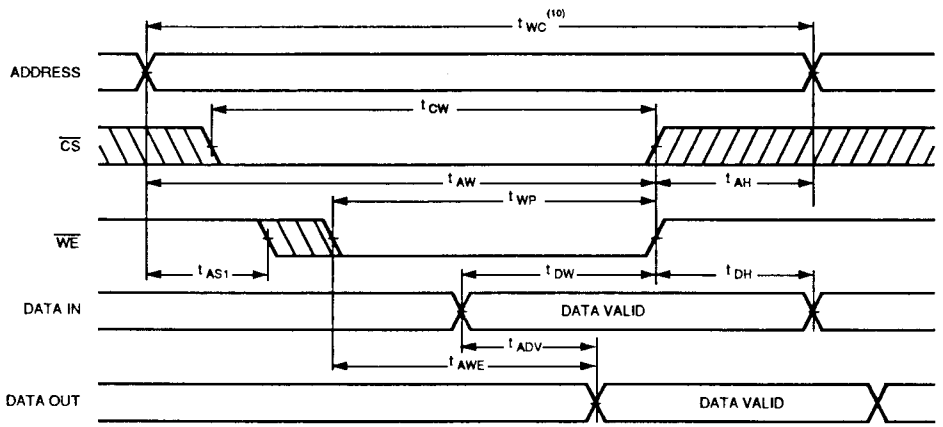
TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED) [9]



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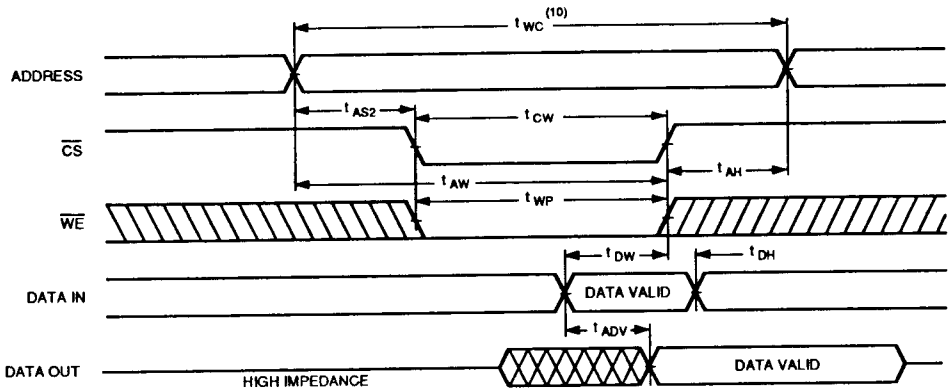
Notes:

9. $\overline{CS}$ and $\overline{WE}$ must be LOW for WRITE cycle.
10. Write Cycle Time is measured from the last valid address to the first transition address.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED) [9]



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Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figures 1 and 2

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Mode	$\overline{CS}$	$\overline{WE}$	Output
Standby	H	X	High Z
Read	L	H	D_{OUT}
Write	L	L	D_{IN}

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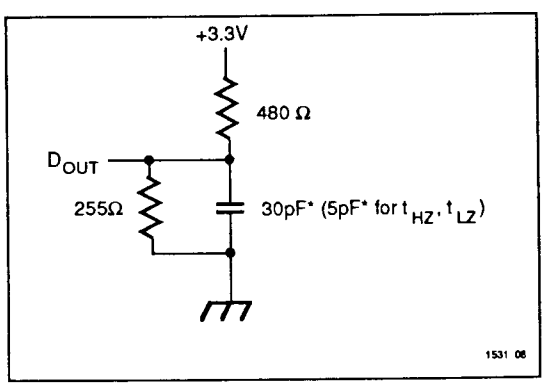


Figure 1. Output Load

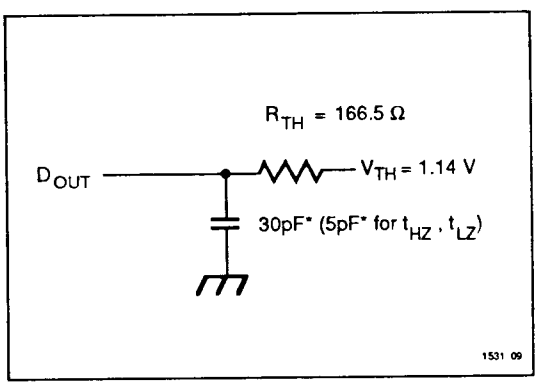
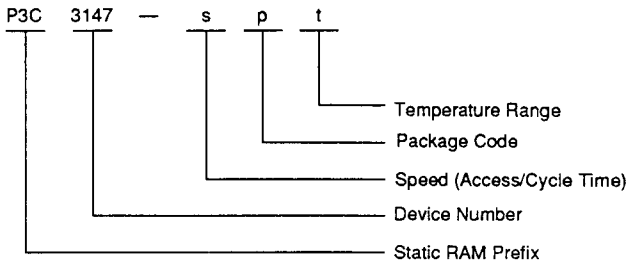


Figure 2. Thevenin Equivalent

* including scope and test fixture.

Note:
Because of the ultra-high speed of the P3C3147, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.14V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with D_{OUT} to match 166Ω (Thevenin Resistance).

ORDERING INFORMATION



s = Speed (access/cycle time in ns), e.g., 6, 7, 8

p = Package code, i.e., S.

t = Temperature range, i.e., C.

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PACKAGE SUFFIX

Package Suffix	Description
S	Plastic SOIC, 300 mil wide standard

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TEMPERATURE RANGE SUFFIX

Temperature Range Suffix	Description
C	Commercial Temperature Range, 0°C to +70°C.

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SELECTION GUIDE

The P3C3147 is available in the following temperature, speed and package options.

Temperature Range	Speed (ns) / Package	6	7	8
Commercial	Plastic SOIC	-6SC	-7SC	-8SC

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