Power failure detector and reset generator   PCF1252X Family

GENERAL DESCRIPTION

The PCF1252-X family are CMOS voltage detectors designed especially for power-ON/OFF detection in microcontroller/microprocessor systems (for initialization and data storage purposes). The output POWF is activated at a precise, temperature stable, trip-point. The RESET output has a built-in delay with duration determined by an external capacitor (C_{CT}). A second comparator (comparator 2) has been included to allow for the possibility of a second monitoring point in the system.

Features

- Low current consumption, typically 6 μA
- 10 versions available, trip-points vary from 2.55 V to 4.75 V
- Temperature stable trip-point
- Variable RESET delay
- Reset polarity selection
- Comparator for second level detection (e.g. overvoltage detection)
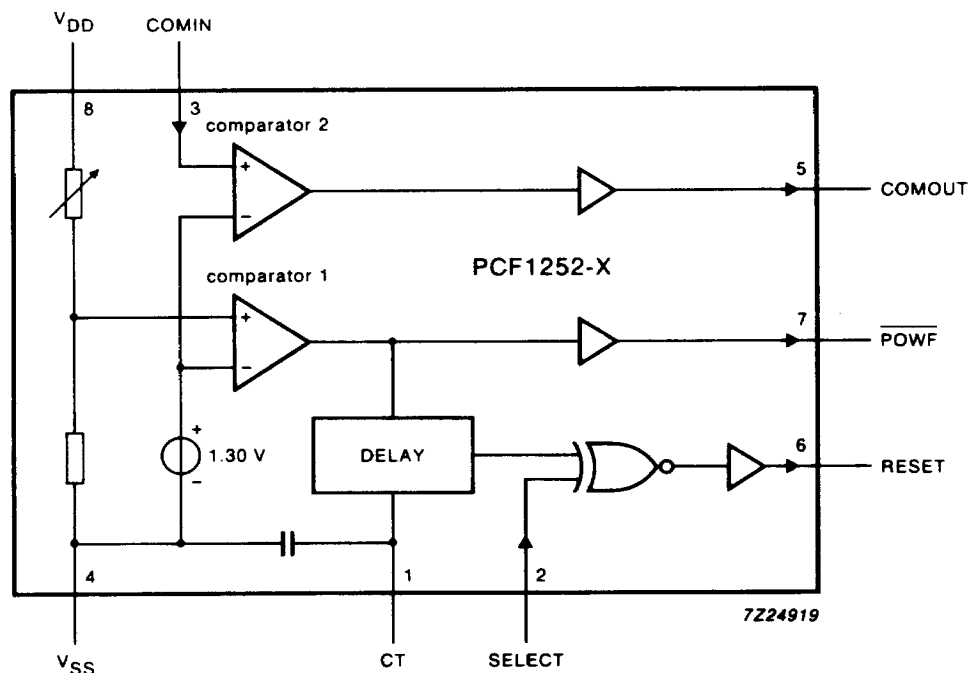- Advance warning of power failure

Fig.1 Block diagram.

PACKAGE OUTLINES

PCF1252-XP: 8-lead DIL; plastic (SOT97).
PCF1252-XT: 8-lead mini-pack; plastic (SO8; SOT96A).

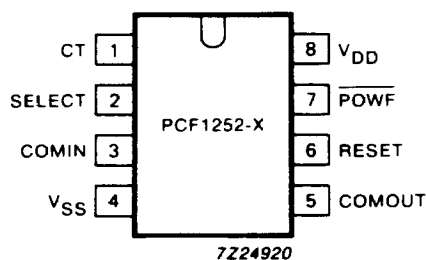Power failure detector and reset generator

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PINNING

Fig.2 Pinning diagram.

pin no.	mnemonic	description
1	CT	connection for the external capacitor
2	SELECT	select polarity or external reset input
3	COMIN	comparator input
4	V_{SS}	ground (0 V)
5	COMOUT	comparator output
6	RESET	reset output
7	$\overline{POWF}$	power failure signal output
8	V_{DD}	positive supply voltage

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FUNCTIONAL DESCRIPTION (see Fig.1)

The PCF1252-X contains a precise factory-programmed voltage reference, two comparators and a delay circuit. The PCF1252-X family is comprised of 10 versions with varying voltage trip-points (V_{TRIP}), see section "Characteristics".

Supply

The supply voltage (V_{DD}) is internally divided before being compared, via comparator 1, with the internal reference voltage.

$\overline{POWF}$ (see Fig.3)

The $\overline{POWF}$ output is:

- LOW, if V_{DD} is below V_{TRIP}.
- HIGH, if V_{DD} is above V_{TRIP}.

Power-ON reset (SELECT = LOW)

As V_{DD} rises past V_{TRIP}, a positive reset pulse is generated at RESET. The duration of the reset pulse (t_R) is determined by the value of the external capacitor (C_{CT}; maximum 1 μF, see Fig.8) connected to CT. With no external capacitor connected, C_{CT} assumes a minimum value of 100 pF. If SELECT is HIGH, the reset pulse is inverted.

Power failure

During a power-OFF condition ($V_{DD} < V_{TRIP}$), $\overline{POWF}$ goes LOW. After a time delay (t_S), also determined by C_{CT}, RESET goes HIGH. Any $\overline{POWF}$ output ($V_{DD} < V_{TRIP}$) will result in a subsequent RESET pulse.

Voltage trip-point

By selecting the voltage trip-point slightly higher than the minimum operating voltage of the microcontroller/microprocessor, there is sufficient time for data storage before the power actually fails.

In order to prevent oscillations around the voltage trip-point, a small hysteresis has been included, resulting in a power-ON switching point that is higher than the voltage trip-point (minimum of 15 mV). The voltage trip-point refers to the value at which power-OFF is signalled.

COMIN

Input to the second comparator (comparator 2). When used in conjunction with an external voltage divider, this allows a second point in the system to be monitored. This input has no built-in hysteresis. When not in use connect to V_{DD}. COMOUT will be LOW or HIGH depending on the voltage at COMIN:

- COMOUT = HIGH, if voltage at COMIN is above the switch point V_{SP} (typically 1.30 V).

- COMOUT = LOW, if voltage at COMIN is below the switch point V_{SP} (typically 1.30 V).

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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_{DD}	−0.5	+ 7	V
Input voltage range		V_I	−0.5	$V_{DD} + 0.5$	V
DC clamp-diode current	all pins; $V_I < -0.5$ V or $> V_{DD} + + 0.5$ V	I_I	−	20	mA
Output current		I_O	−	20	mA
Total power dissipation		P_{tot}	−	150	mW
Storage temperature range		T_{stg}	−65	+ 100	°C
Operating ambient tempeteture range		T_{amb}	−40	+ 85	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal handling precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

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CHARACTERISTICS (see Fig.3)

V_{DD} = 2.4 V to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 °C to + 85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_{DD}	2.4	—	6.0	V
Voltage trip-point:	T_{amb} = + 25 °C					
PCF1252-0		V_{TRIP}	4.70	4.75	4.80	V
PCF1252-1		V_{TRIP}	4.50	4.55	4.60	V
PCF1252-2		V_{TRIP}	4.20	4.25	4.30	V
PCF1252-3		V_{TRIP}	4.00	4.05	4.10	V
PCF1252-4		V_{TRIP}	3.70	3.75	3.80	V
PCF1252-5		V_{TRIP}	3.50	3.55	3.60	V
PCF1252-6		V_{TRIP}	3.20	3.25	3.30	V
PCF1252-7		V_{TRIP}	3.00	3.05	3.10	V
PCF1252-8		V_{TRIP}	2.70	2.75	2.80	V
PCF1252-9		V_{TRIP}	2.50	2.55	2.60	V
Supply current	T_{amb} = + 25 °C; see Figs 4 and 5 V_{DD} = V_{TRIP} + 0.5 V; COMIN = V_{DD}	I_{DD}	—	6	10	μA
Voltage trip-point temperature coefficient	note 1	ΔV_{TRIP}	—	$\pm 100 \times 10^{-6}$	$\pm 400 \times 10^{-6}$	/K
Voltage trip-point hysteresis		V_H	15	30	50	mV
COMIN switch point	T_{amb} = + 25 °C	V_{SP}	1.28	1.30	1.32	V
COMIN switch point temperature coefficient	note 1	ΔV_{SP}	—	±0.1	±0.5	mV/K
SELECT input voltage:						
LOW		V_{IL}	—	—	$0.3V_{DD}$	V
HIGH		V_{IH}	$0.7V_{DD}$	—	—	V
SELECT and COMIN leakage current:						
LOW		$-I_{IL}$	—	—	1.0	μA
HIGH		I_{IL}	—	—	1.0	μA
POWF, RESET and COMOUT						
Output sink current	see Fig.6; V_O = 0.4 V; V_{DD} = 2.4 V	I_O	1	3	—	mA
Output source current	see Fig.7; V_O = 2.0 V; V_{DD} = 2.4 V	$-I_O$	0.75	2	—	mA
Reset time	note 2; C_{CT} = 1 nF	t_R	400	1000	2000	μs
Save time	note 2; C_{CT} = 1 nF	t_S	40	100	200	μs
Reset to save time ratio		t_R/t_S	—	10	—	

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CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
CT internal capacitance		C_{INT}	–	100	–	pF

Notes to the characteristics

1. Value given per degree Kelvin. Tested on a sample basis.
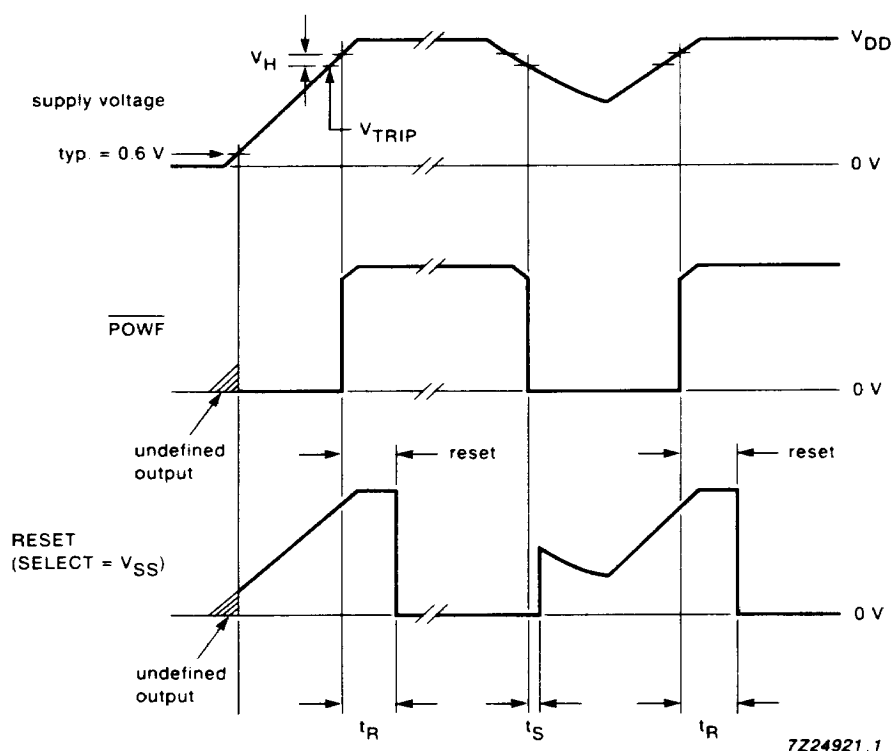2. Conformance to these specifications is only guaranteed when the slew rate of V_{DD} is less than 25 V/ms.

Fig.3 Timing diagram.

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Typical performance characteristics
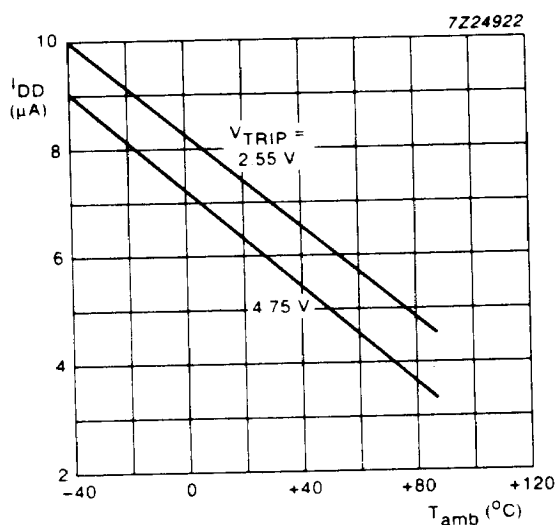
Fig.4 Supply current as a function of temperature; V_{DD} = 5 V; COMIN = V_{DD}.
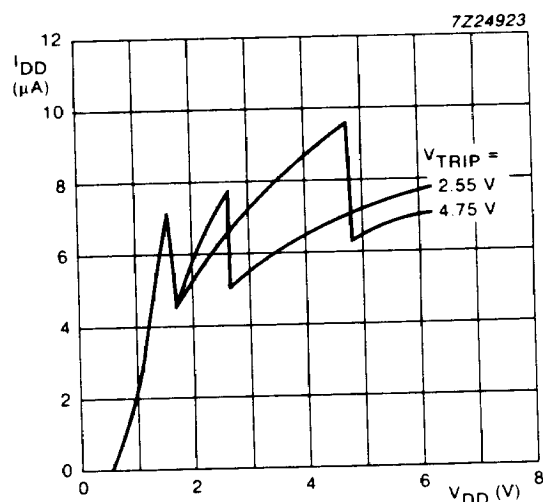
Fig.5 Supply current as a function of the supply voltage; T_{amb} = + 25 °C.
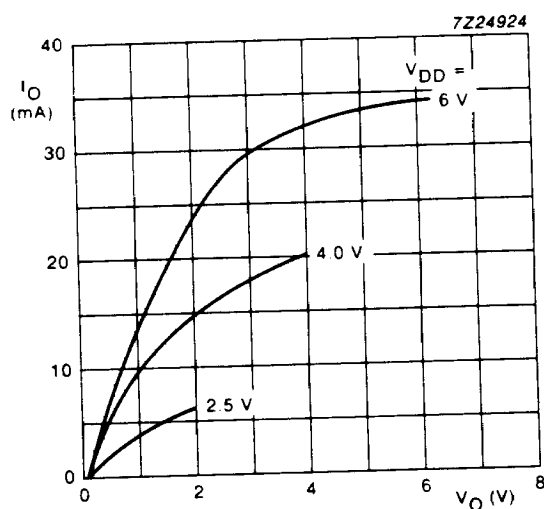
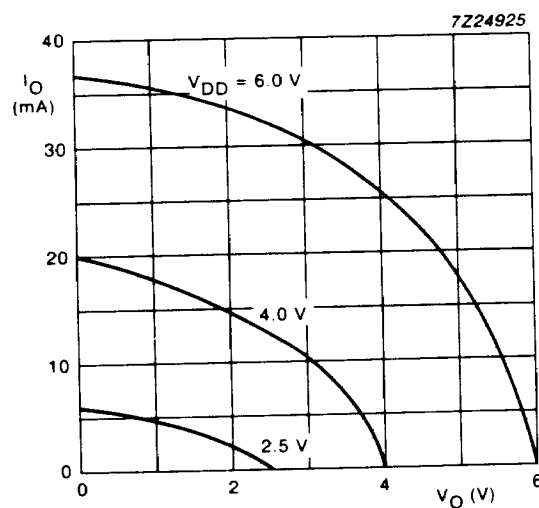Fig.6 Output sink current as a function of the output voltage.

Fig.7 Output source current as a function of the output voltage.

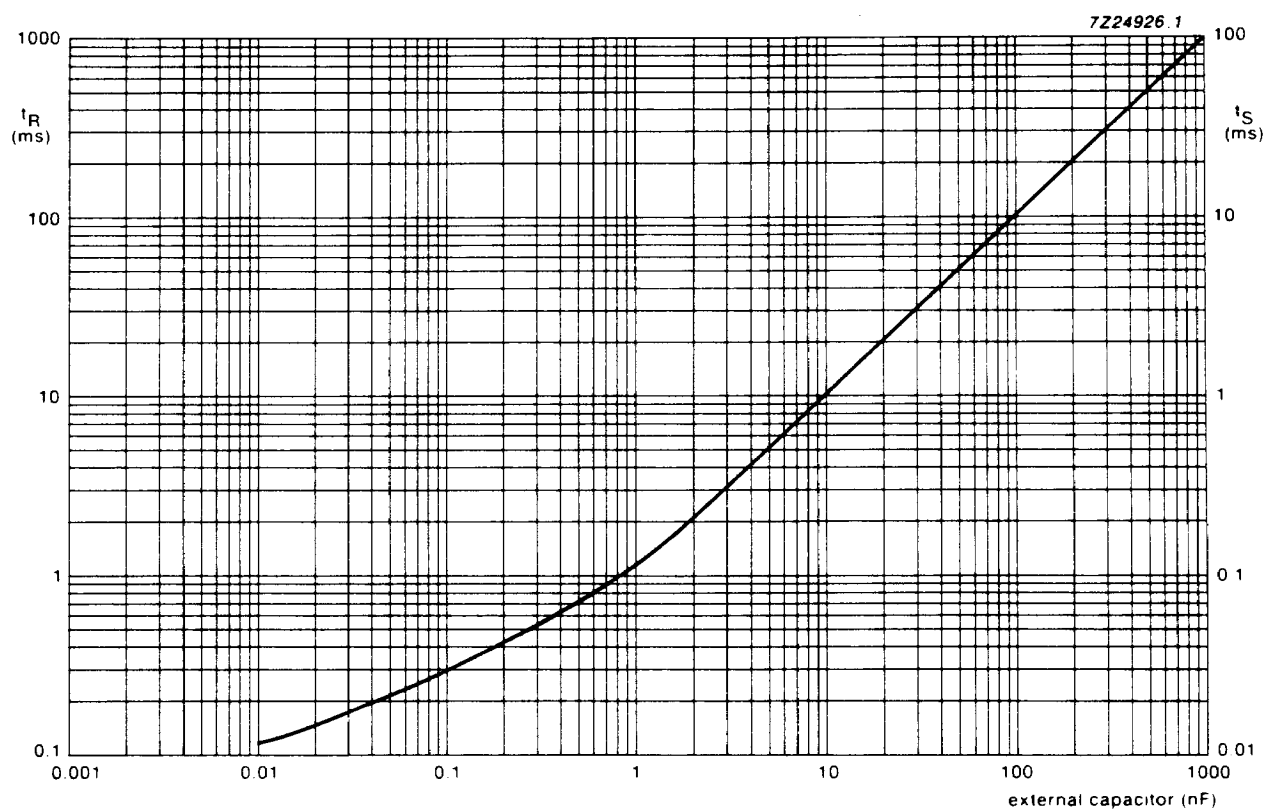## Power failure detector and reset generator

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Fig.8 Reset and save times as a function of the external capacitor (C_{CT}).

Notes to Fig.8

1. t_R (typ.) = $(0.1 + C_{CT})$ ms.
2. t_S (typ.) = $(0.01 + 0.1 C_{CT})$ ms.

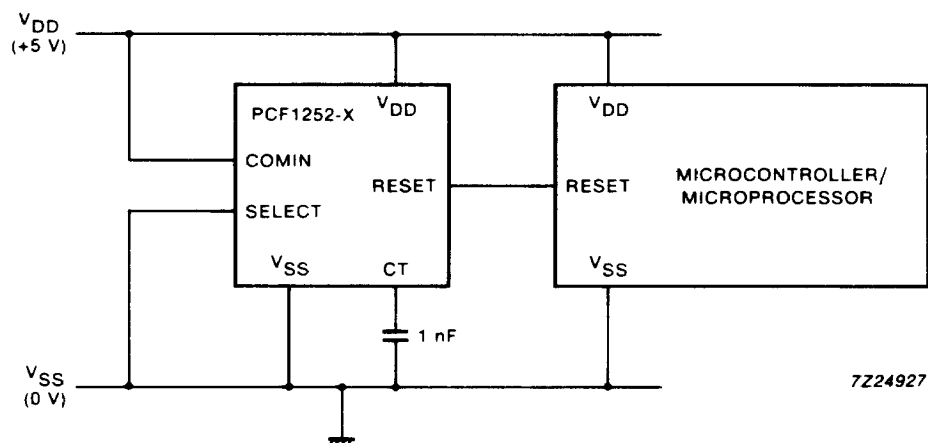## Power failure detector and reset generator

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APPLICATION INFORMATION

Fig.9 Typical power-ON reset circuit for a microcontroller/microprocessor system;
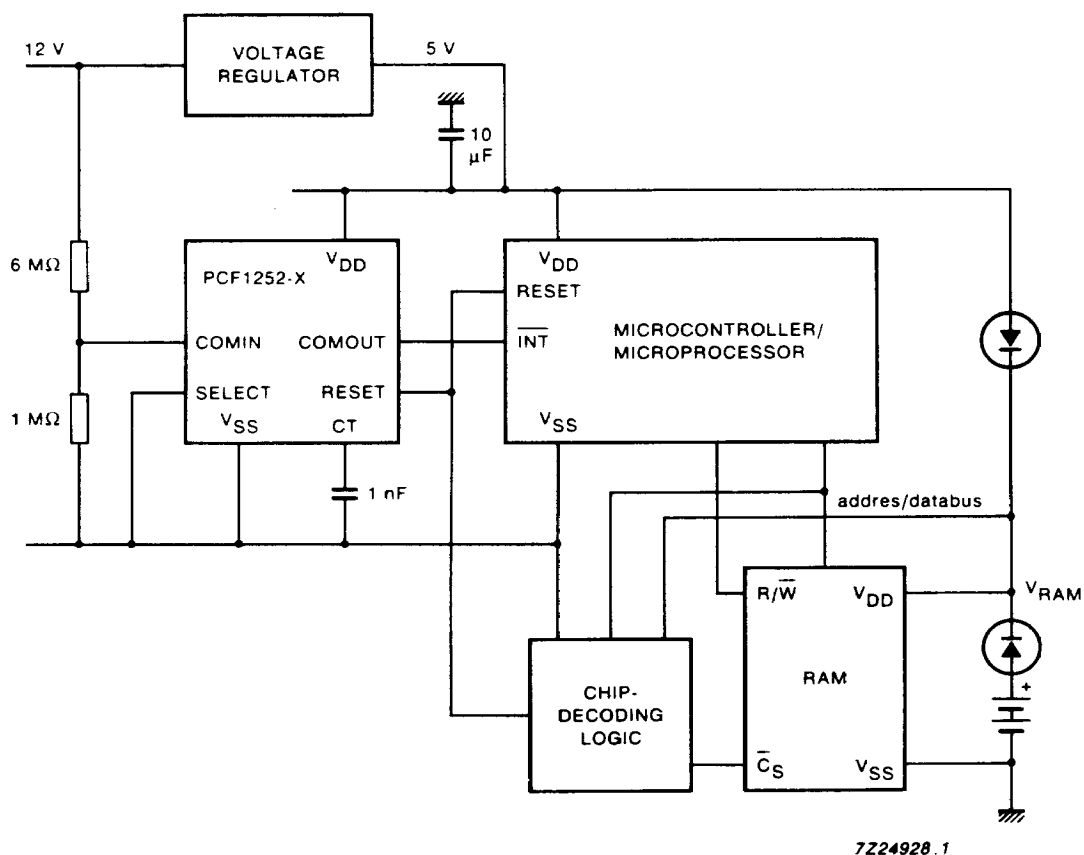(when not used, COMIN must be connected to V_{DD}).

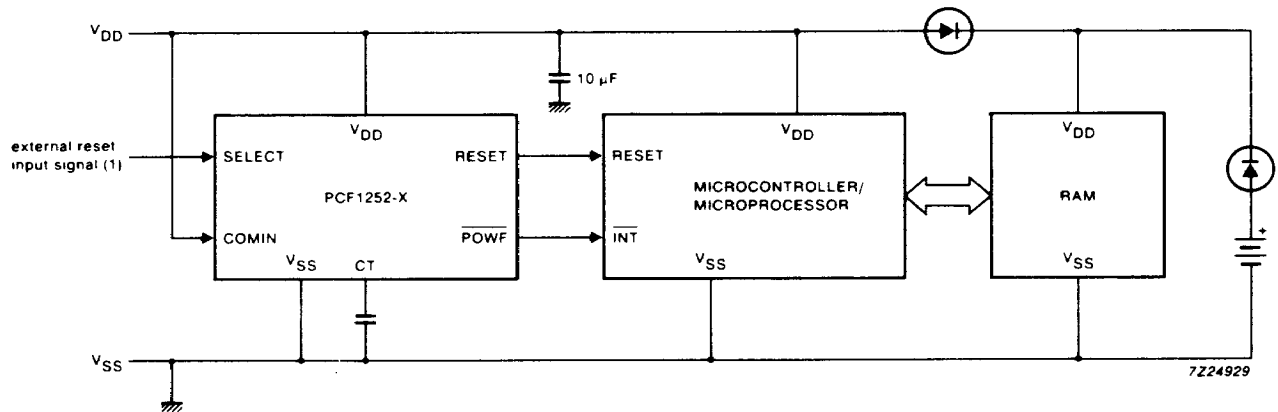Fig.10 Data retention circuit for memory back-up systems.

Fig.11 Data retention circuit with external switchable reset for systems with a single voltage supply.

Note to Fig.11

1. For external reset application, the SELECT input must be debounced.