DATA SHEET

TEA6821T
ICE car radio

Preliminary specification
File under Integrated Circuits, IC01

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Philips
Semiconductors

PHILIPS

FEATURES

General

- FM mixer for conversion from FM IF_1 = 72.2 MHz to FM IF_2 = 10.7 MHz
- AM mixer for conversion from AM IF_1 = 10.7 MHz to AM IF_2 = 450 kHz
- FM IF gain stage
- Crystal oscillator providing mixer frequencies and references for IF count and stereo decoder
- FM quadrature demodulator with automatic centre frequency adjust and THD compensation
- Level and multipath and noise detectors
- Soft mute
- Stereo noise cancelling and variable de-emphasis
- PLL stereo decoder
- Noise blanker
- AM IF amplifier and demodulator
- I^2C-bus transceiver
- IF count for AM and FM
- Reference frequency generation for PLL synthesizer
- Reduced external components
- SW applicable.

Stereo decoder

- Adjustment-free PLL-VCO
- Pilot depending mono/stereo switching
- Analog control of mono/stereo blend
- Adjacent channel noise suppression (114 kHz)
- Pilot canceller
- Analog control of de-emphasis
- Integrated low-pass filters for 190 kHz adjacent channel interferences and signal delay for interference absorption circuit.

GENERAL DESCRIPTION

The TEA6821T together with the TEA6810T / TEA6811T forms an AM/FM electronic tuned car radio in a double conversion receiver concept for European, American and Japanese frequency range.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{s1}	supply voltage 1 (pins 56 and 28)	note 1	7	8.5	10	V
V_{s1}	operating range		8.1	8.5	8.9	V
I_{s1}	supply current 1 FM		–	28	–	mA
I_{s1}	supply current 1 AM		–	24	–	mA
V_{s2}	supply voltage 2 (pin 5)	note 1	4.5	5.0	5.5	V
V_{s2}	operating range		4.75	5.0	5.25	V
I_{s2}	supply current 2 FM		–	31	–	mA
I_{s2}	supply current 2 AM		–	28	–	mA
S+N/N	signal-to-noise AM	m = 0.3	–	57	–	dB
THD	distortion AM		–	1	2	%
S+N/N	signal-to-noise FM	Δf = 22.5 kHz at pins 43 and 47	66	72	–	dB
THD	distortion FM	Δf = 75 kHz	–	0.1	0.35	%
α	channel separation (adjusted)		40	–	–	dB
T_{amb}	operating ambient temperature		–40	–	+85	°C

Note to the quick reference data

1. IC is functional, specified parameters may deviate from limits which are valid for operating range.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA6821T	VSO56	plastic very small outline package; 56 leads	SOT190-1

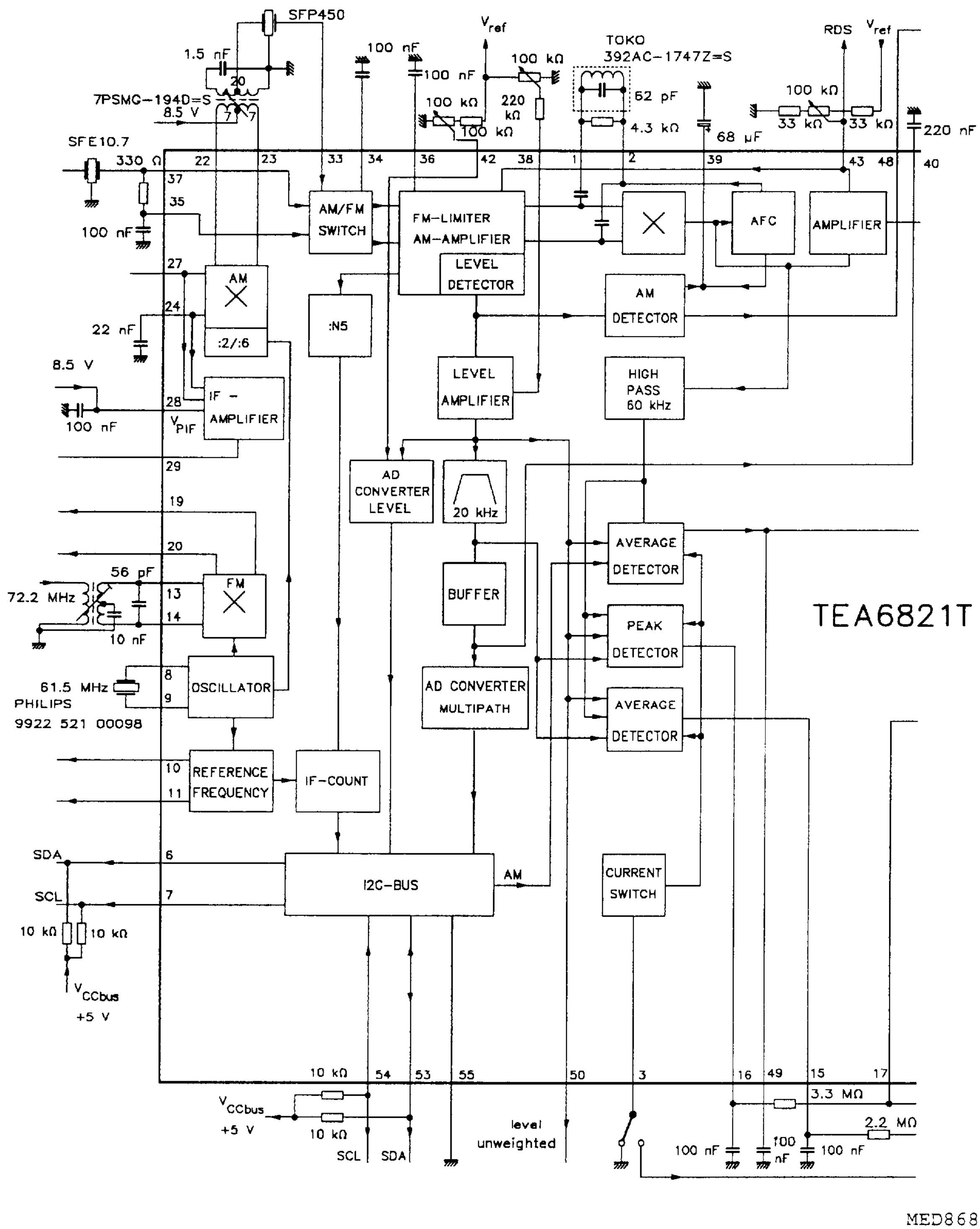


Fig.1 Block diagram (continued in Fig.2).

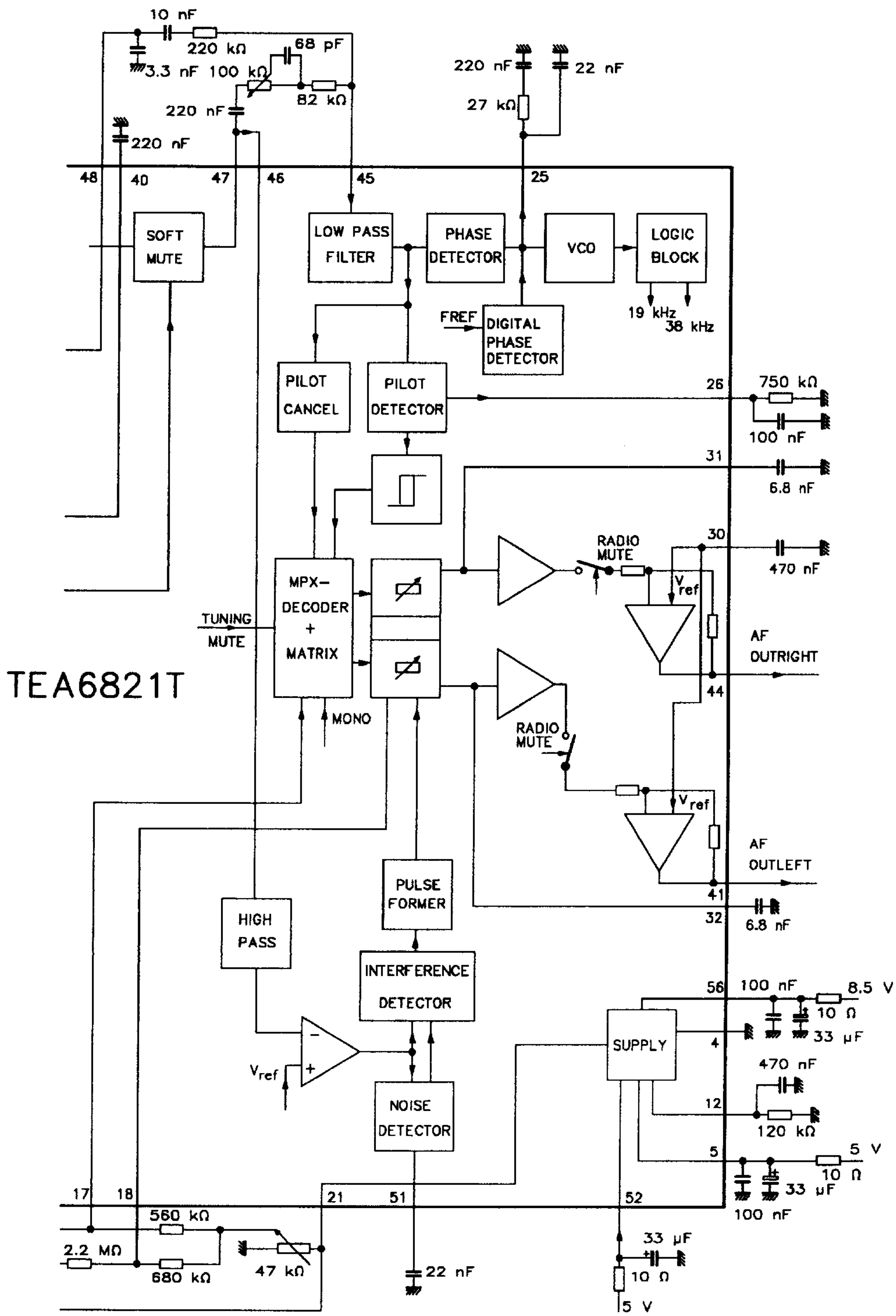


Fig.2 Block diagram (continued from Fig.1).

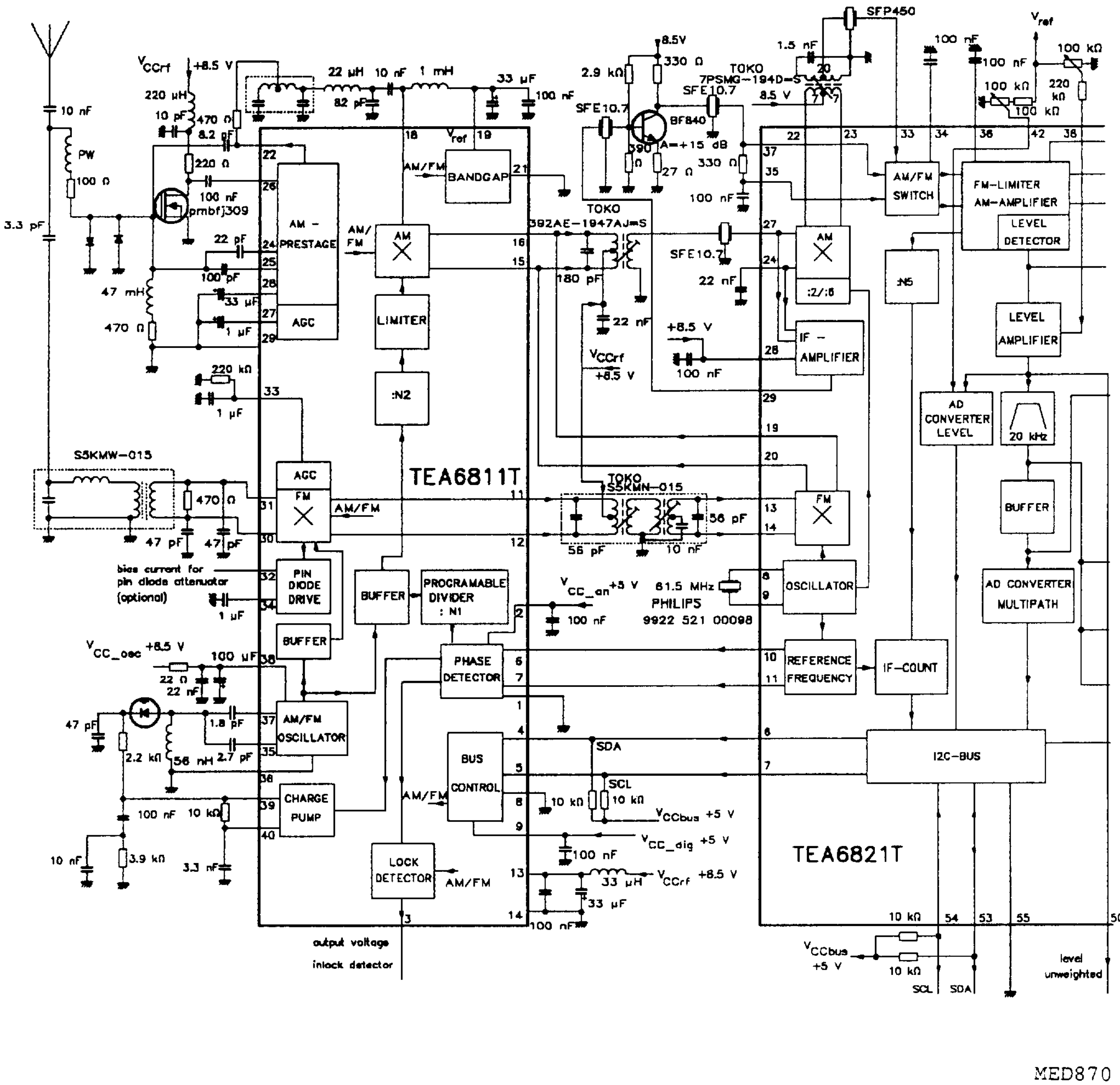


Fig.3 ICE91 application diagram (continued in Fig.4).

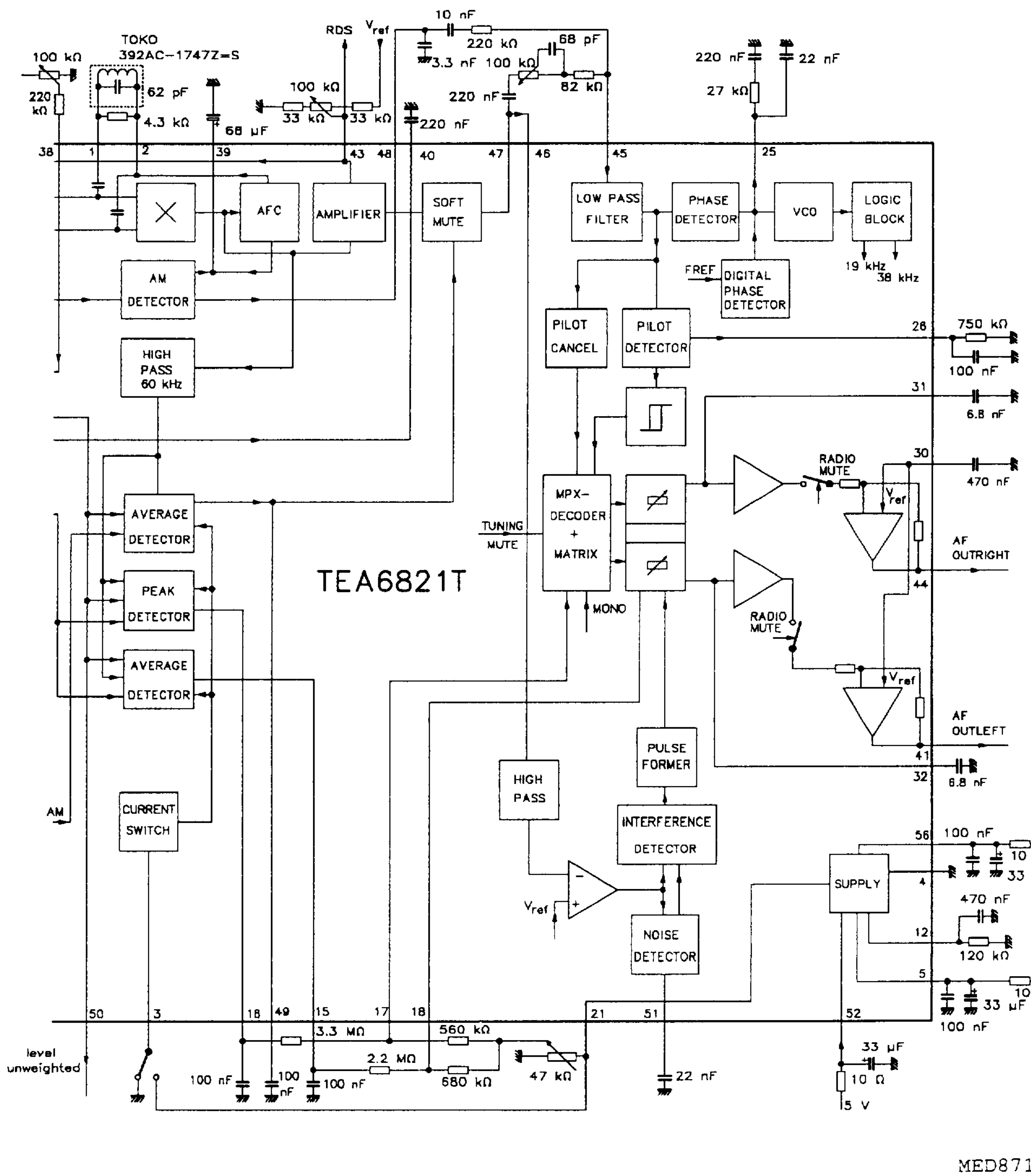


Fig.4 ICE91 application diagram (continued from Fig.3).

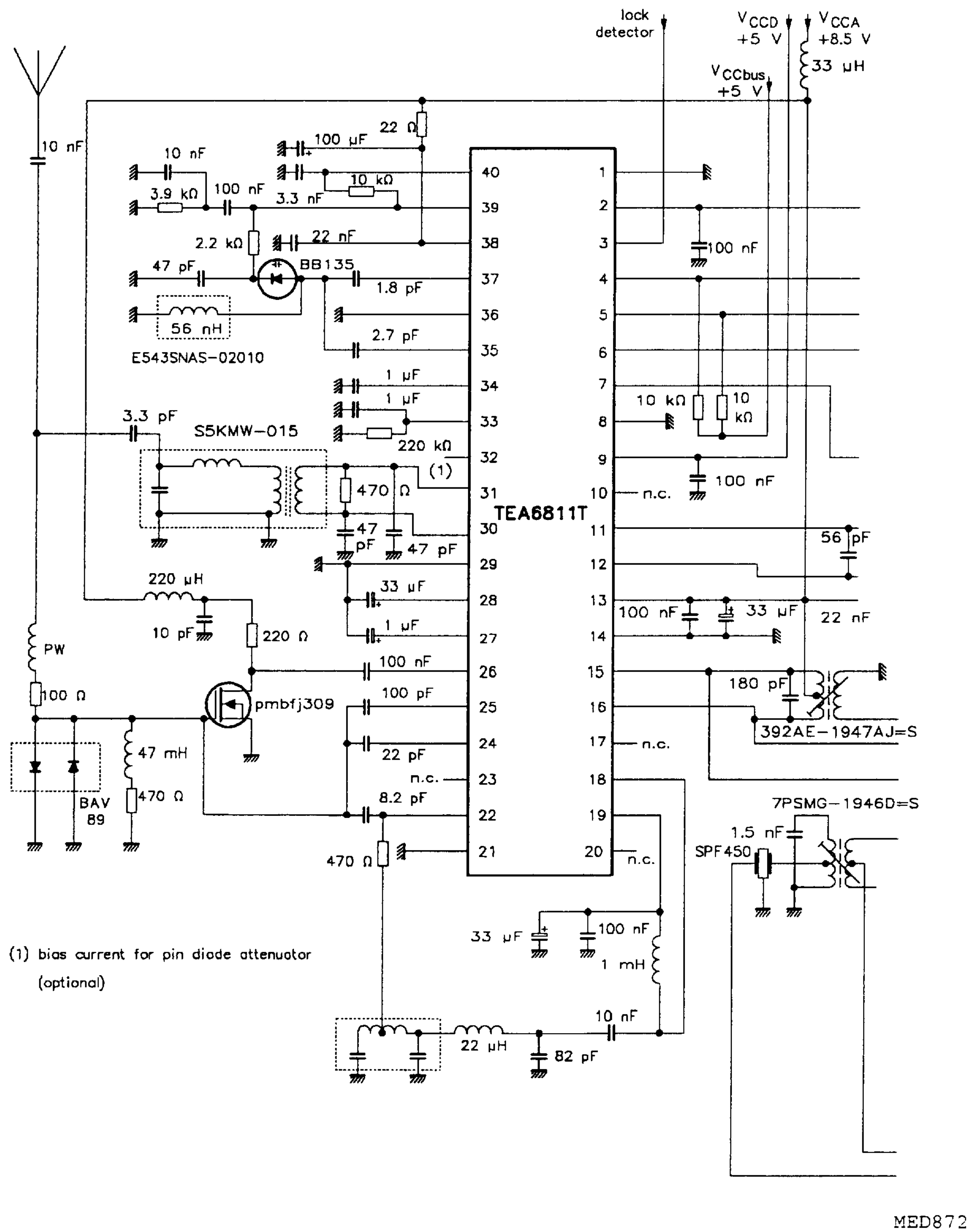


Fig.5 AM/FM car radio receiver with TEA6811T and TEA6821T (continued in Fig.6).

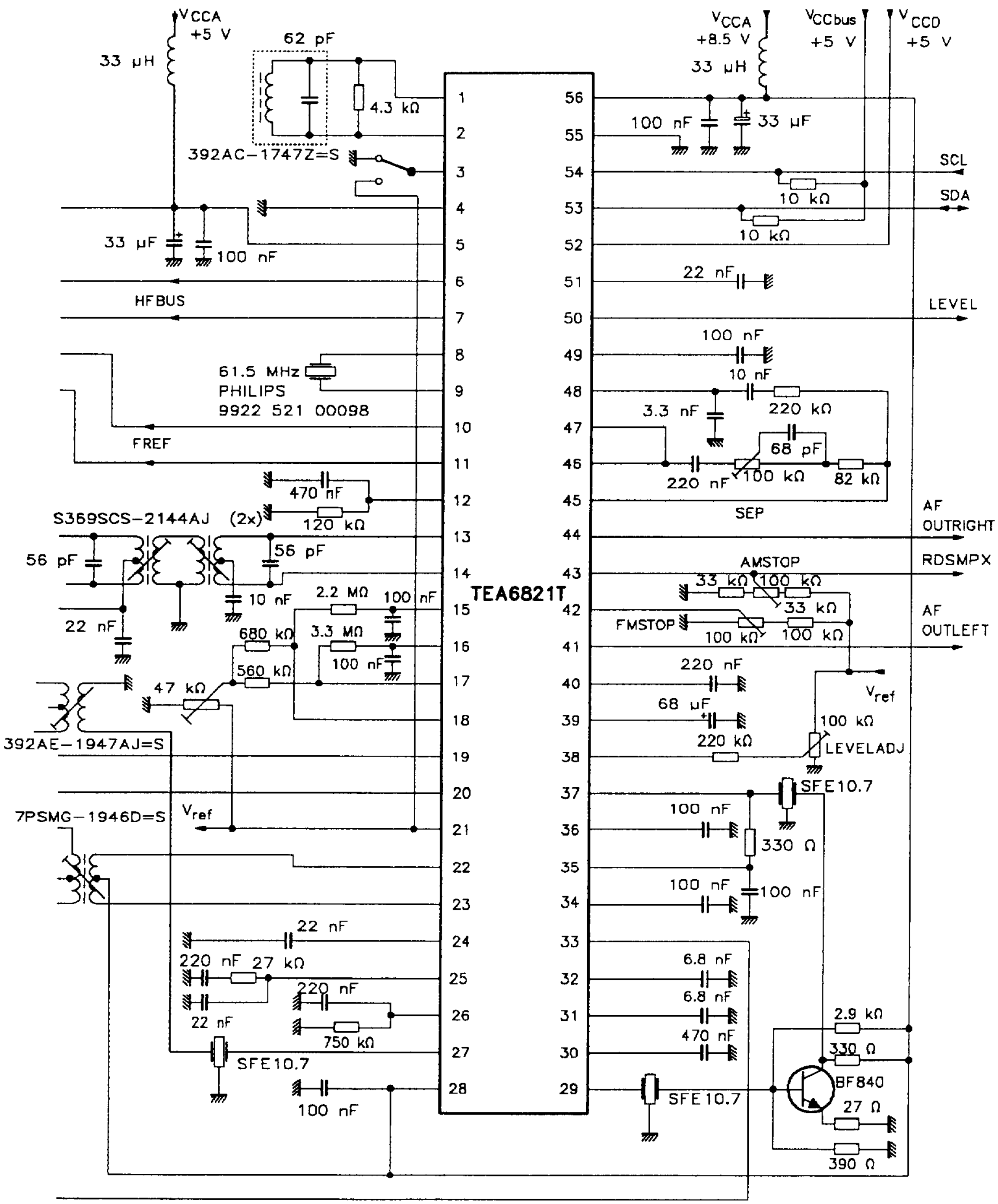


Fig.6 AM/FM car radio receiver with TEA6811T and TEA6821T (continued from Fig.5).

PINNING

SYMBOL	PIN	DESCRIPTION
QDET1	1	demodulator tank
QDET2	2	demodulator tank
TSWITCH	3	time switch
GND	4	analog ground
V_{P5}	5	5 V supply voltage
HFBUS1	6	HF bus, pull-up to 5 V
HFBUS2	7	HF bus, pull-up to 5 V
XTAL1	8	crystal oscillator
XTAL2	9	crystal oscillator
F_{REFP}	10	PLL reference frequency
F_{REFN}	11	PLL reference frequency
I_{REF}	12	reference current
FMIF1IN1	13	70 MHz FM-IF input
FMIF1IN2	14	70 MHz FM-IF input
TSDR	15	time constant for SDR
TSDS	16	time constant for SDS
V_{SDS}	17	SDS control voltage
V_{SDR}	18	SDR control voltage
FMIF2OUT1	19	FM mixer output
FMIF2OUT2	20	FM mixer output
V_{REF}	21	reference voltage
AMIF2OUT1	22	AM mixer output
AMIF2OUT2	23	AM mixer output
FMAMDEC	24	FM/AM 10.7 MHz decoupling
PHASEDET	25	phase detector
PILDET	26	pilot detector
FMAM10.7	27	FM/AM 10.7 MHz input
V_{PIF}	28	V_P IF amplifier

SYMBOL	PIN	DESCRIPTION
FMIFAMPOUT	29	FM-IF amplifier output
AFGND	30	AF ground
DEEMPHR	31	de-emphasis capacitor right
DEEMPHL	32	de-emphasis capacitor left
AMIF2IN1	33	AM IF2 input 1
AMIF2IN2	34	AM IF2 input 2
FMIN2	35	FM limiter input
DCFEED	36	DC feed FM limiter
FMIN1	37	FM limiter input
LEVELADJ	38	level adjust
C_{AFC}	39	AFC capacitor
MPBUF	40	multipath buffer time constant
OUTLEFT	41	AF output left
FMSTOP	42	FMSTOP adjust
RDS/AMSTOP	43	MPX for RDS/AMSTOP adjust
OUTRIGHT	44	AF output right
MPXIN	45	stereo decoder MPX input
IAC_{IN}	46	IAC input
MPXOUT	47	FM demodulator MPX output
AMAFOUT	48	AM demodulator AF output
V_{MUTAML}	49	mute voltage / AM level
LEVELUNWEIG	50	level unweighted
$I_{ACCONTR}$	51	IAC control voltage
V_{PDIG}	52	V_P digital
SDA	53	SDA, pull-up to 5 V
SCL	54	SCL, pull-up to 5 V
BUSGND	55	bus ground
$V_{P8.5}$	56	V_P 8.5 V

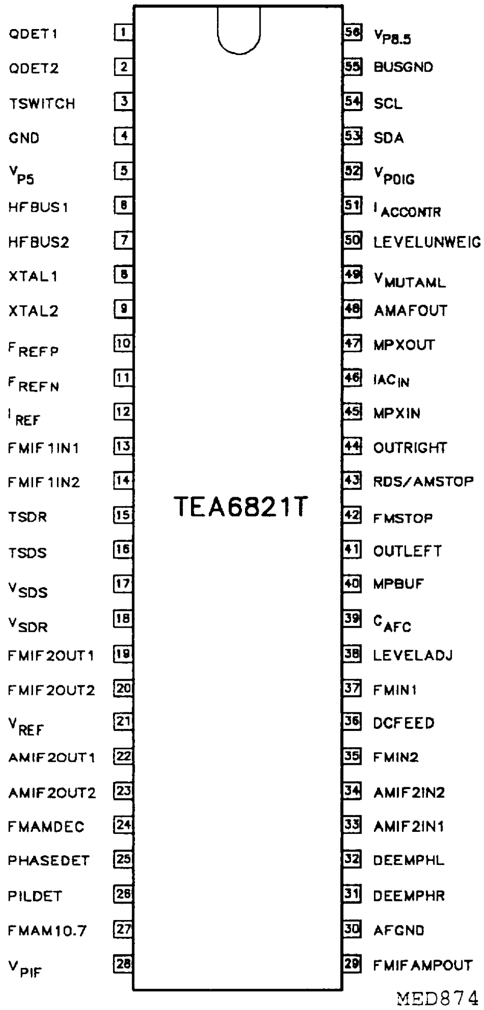


Fig.7 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{s1}	supply voltage 1 (pins 56 and 28)	–0.3	+12	V
V_{s2}	supply voltage 2 (pin 5)	–0.3	+6.5	V
V_{s3}	supply voltage 3 (pin 52)	–0.3	+6.5	V
T_{stg}	storage temperature	–55	+150	°C
T_{amb}	operating ambient temperature	–40	+85	°C
V_{ESD}	electrostatic handling (note 1)			
	for pins 8 and 9	–	±100	V
	for other pins	–	±300	V

Note to the limiting values

1. Charge device model class B: discharging a 200 pF capacitor through a 0 Ω series resistor.

CHARACTERISTICS

V_{56-4} = V_{28-4} = 8.5 V, V_{5-4} = V_{52-55} = 5 V, T_{amb} = +25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Current consumption						
I_{s1}	supply current 1	FM	24	30	36	mA
I_{56}	supply current 1at pin 56		16	20	24	mA
I_{28}	supply current 1 at pin 28		2.4	3.0	3.6	mA
I_{19} + I_{20}	supply current 1 at pins 19 and 20		4.8	6.0	7.2	mA
I_{s1}	supply current 1	AM	18	24	30	mA
I_{56}	supply current 1at pin 56		9.5	12	15	mA
I_{22} + I_{23}	supply current 1 at pins 22 and 23		8	10	12.5	mA
I_{s2}	supply current 2 at pin 5	FM	18	21	25	mA
		AM	14	17	21	mA
I_{s3}	supply current 3 at pin 52		8	10	12	mA
FM IF path						
FM mixer						
R_{13-14}	input resistance		5	7	–	kΩ
C_{13-4}, C_{14-4}	input capacitance		–	3	4.5	pF
R_{opt}	optimum generator resistance		–	1.2	–	kΩ
R_{19-20}	output resistance		15	20	–	kΩ
C_{19-4}, C_{20-4}	output capacitance		–	5	7	pF
$I_{19IF2}/V_{13-14IF1}$	conversion gain		1.65	1.9	2.2	mS
I_{19}, I_{20}	mixer bias current		2.4	3.0	3.6	mA
	mixer leakage current	in AM position	–	–	2	µA
V_{19-20}	maximum output voltage (peak-to-peak value)		12.0	14.0	–	V
IP3	third order intermodulation		114	124	–	dBµV
Oscillator						
f_{osc}	oscillator frequency		–	61.5	–	MHz
	oscillator spread		–	–	250	Hz
$\Delta f_{osc}/\Delta T$	temperature dependence of oscillator frequency	crystal type PHILIPS 9922 521 00098	–	30	–	ppm/K
R_1	crystal motional resistance		–	–	70	Ω
C_0	crystal shunt capacitance		–	–	5	pF
FM IF2 amplifier						
V_{29-4}/V_{27-24}	amplifier gain	loaded with 330 Ω; see Fig.9	8	10	12	dB
V_{27-24}	maximum input voltage for 1 dB compression point (RMS value)		80	110	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{29-4}	maximum output voltage (RMS value)		220	270	–	mV
R_{27-24}	input resistance		300	330	360	Ω
C_{27-4}, C_{24-4}	input capacitance		–	–	5	pF
R_{29-4}	output resistance		300	330	360	Ω
C_{29-4}	output capacitance		–	–	5	pF
FM IF2 limiter						
V_{1-2}/V_{37-35}	limiter gain	see Fig.10	–	74	–	dB
C_{37-4}	input capacitance		–	–	5	pF
R_{1-2}	output resistance		–	–	1.0	kΩ
C_{1-2}	output capacitance		10	15	20	pF
V_{1-2}	limiter output voltage (peak-to-peak value)		500	700	–	mV
FM demodulator						
f_{mod} = 1kHz; deviation = 22.5 kHz; R_g= 50 Ω; V_{37-35} = 10 mV; with de-emphasis = 50 µS; coil quality = 15 unless otherwise specified.						
V_{47-4}	MPX output (RMS value)		160	200	240	mV
R_{47out}	output resistance		–	–	500	Ω
B	AF bandwidth		200	–	–	kHz
V_{43-4}	MPX output for RDS (RMS value)		160	200	240	mV
R_{43out}	output resistance		–	–	500	Ω
B	AF bandwidth		200	–	–	kHz
V_{37-35}	start of limiting (RMS value)	α_{AF} = –3 dB	–	40	60	µV
V_{37-35}	input voltage for signal-plus-noise-to-noise ratio (RMS value)	see Fig.11 for pin 47 (MPXOUT) and Fig.12 for pin 43 (RDS/AMSTOP)				
		S+N/N = 26 dB	–	40	55	µV
		S+N/N = 46 dB	–	100	140	µV
S + N/N	signal-plus-noise-to-noise ratio		66	72	–	dB
V_{43FM}/V_{43AM}	suppression	∆f = 22.5 kHz; f_{modAM} = 1 kHz; m_{AM} = 30%; V_{37-35} = 3 mV to 300 mV	55	60	–	dB
V_{47FM}/V_{47AM}	suppression	V_{37-35} = 1 mV to 300 mV	55	60	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
THD	total harmonic distortion	detuning ≤ 50 kHz; Δf = 75 kHz; f_{mod} = 1 kHz without de-emphasis L_{demod} = typical value				
		pin 43	–	0.1	0.35	%
		V_{37-35} = 300 μV to 800 mV				
		pin 47	–	0.1	0.35	%
		V_{37-35} = 1 mV to 800 mV				
$\Delta V_{43AFCdisabled}$ /$\Delta V_{43AFCactive}$	demodulator frequency control (AFC) efficiency at 100 kHz detune from exact tuning		30	34	–	dB
ΔV_{43}	residual DC-offset	ΔL_{demod} = typical value;				
		10 μV < V_{37-35} < 80 μV	–	100	1000	mV
		80 μV < V_{37-35} < 800 mV	–	10	30	mV
Unweighted level voltage						
BW_{50}	bandwidth		500	–	–	kHz
R_{out50}	output resistance		–	–	100	Ω
V_{50-4}	level unweighted voltage	see Fig.13; V_{38} = 2.52 V;				
		V_{37-35} ≤ 2.5 μV	1.8	2.4	3.2	V
		V_{37-35} = 1.0 mV	2.7	3.4	4.7	V
V/20 dB	slope of level unweighted voltage $\Delta V_{50-4}/\Delta V_{37-35}$	V_{37-35} ≤ 100 μV (RMS) < 300 mV	0.75	0.845	0.95	V
ΔV_{50-4}/VK	temperature dependence	V_{37-35} = 1 mV	–	4.0	–	mV/VK
Adjust of level unweighted voltage and V_{mutaml}; typical adjusting range see Figs 14 and 17.						
ΔV_{50}	adjusting range	V_{37-35} = 1 mV (RMS)	–	±2	–	V
ΔV_{50-4} /ΔV_{38-4}	adjusting gain		–	–0.9	–	–
R_{38}	input resistance		–	80	–	kΩ
V_{38-4}	internal bias voltage		–	2.6	–	V
Muting dependence on adjust of level unweighted voltage; typical curve see Fig.15.						
$\alpha = V_{43}/V_{47}$	start of mute	V_{49}/V_{21} = 0.6	–	3	–	–
$\Delta\alpha$ /ΔV_{49}	mute slope	α = –6 dB	–	25	–	dB/V
Soft mute, time constant control, mono/stereo blend and high-cut control						
Time constant control (see application diagram Fig.3): Slow or fast attack and decay time constants for soft mute, mono/stereo and high-cut control can be chosen connecting pin 3 to GND or pin 21.						
Mute voltage: The static mute voltage follows the level unweighted voltage as function of FM IF_2 voltage and level adjust voltage V_{38-4}. It additionally depends on multipath level, noise (adjacent channel interferences) and the position of Tswitch. Typical curve for mute voltage dependence on V_{37-35} see Fig.16.						
V_{49-4}	mute voltage	V_{38} = 2.52 V;				
		V_{37-35} ≤ 2.5 μV	1.8	2.2	3.2	V
		V_{37-35} = 1.0 mV	2.7	3.3	4.7	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V/20 dB	slope of mute voltage $\Delta V_{49-4}/\Delta V_{37-35}$	$V_{37-35} \leq 100$ µV (RMS) < 300 mV	0.75	0.845	0.95	V
ΔV_{49-4}/VK	temperature dependence	V_{37-35} = 1 mV	–	4.0	–	mV/VK
Attack and decay time for mute voltage.						
I_{49}	charge current	pin 3 connected to GND	–	3.0	–	µA
	discharge current		–	–3.6	–	µA
	charge current	pin 3 connected to pin 21	–	130	–	µA
	discharge current		–	–160	–	µA
Δf	muting activated by 60 kHz FM interference	pin 3 connected to GND; V_{37-35} = 3 mV; V_{49} < 2 V; f_{mod} = 60 kHz	–	30	–	kHz
Time constant for mono/stereo blend voltage. The mono/stereo blend voltage is generated as a function of FM IF_2 voltage, multipath level, noise and position of Tswitch.						
I_{16}	charge current	V_{37-35} = 3 mV;	–	0.5	–	µA
	discharge current	pin 3 connected to GND	–	–18	–	µA
	charge current	V_{37-35} = 3 mV;	–	26	–	µA
	discharge current	pin 3 connected to pin 21	–	–800	–	µA
m	mono/stereo blend activated by 20 kHz AM interference	V_{16} < 2 V; V_{37-35} = 3 mV; R_{L16} > 50 MΩ;				
		f_{mod} = 20 kHz; pin 3 connected to GND	–	45	–	%
		pin 3 connected to pin 21	–	40	–	%
Δf	mono/stereo blend activated by 60 kHz FM interference	V_{16} < 3 V; V_{37-35} = 3 mV; R_{L16} > 50 MΩ;				
		f_{mod} = 60 kHz; pin 3 connected to GND	–	30	–	kHz
		pin 3 connected to pin 21	–	22	–	kHz
Time constant for high-cut control voltage (SDR). The high-cut control voltage is generated as a function of FM IF_2 voltage, multipath level, noise and position of Tswitch.						
I_{15}	charge current	V_{37-35} = 3 mV;	–	0.4	–	µA
	discharge current	pin 3 connected to GND	–	–0.44	–	µA
	charge current	V_{37-35} = 3 mV;	–	41	–	µA
	discharge current	pin 3 connected to pin 21	–	–44	–	µA
m	high-cut control activated by 20 kHz AM interference	V_{15} < 2 V; V_{37-35} = 3 mV; R_{L15} > 50 MΩ; f_{mod} = 20 kHz;				
		pin 3 connected to GND	–	40	–	%
		pin 3 connected to pin 21	–	35	–	%
Δf	high-cut control activated by 60 kHz FM interference	V_{15} < 2 V; V_{37-35} = 3 mV; R_{L15} > 50 MΩ; f_{mod} = 60 kHz;				
		pin 3 connected to GND	–	25	–	kHz
		pin 3 connected to pin 21	–	20	–	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Multipath detector						
f_{MP}	multipath detector band-pass centre frequency		–	20	–	kHz
B_{MP}	band-pass bandwidth		7.0	–	–	kHz
Reference voltage						
V_{21-4}	output voltage	I_{21} = –1 mA	4.5	5.1	5.7	V
ΔV_{21-4}	temperature dependence		–	3.3	–	mV/VK
I_{21}	output current		–	–	1	mA
AM IF path						
AM mixer; f_{IF1} = 10.7 MHz; f_{IF2} = 450 kHz; (see Fig.18)						
R_{27-24}	input resistance		300	330	360	Ω
C_{27-24}	input capacitance		–	5	8	pF
R_{22-23}	output resistance		10.0	20.0	–	kΩ
C_{22-23}	output capacitance		–	5	10	pF
$I_{22IF2}/V_{27-24IF1}$	conversion gain		2.2	2.7	3.4	mS
I_{22}, I_{23}	mixer bias current		4.0	5.0	6.0	mA
	mixer leakage current	in FM position	–	–	2	μA
V_{22-23}	maximum output voltage (peak-to-peak value)		12	15	–	V
IP3	third order intermodulation		–	137	–	dBμV
AM oscillator						
The AM oscillator signal is generated by division of the 61.5 MHz crystal oscillator. Two divider ratios programmable via I^2C-bus: division by 6 (AM IF_1 = 10.7 MHz), division by 2 (AM IF_1 = 30 MHz)						
AM detector f_{AMIF2} = 450 kHz; f_{mod} = 400 Hz; m = 30%						
V_{48-4}	AF output level (RMS value)	R_{L48} > 500 kΩ; 300 μV ≤ V_{33-34} ≤ 300 mV	190	240	290	mV
V_{33-34}	sensitivity (RMS value)	S+N/N = 26 dB	–	150	250	μV
		S+N/N = 46 dB	–	500	700	μV
S+N/N	signal-plus-noise-to-noise ratio		54	57	–	dB
THD	total harmonic distortion	m = 0.8; 1 mV ≤ V_{24-23} ≤ 300 mV	–	1.0	3.0	%
V_{33-34}	AM IF_2 minimum input (RMS value)	THD ≤ 5%; m = 0.8	–	–	500	μV
	AM IF_2 maximum input (RMS value)		800	–	–	mV
R_{33-34}	IF_2 input resistance		1.8	2.0	2.2	kΩ
C_{24-23}	IF_2 input capacitance		–	10	15	pF
R_{48out}	output resistance		27	33	39	kΩ
C_{48out}	output capacitance		–	–	10	pF
typical AM level curve see Fig.19						
Stereo decoder; note 1						
Input signal (Δf = 75 kHz) V_{MPX} (p-p) = 1.7 V; modulation frequency f_{mod} = 1 kHz; de-emphasis time constant τ = 50 μs; nominal input resistor (pin 45) R_i = 168 kΩ.						

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	MPX input overdrive margin	THD = 1%	4	–	–	dB
V_{44-4}, V_{41-4}	AF output voltage (RMS value)		800	900	1000	mV
V_{44-4}/V_{41-4}	difference of output voltage		–	–	±1	dB
R_{o44}, R_{o41}	output resistor		–	–	130	Ω
R_{lmin}	minimum load resistor		12	–	–	kΩ
I_{44}, I_{41}	maximum output current		150	–	–	μA
V_{44-4}, V_{41-4}	DC output voltage		3.3	3.8	4.3	V
α	channel separation (adjusted; a typical roll-off at f_{MPX} = 38 kHz of 1 dB is internally compensated)		40	–	–	dB
THD	total harmonic distortion		–	0.1	0.3	%
S+N/N	signal-plus-noise-to-noise ratio	f = 20 Hz to 20 kHz	74	80	–	dB
Carrier and harmonic suppression at the output (note to the stereo decoder).						
α_{19}	pilot signal	f = 19 kHz	–	50	–	dB
α_{38}	subcarrier	f = 38 kHz	–	50	–	dB
α_{57}(4)		f = 57 kHz	–	46	–	dB
α_{76}		f = 76 kHz	–	60	–	dB
α_2(2)	intermodulation	f_{mod} = 10 kHz; f_{spur} = 1 kHz	–	60	–	dB
α_3(3)		f_{mod} = 13 kHz; f_{spur} = 1 kHz	–	58	–	dB
α_{57}(4)	traffic radio (ARI)	f = 57 kHz	–	70	–	dB
α_{67}(5)	subsidiary communications authorization	f = 67 kHz	70	–	–	dB
α_{114}(6)	adjacent channel frequency	f = 114 kHz	–	80	–	dB
α_{190}(7)		f = 190 kHz	–	70	–	dB
α_{rr}	ripple rejection at output	f_r = 100 Hz; V_r = 100 mV_{eff}	–	30	–	dB
Mono/stereo control						
V_{ipil}	pilot threshold voltage	stereo on	–	24	30	mV
		mono on	8	20	–	mV
ΔV_{ipil}	switch hysteresis V_{ion}/V_{ioff}		–	2	–	dB
The stereo decoder can be set to mono via the I^{2}C-bus						
Pilot presence indication via I^{2}C-bus						
External Mono/stereo control						
$V_{17} - 0.75V_{21}$	control voltage channel separation	see Fig.21				
		α = 6 dB	–	–80	–	mV
		α = 16 dB	–	–40	–	mV
Muting functions (mute via I^{2}C-bus)						
α_{mute}	tuned mute		60	–	–	dB
ΔV_{44}, ΔV_{41}	DC offset voltage		–50	–	+50	mV
α_{mute}	radio mute (in combination with tuned mute)		80	–	–	dB
ΔV_{44}, ΔV_{41}	DC offset voltage		–300	–	+300	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
High-cut control (see Fig.22)						
τ_{deemph}	control range of de-emphasis		50	–	80	µs
$V_{18} – 0.75V_{21}$	control voltage	τ_{deemph} = 50 µs	0	–	–	mV
		τ_{deemph} = 80 µs	–	–300	–	mV
The nominal de-emphasis value can be changed to 75 µs with C_{31}, C_{32} = 10 nF.						
Voltage controlled oscillator						
The VCO is adjusted by means of a digital auxiliary PLL.						
f_{osc}	oscillator frequency range		450	456	462	kHz
Noise blanker						
Interference detection at pin 50 level unweighted or MPXOUT (pin 47)						
T_{sup}	interference suppression time		–	40	50	µs
f_c	high-pass input filter for interference pulse, 2nd order	3 dB frequency	150	200	250	kHz
IAC control						
I_{51}	charge current (into 4 V)		5.0	10	18	µA
	discharge current (from 8.5 V)		–0.5	–1.0	–1.8	mA
V_{pulse}	trigger sensitivity	τ_{pulse} = 10 µs	–	–	20	mV
ΔV_{DC} (pin 51)	trigger threshold measured with f_{int} = 250 kHz	V_{noise} (pin 46) = 10 mV	–	200	–	mV
V_{tr} (pin 46)		V_{DC} (pin 51) = 7.7 V	–	10	–	mV
ΔV_{DC} (pin 51)		V_{noise} (pin 46) = 100 mV	–	2.3	–	V
V_{tr} (pin 46)		V_{DC} (pin 51) = 6.7 V	–	100	–	V
I_{os}	gate input offset current at pins 31 and 32 during suppression pulse duration		–	20	50	nA

Notes to the characteristics

1. By changing the value of the input resistor at pin 12 the MPX input can be adapted to the level of the FM demodulator output (see Fig.20). A 3rd order low-pass filter f_g = 90 kHz at the MPX input provides extra 190 kHz ACI suppression. For AM the VCO is switched off. Interference gate at MPX demodulator outputs.

2. $\alpha_2 = \frac{V_0 \text{(signal) (at 1 kHz)}}{V_0 \text{(spurious) (at 1 kHz)}}$; $f_s = (2 \times 10 \text{ kHz}) - 19 \text{ kHz}$

3. $\alpha_3 = \frac{V_0 \text{(signal) (at 1 kHz)}}{V_0 \text{(spurious) (at 1 kHz)}}$; $f_s = (3 \times 13 \text{ kHz}) - 38 \text{ kHz}$

4. $\alpha_{57} \text{ (ARI)} = \frac{V_0 \text{(signal) (at 1 kHz)}}{V_0 \text{(spurious) (at 1 kHz} \pm \text{23 Hz)}}$

5. $\alpha_{67} = \frac{V_0 \text{(signal) (at 1 kHz)}}{V_0 \text{(spurious) (at 9 kHz)}}$; $f_s = (2 \times 38 \text{ kHz}) - 67 \text{ kHz}$

6. $\alpha_{114} = \frac{V_0 \text{(signal) (at 1 kHz)}}{V_0 \text{(spurious) (at 4 kHz)}}$; $f_s = 110 \text{ kHz} - (3 \times 38 \text{ kHz})$

7. $\alpha_{190} = \frac{V_0 \text{(signal) (at 1 kHz)}}{V_0 \text{(spurious) (at 4 kHz)}}$; $f_s = 186 \text{ kHz} - (5 \times 38 \text{ kHz})$

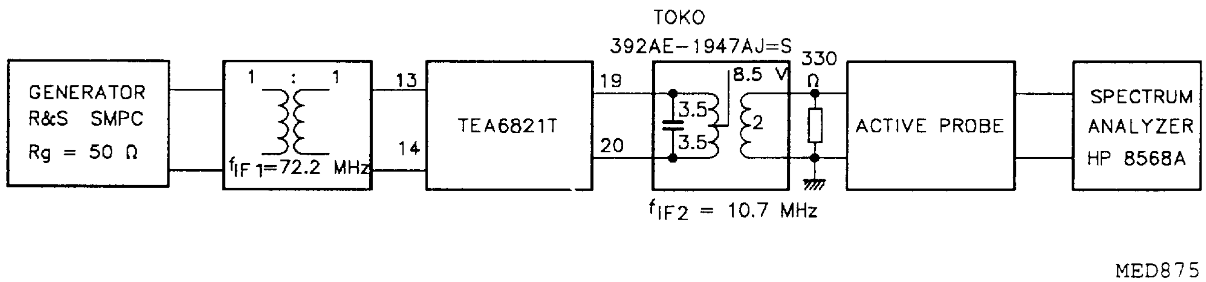


Fig.8 Test circuit FM mixer.

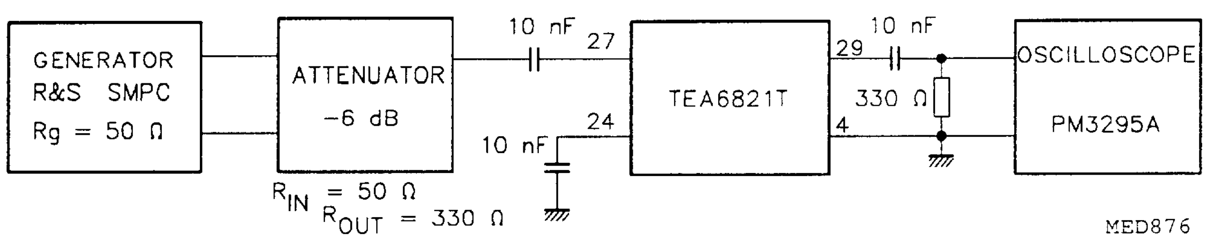


Fig.9 Test circuit IF amplifier.

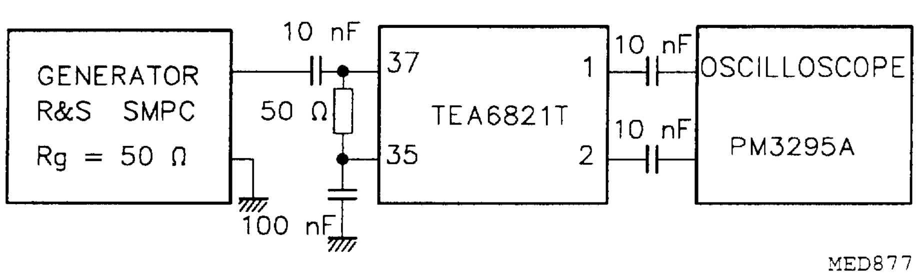


Fig.10 Test circuit limiter gain.

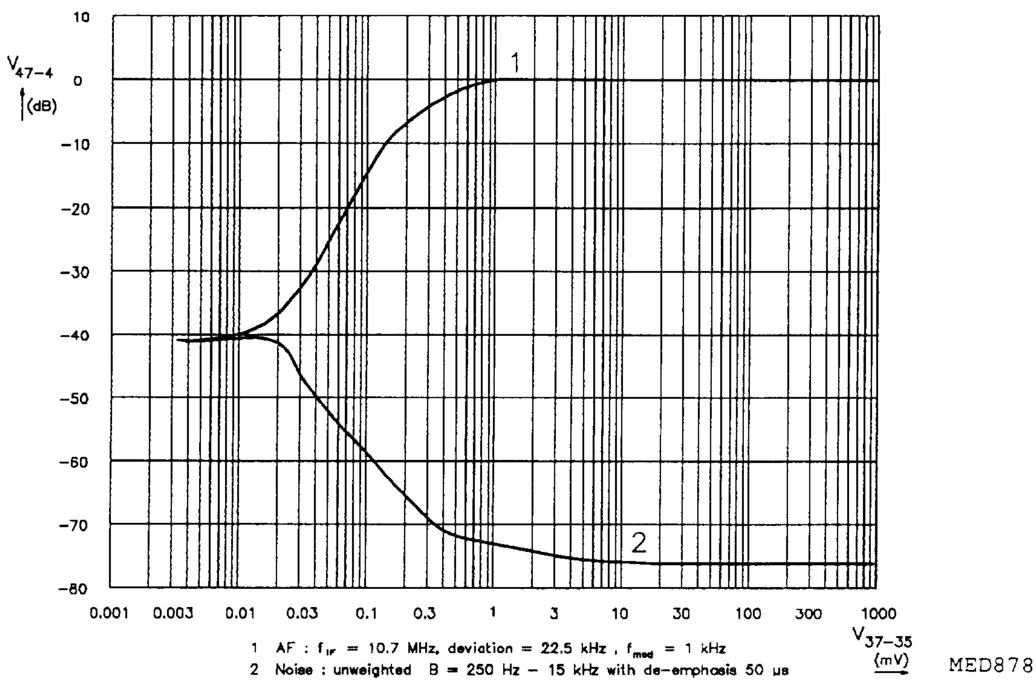


Fig.11 Signal and noise of muted MPX voltage.

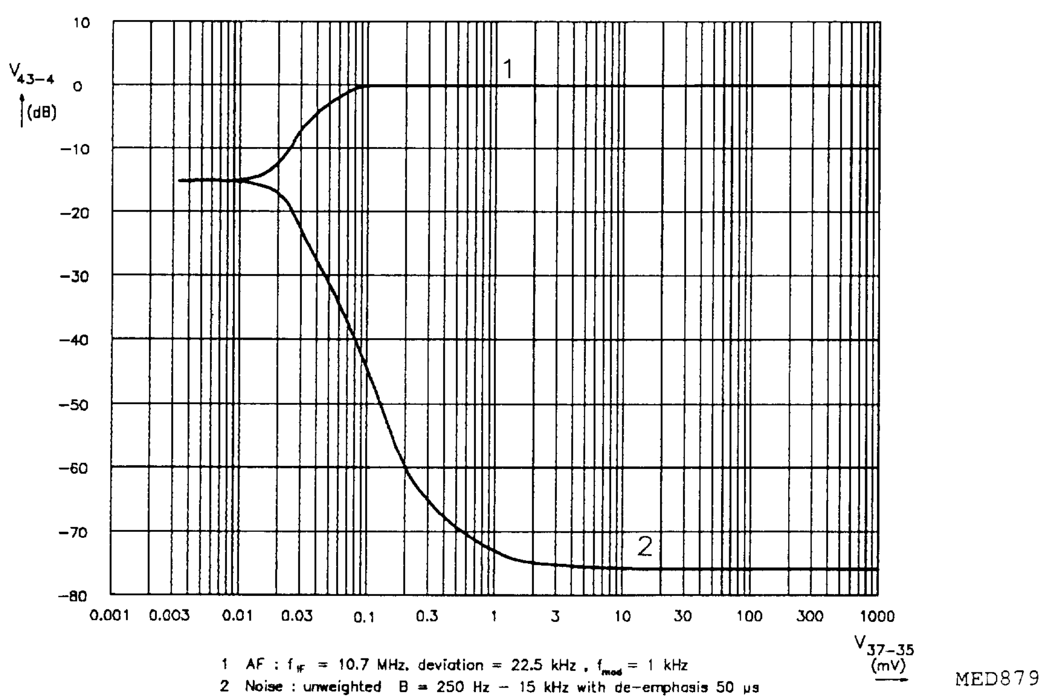


Fig.12 Signal and noise of unmuted MPX voltage.

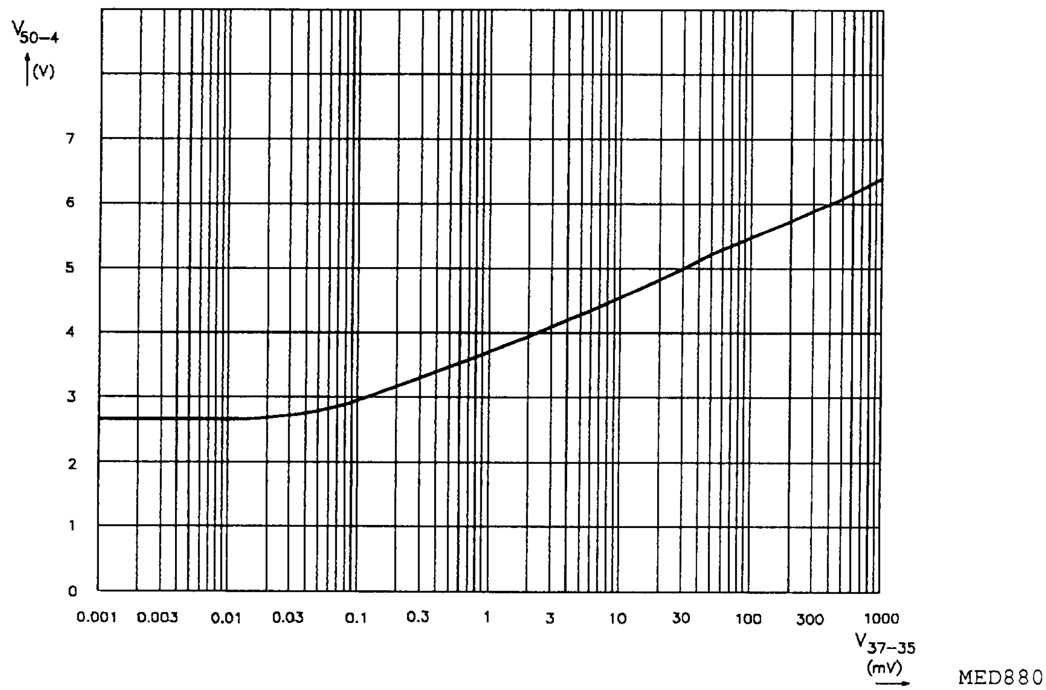


Fig.13 Level unweighted voltage (typical curve).

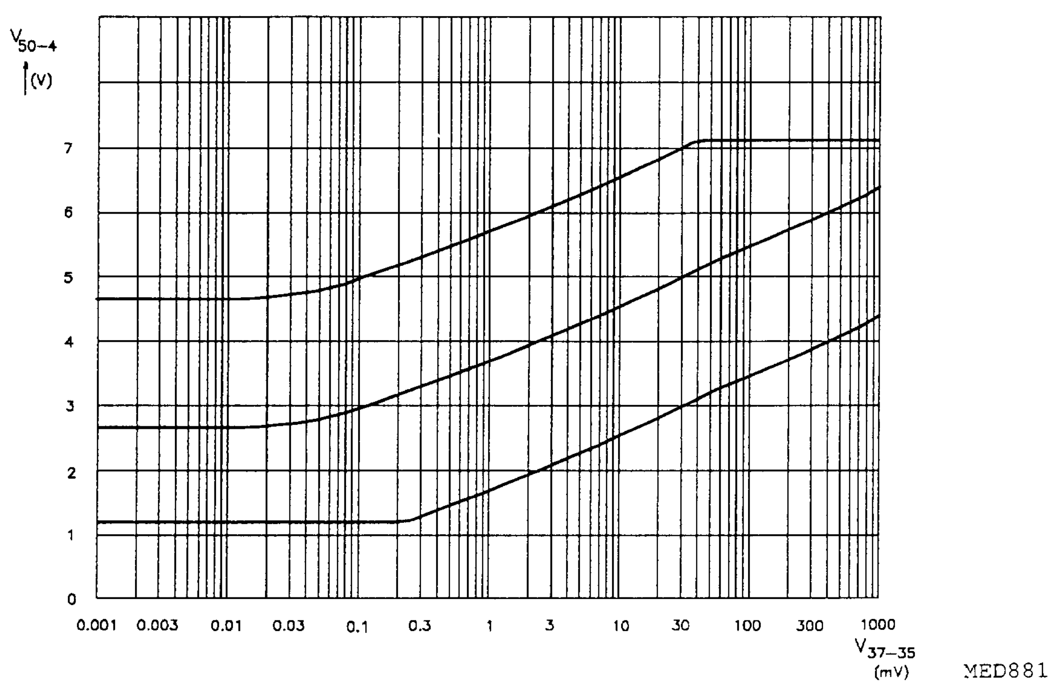


Fig.14 Adjustment range level unweighted voltage.

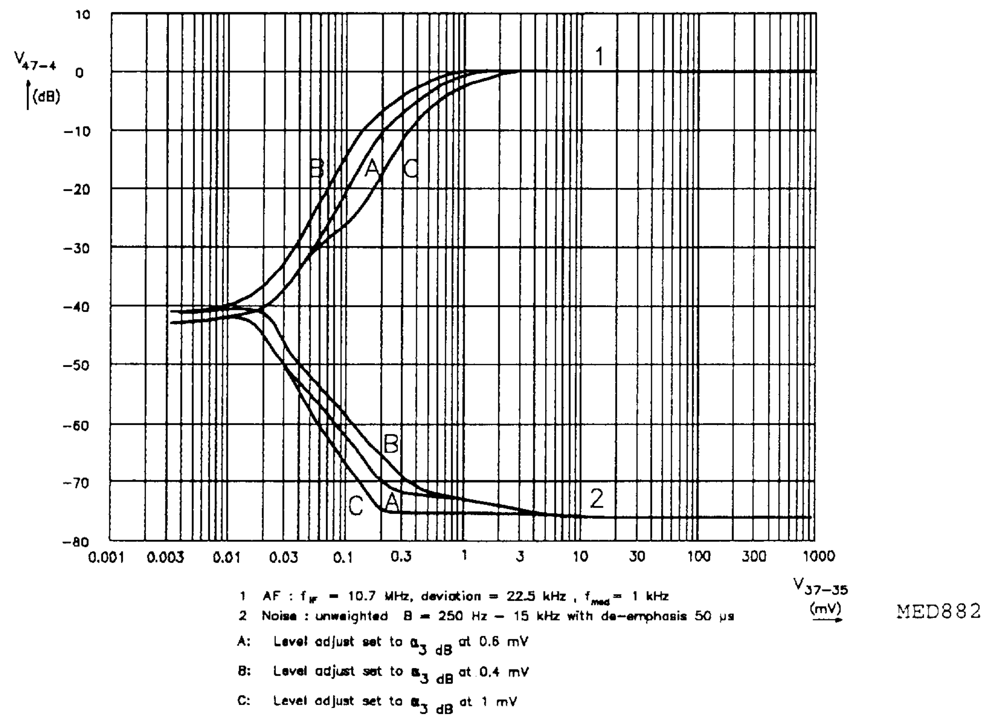


Fig.15 Muting dependence on adjust of level unweighted voltage (typical curve).

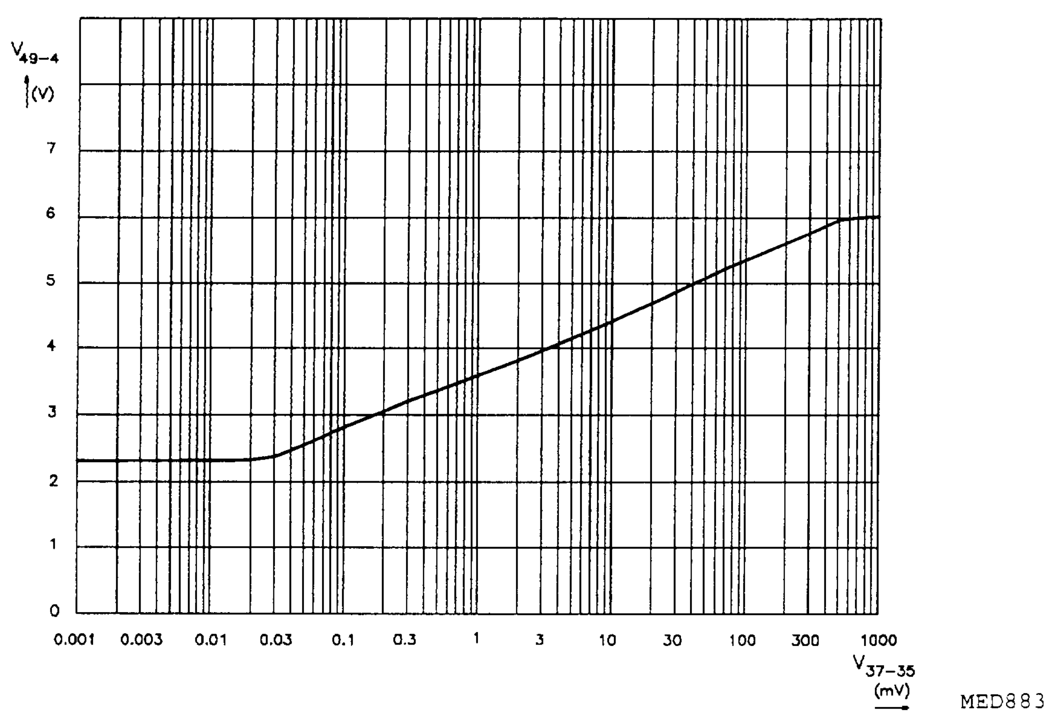


Fig.16 Typical mute voltage as function of FM IF_2 voltage.

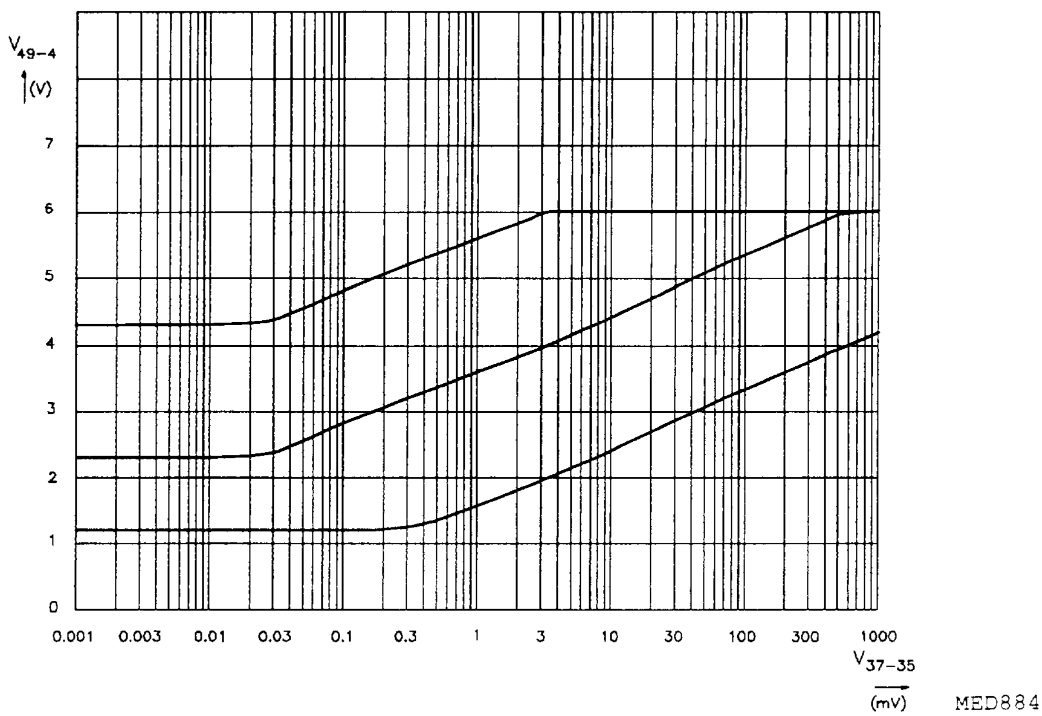


Fig.17 Adjustment range mute voltage.

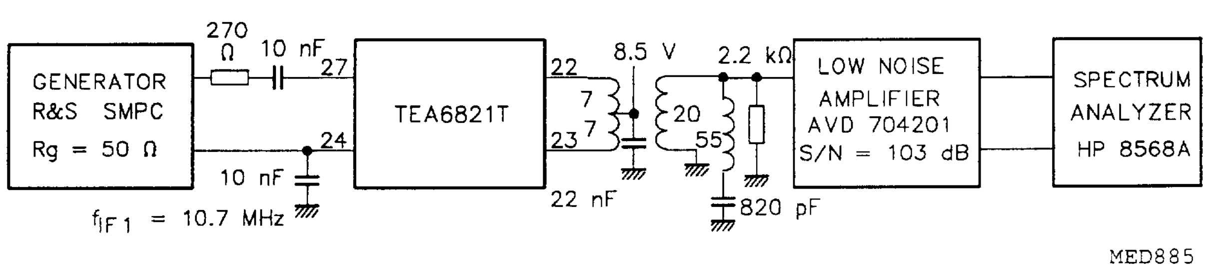


Fig.18 Test circuit AM mixer.

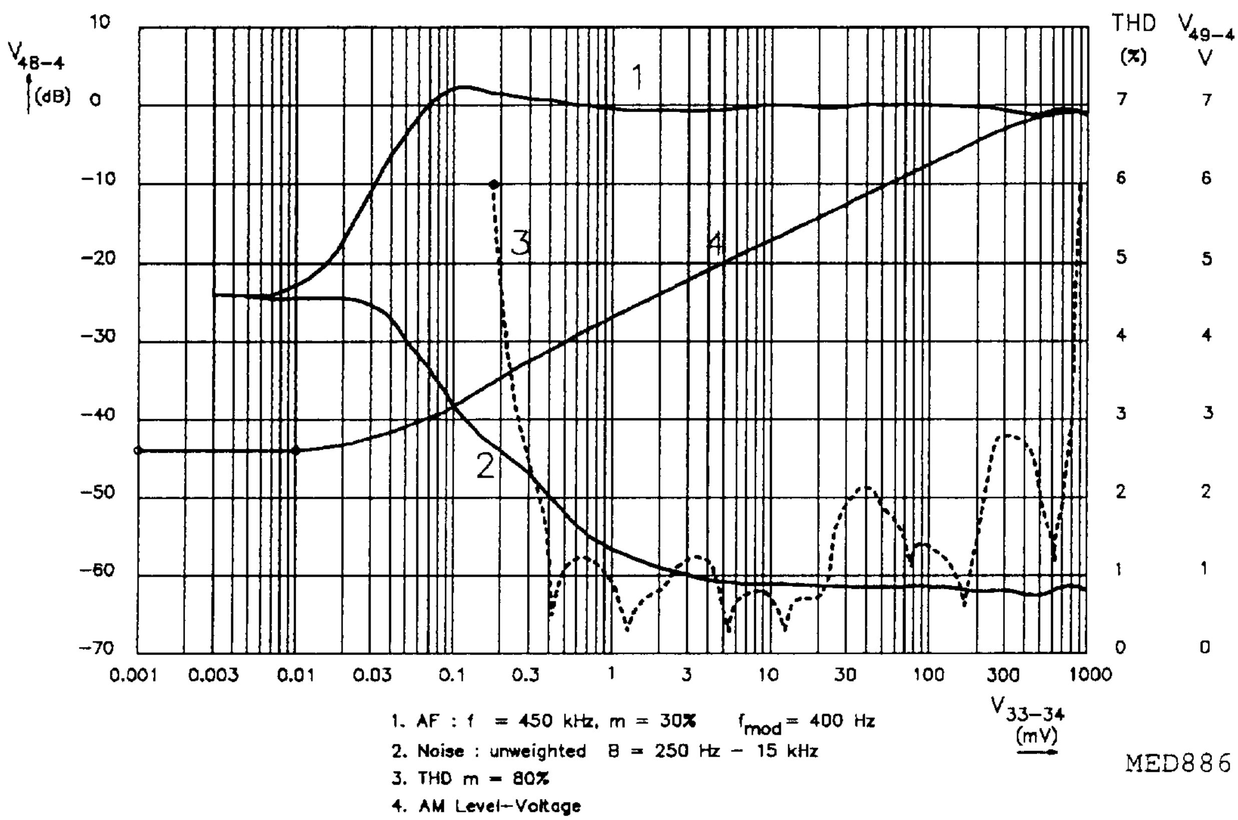


Fig.19 Signal, noise and distortion of AM AF output voltage and AM level voltage (typical curve).

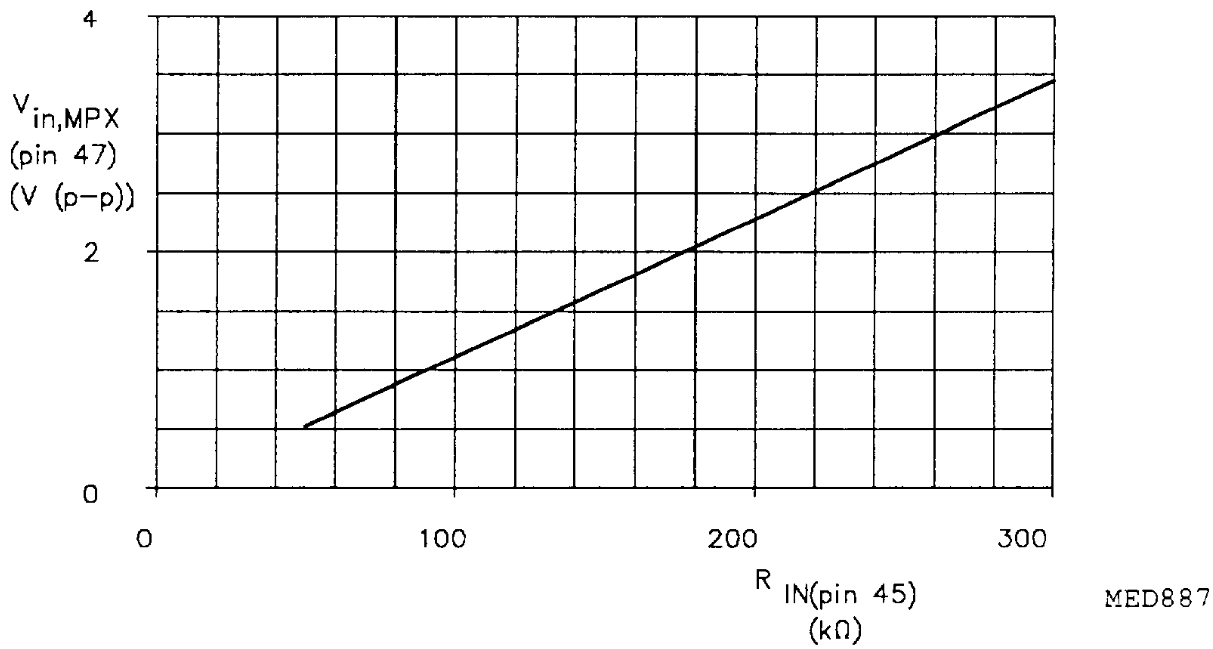


Fig.20 Adaption of MPX input to FM-demodulator output level by variation of the input resistor.

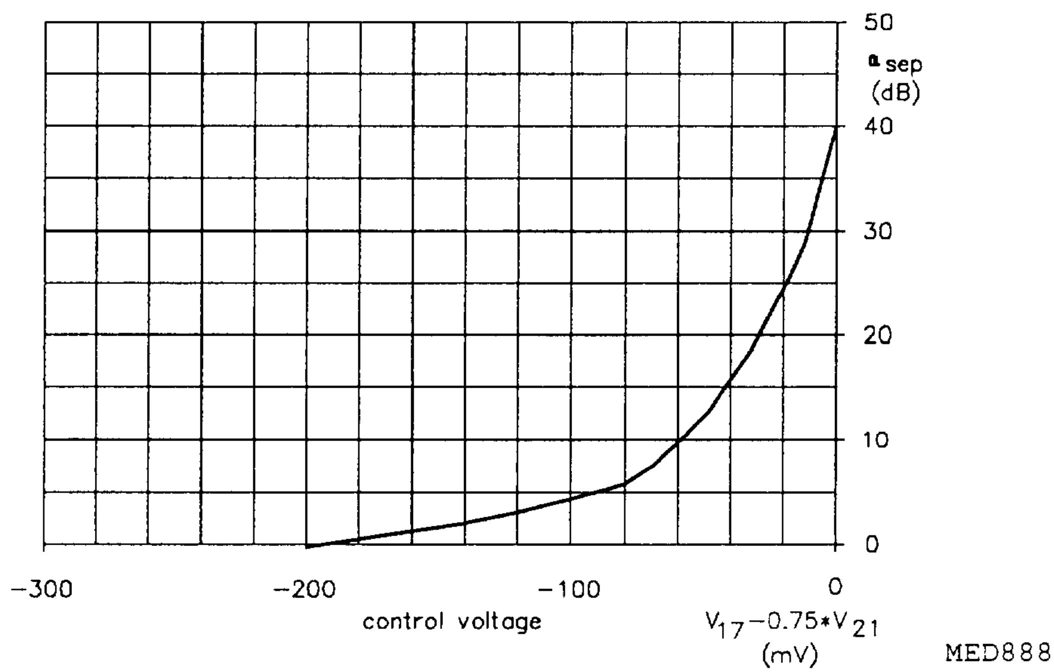


Fig.21 Channel separation as function of control voltage.

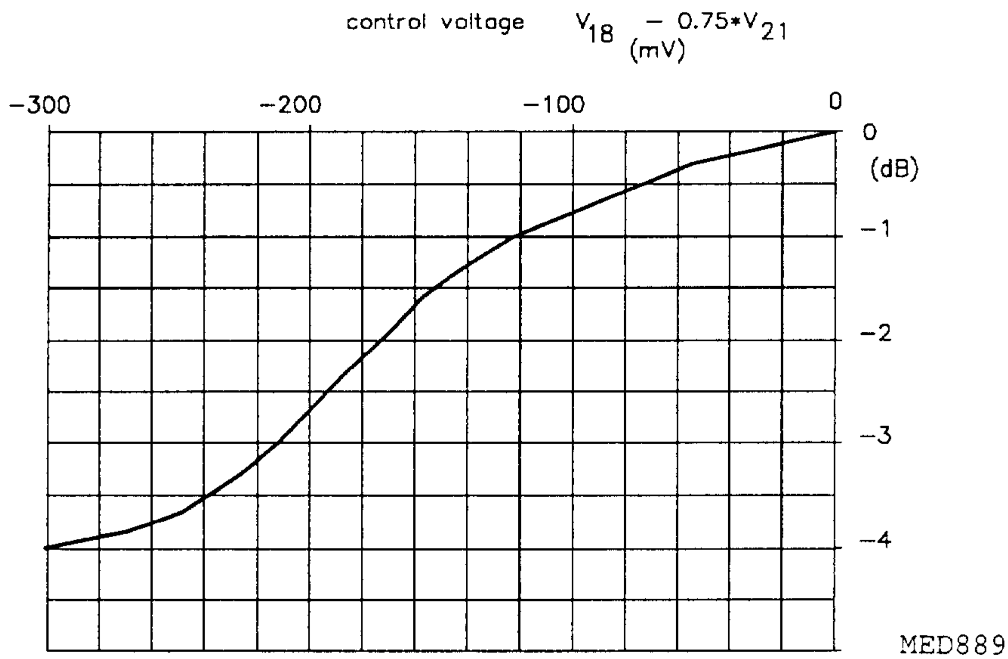


Fig.22 High-cut as function of control voltage.

I²C-BUS SPECIFICATION AND I²C-BUS CONTROLLED FUNCTIONS

I²C-bus specification

The standard I²C-bus specification is expanded by the following definitions. Structure of the I²C-bus logic: slave transceiver with auto increment and expansion to switch a direct transfer of all transmissions to an output for the radio front end IC (TEA6810T respectively TEA6811T). Subaddresses are not used. Data transfer to the TEA6821T Data sequence: address byte 1 byte 2 The data transfer has to be only in this order. The transfer direction of the data bytes is defined by the LSB of the address. The data becomes valid at the output of the internal latches with the acknowledge of each byte. A stop condition after any byte can shorten transmission times. When writing to the transceiver by using the stop condition before completion of the whole transfer:

- The remaining bytes will contain the old information
- If the transfer of a byte was not completed, this byte is lost and the previous information is available.

Data transfer to an output of the front end IC.

A data bit in the transceiver of the TEA6821T enables or disables a direct transfer of all transmissions to an interface stage for the front end IC.

For a transmission to the front end IC the address and the data format of the front end IC has to be used.
Hint: The pull-up resistors for the front end interface (pins 6 and 7) should not be connected to the 5 V supply voltage of the front end IC, otherwise a bus pull-down (pin 53) can occur during switching off the front end supply when the interface stage is enabled.
Data transfer to the IF IC (TEA6821T) is independent of the state of interface stage for the front end IC.

General specification

bus address of the TEA6821T	1100 001X
subaddress	not used
hardware (pin) programmable address bits	not available
default settings by power-on reset	radio mute and 40 ms IF count time is enabled, all other bits are random

I²C-bus data

Data to be received by the IC		
data byte 1	bit 0	switch for mono: bit 0 = 1; stereo: bit 0 = 0
	bit 1	LSB reference frequency for synthesizer; see Table 1
	bit 2	reference frequency for synthesizer; see Table 1
	bit 3	MSB reference frequency for synthesizer; see Table 1
	bit 4	tuning mute, bit 4 = 1: off; bit 4 = 0: on
	bit 5	SDS/SDR hold, bit 5 = 1: off; bit 5 = 0: on
	bit 6	radio mute, bit 6 = 1: off; bit 6 = 0: on
	bit 7	I²C-bus to front end, bit 7 = 1: enabled; bit 7 = 0: disabled
data byte 2	bit 0	AM/FM, bit 0 = 0: AM; bit 0 = 1: FM
	bit 1	divider for AM mixer, bit 1 = 0: division by 2; bit 1 = 1: division by 6
	bit 2	measure time IF count, bit 2 = 0: 40 ms; bit 2 = 1: 4 ms
	bit 3	SDR off, bit 3 = 0: SDR off; bit 3 = 1: SDR on
	bit 4	not used
	bit 5	not used
	bit 6	not used
	bit 7	not used
Data to be transmitted by the IC		
data byte 1(1)	bit 0	LSB level information
	bit 1	level information
	bit 2	MSB level information
	bit 3	LSB multipath information
	bit 4	multipath information
	bit 5	MSB multipath information
	bit 6	bit 6 = 1: stereo pilot presence
	bit 7	not used

data byte 2	bit 0	LSB of the IF-counter
	bit 1	IF-counter
	bit 2	IF-counter
	bit 3	IF-counter
	bit 4	IF-counter
	bit 5	IF-counter
	bit 6	IF-counter
	bit 7	MSB of the IF-counter

Note

1. The A/D conversion for multipath and level will be done while a transmission of any address to the I^2C-bus.

Table 1 Reference frequency setting in byte 1

BIT 3	BIT 2	BIT 1	REFERENCE FREQUENCY
0	0	0	3 kHz
0	0	1	5 kHz
0	1	0	10 kHz
0	1	1	15 kHz
1	0	0	25 kHz
1	0	1	50 kHz
1	1	0	not defined
1	1	1	not defined

Reference frequency generation; note 1

DIVISION RATIO	REFERENCE FREQUENCY (kHz)
20500	3
12300	5
6150	10
4100	15
2460	25
1230	50

Note

1. All specified frequencies are valid for a crystal oscillator frequency of 61.5 MHz.

Output signal of reference frequency divider

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
C_{10-4}, C_{11-4}	output capacitance	–	–	4	pF
R_{10-52}, R_{11-52}	output resistance	800	1000	1200	Ω
V_{10-11}	differential output voltage (peak-to-peak value)	0.3	0.4	0.5	V
V_{10-4}, V_{11-4}	single-ended output voltage (peak-to-peak value)	0.15	0.2	0.3	V

IF-counter; note 1

SYMBOL	PARAMETER	MIN.	UNIT
V_{33-34}	IF-counter sensitivity for AM, m = 0	200	μV
V_{37-35}	IF-counter sensitivity for FM	200	μV

Note

1. Counting windows AM: 4 ms, (40 ms); FM: 40 ms, 4 ms
   Counting resolution AM: 250 Hz, (25 Hz); FM: 5 kHz, 50 kHz
   IF-prescaler AM: division by 1; FM: division by 200

The IF-count windows are valid for a crystal oscillator frequency of 61.5 MHz.
The FM/AM switching is done by bit 0 of byte 2 of the received data of the IC.
The IF-counter operates continuously.
The IF-counter and window-counter will be resetted when the I^2C-bus logic detects the address of the IC. This disables changes in the latches for the IF-count, while reading this value. If the transmission to the front end IC will be disabled after the synthesizer loop of the TEA6811T front end IC has locked for a new frequency, the IF-count will be available after the set measuring time.
The IF-counter starts at 0. The IF-counter output are the **8 least significant bits** of the counting result.

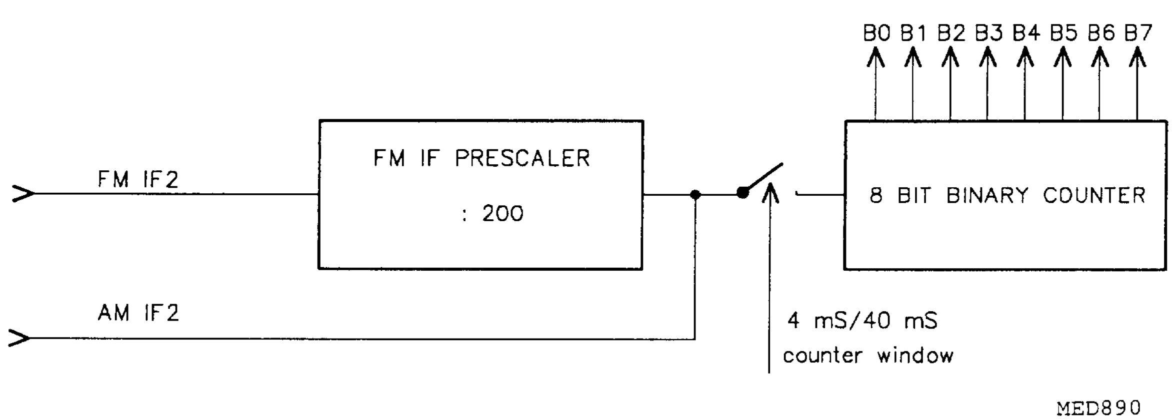
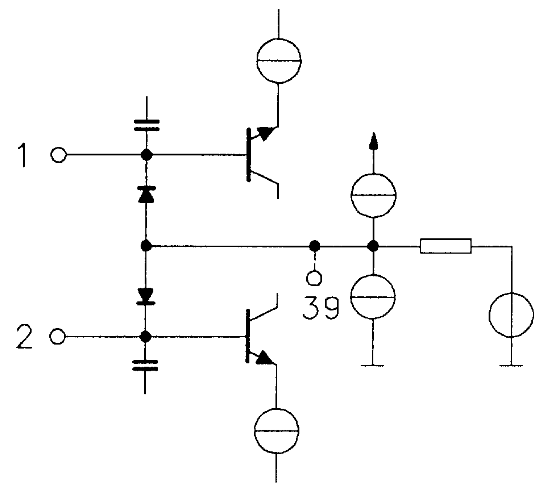
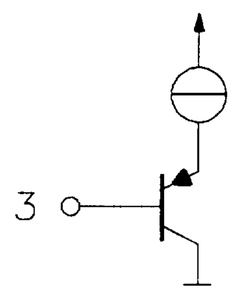
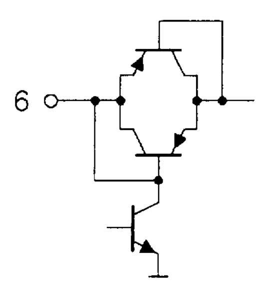


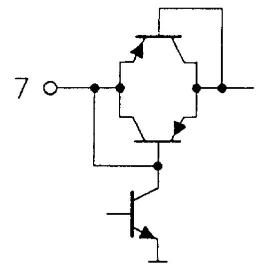
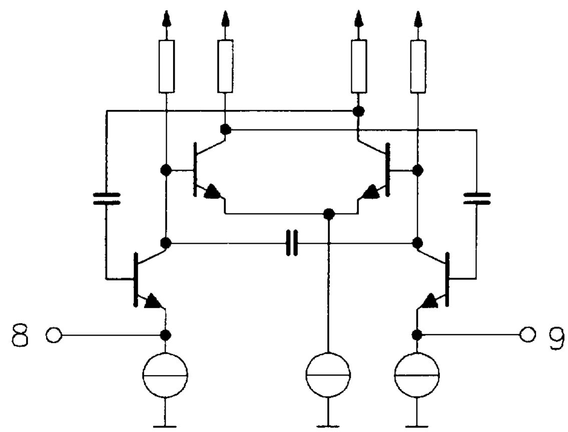
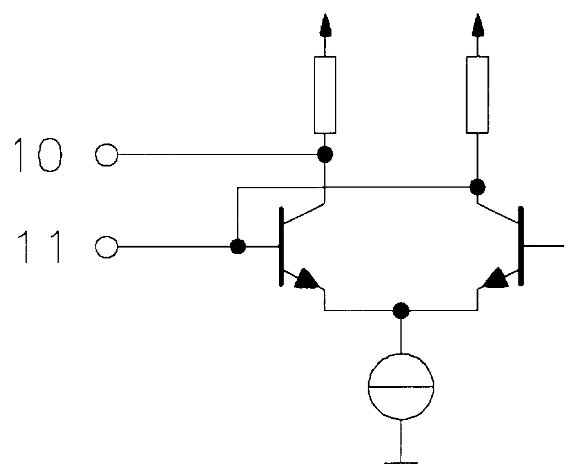
Fig.23 IF-counter structure.

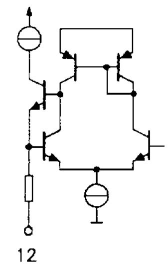
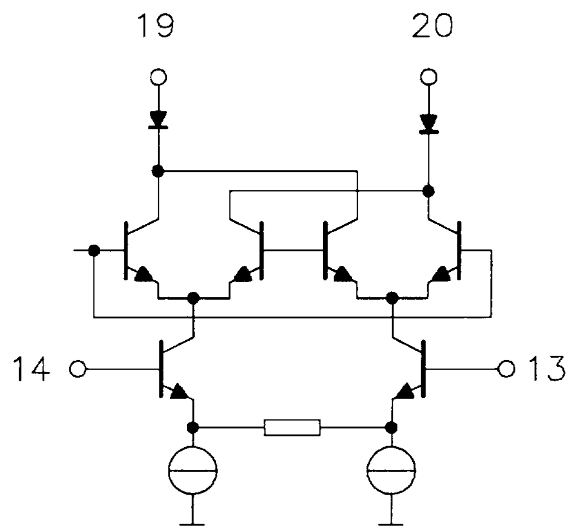
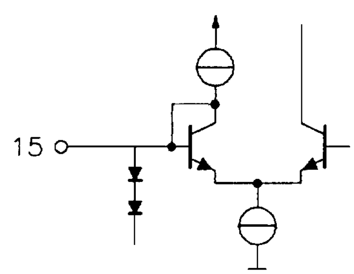
A/D converters for level and multipath voltage

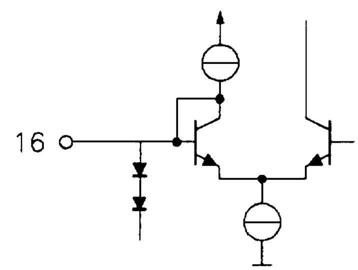
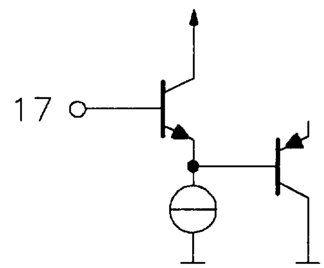
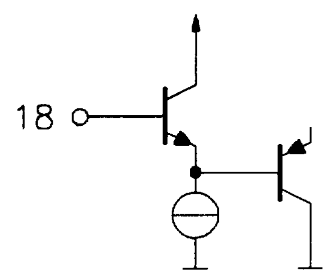
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
A/D converter for FM level information					
The FM level information $V_{50\text{-}3}$ is A/D converted with 3 bit					
$\Delta V_{50\text{-}4}$	AD conversion step size	–	6	–	dB/step
FM stop					
ΔV_{stop}	variation of stop level as function of $V_{42\text{-}4}$	–	30	–	dB/V
A/D converter for AM level information					
The AM level information $V_{49\text{-}4}$ is A/D converted with 3 bit					
$\Delta V_{49\text{-}4}$	AD conversion step size	–	6	–	dB/step
AM stop					
ΔV_{stop}	variation of stop level as function of $V_{43\text{-}4}$	–	30	–	dB/V
A/D converter for multipath information					
The multipath information $V_{40\text{-}4}$ is A/D converted with 3 bit covering an IF_2 amplitude modulation range $0.15 \leq m \leq 0.9$; f_{mod} = 20 kHz					
m	multipath conversion step 0	–	–	–	%
	multipath conversion step 1	–	15	–	%
	multipath conversion step 2	–	30	–	%
	multipath conversion step 3	–	40	–	%
	multipath conversion step 4	–	50	–	%
	multipath conversion step 5	–	58	–	%
	multipath conversion step 6	–	66	–	%
	multipath conversion step 7	–	74	–	%

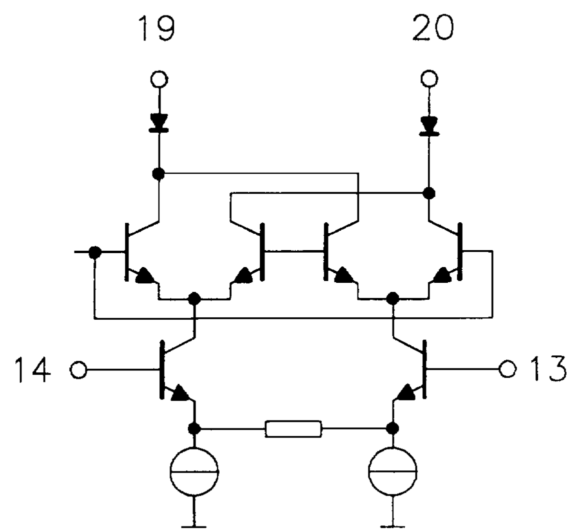
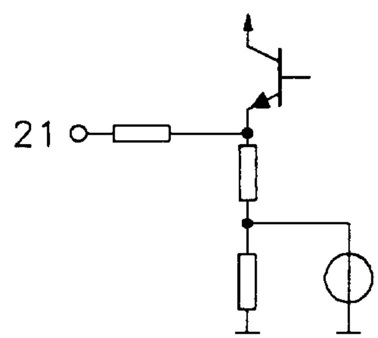
Table 2 Equivalent pin circuits and pin voltages.

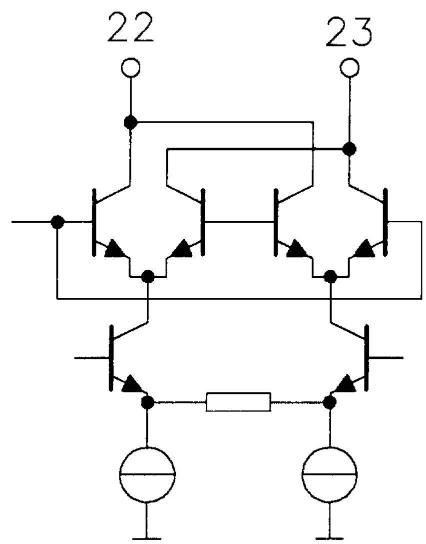
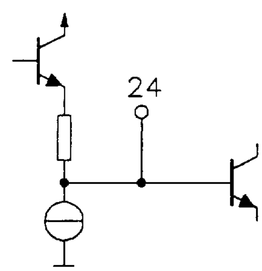
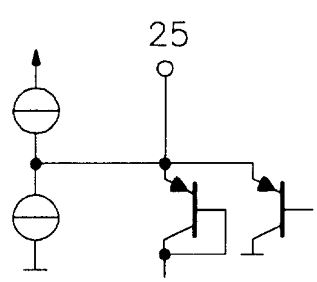
PIN NO.	PIN NAME	DC VOLTAGE (V)		INTERNAL CIRCUIT
		AM	FM	
1	QDET1	4.0	4.0	
2	QDET2	4.0	4.0	
3	TSWITCH	open	$0/V_{21}$	
4	GND			
5	V_{P5}	5.0	5.0	
6	HFBUS1	5.0	5.0	

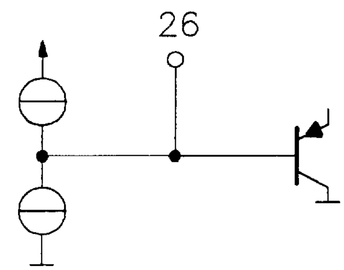
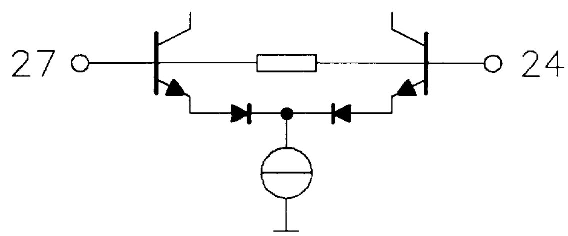
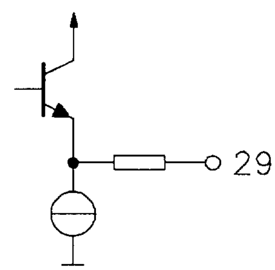
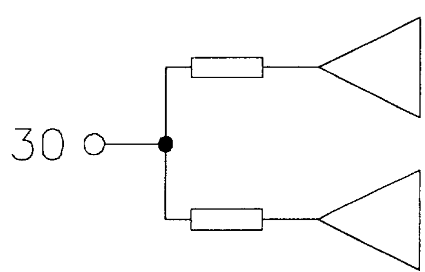
PIN NO.	PIN NAME	DC VOLTAGE (V)		INTERNAL CIRCUIT
		AM	FM	
7	HFBUS2	5.0	5.0	
8	XTAL1	4.1	4.1	
9	XTAL2	4.1	4.1	
10	F_{REFP}	4.9	4.9	
11	F_{REFN}	4.9	4.9	

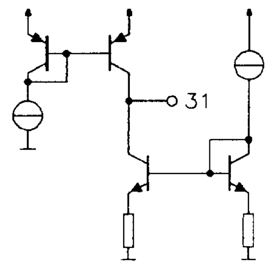
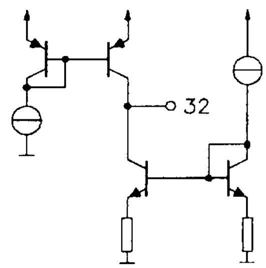
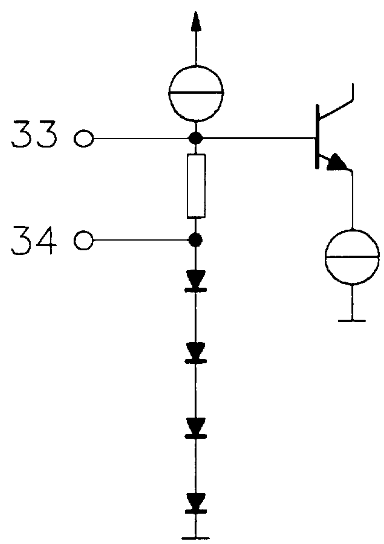
PIN NO.	PIN NAME	DC VOLTAGE (V)		INTERNAL CIRCUIT
		AM	FM	
12	I_{REF}	4.3	4.3	
13	FMIFIN1	2.3	2.3	
14	FMIFIN2	2.3	2.3	
15	TSDR	0.7 – 5.5	0.7 – 5.5	

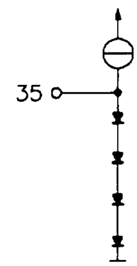
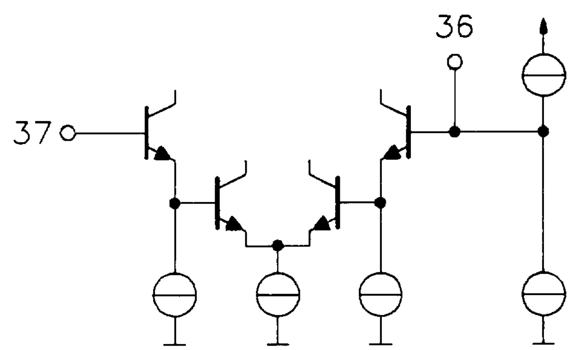
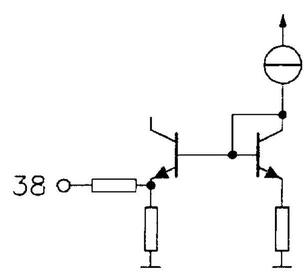
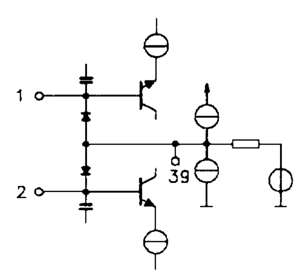
PIN NO.	PIN NAME	DC VOLTAGE (V)		INTERNAL CIRCUIT
		AM	FM	
16	TSDS	0.7 – 5.5	0.7 – 5.5	
17	V_{SDS}	3.0 – 5.5	3.0 – 5.5	
18	V_{SDR}	3.0 – 5.5	3.0 – 5.5	

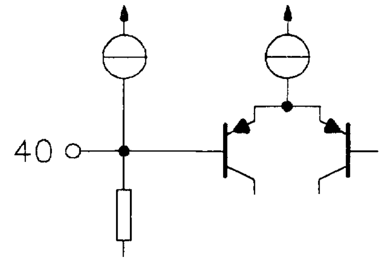
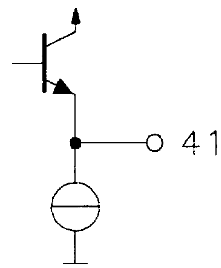
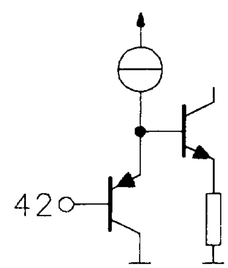
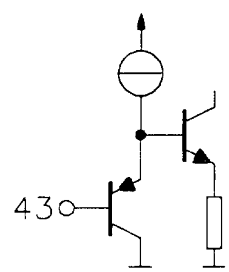
PIN NO.	PIN NAME	DC VOLTAGE (V)		INTERNAL CIRCUIT
		AM	FM	
19	FMIF2OUT1	8.5	8.5	
20	FMIF2OUT2	8.5	8.5	
21	V_{REF}	5.1	5.1	

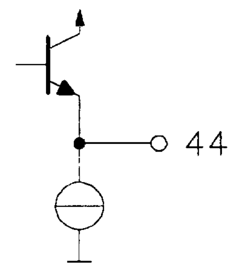
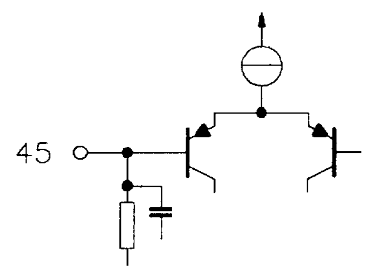
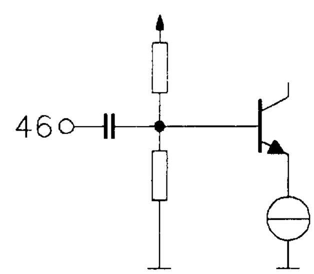
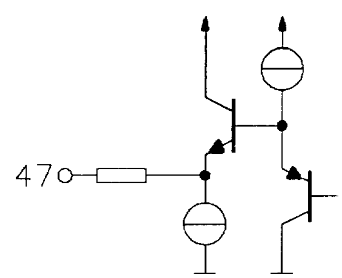
PIN NO.	PIN NAME	DC VOLTAGE (V)		INTERNAL CIRCUIT
		AM	FM	
22	AMIF2OUT1	8.5	8.5	
23	AMIF2OUT2	8.5	8.5	
24	FMAMDEC	3.0	3.0	
25	PHASEDET	3.0 – 7.0	3.0 – 7.0	

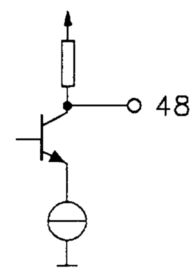
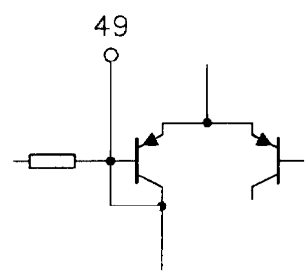
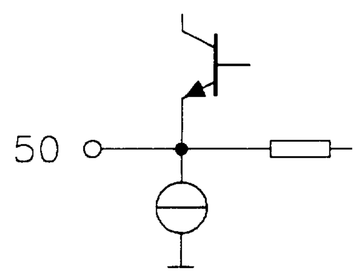
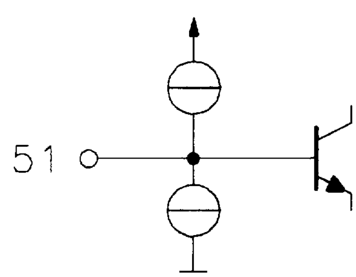
PIN NO.	PIN NAME	DC VOLTAGE (V)		INTERNAL CIRCUIT
		AM	FM	
26	PILDET	0.7	0.7 – 7.0	
27	FMAM10.7	3.0	3.0	
28	V_{PIF}	8.5	8.5	
29	FMIFAMPOUT	6.0	6.0	
30	AFGND	3.6	3.6	

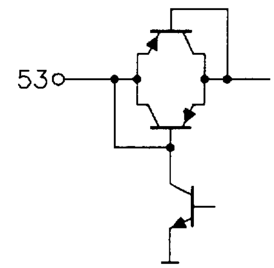
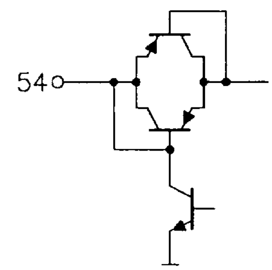
PIN NO.	PIN NAME	DC VOLTAGE (V)		INTERNAL CIRCUIT
		AM	FM	
31	DEEMPHR	2.3	2.3	
32	DEEMPHL	2.3	2.3	
33	AMIF2IN1	2.7	0.7	
34	AMIF2IN2	2.7	0.7	

PIN NO.	PIN NAME	DC VOLTAGE (V)		INTERNAL CIRCUIT
		AM	FM	
35	FMIN2	0.7	2.7	
36	DCFEED	2.7	2.7	
37	FMIN1	0.7	2.7	
38	LEVELADJ	2.6	2.6	
39	C_{AFC}	1.0 – 2.2	1.0 – 7.0	

PIN NO.	PIN NAME	DC VOLTAGE (V)		INTERNAL CIRCUIT
		AM	FM	
40	MPBUF	0.7 – 6.0	0.7 – 6.0	
41	OUTLEFT	3.6	3.6	
42	FMSTOP	0 – 5.2	0 – 5.2	
43	RDS/AMSTOP	0 – 5.2	3.0	

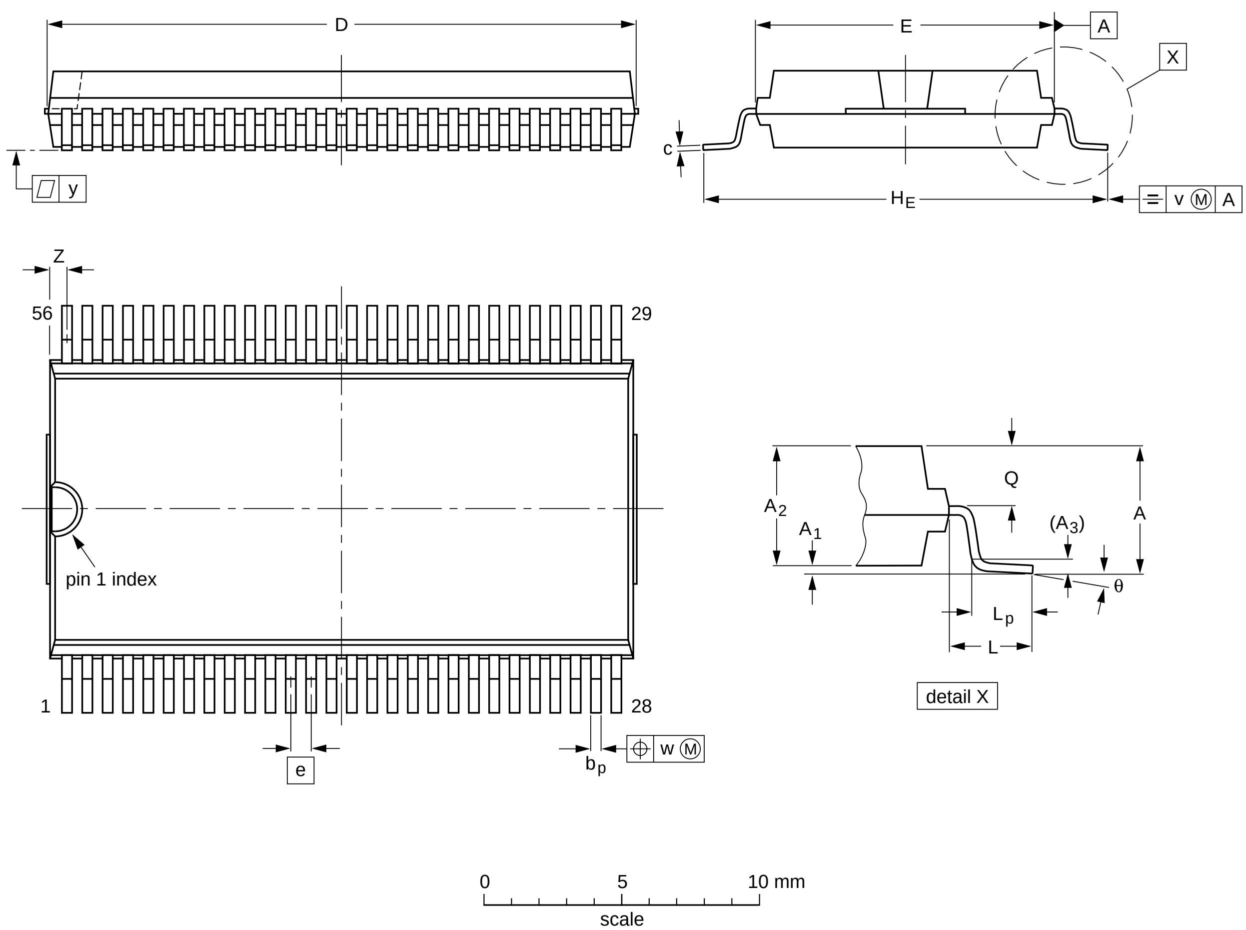
PIN NO.	PIN NAME	DC VOLTAGE (V)		INTERNAL CIRCUIT
		AM	FM	
44	OUTRIGHT	3.6	3.6	
45	MPXIN	2.8	2.8	
46	IAC_{IN}	0	0	
47	MPXOUT	0	3.0	

PIN NO.	PIN NAME	DC VOLTAGE (V)		INTERNAL CIRCUIT
		AM	FM	
48	AMAFOUT	3.7	4.8	
49	V_{MUTAML}	1.0 – 5.5	1.0 – 5.5	
50	LEVELUNWEIG	1.0 – 7.0	1.0 – 7.0	
51	$I_{ACCONTR}$	0	6.0	
52	V_{PDIG}	5.0	5.0	

PIN NO.	PIN NAME	DC VOLTAGE (V)		INTERNAL CIRCUIT
		AM	FM	
53	SDA	5.0	5.0	
54	SCL	5.0	5.0	
55	BUSGND	0	0	
56	$V_{P8.5}$	8.5	8.5	

PACKAGE OUTLINE

VSO56: plastic very small outline package; 56 leads **SOT190-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	3.3	0.3 0.1	3.0 2.8	0.25	0.42 0.30	0.22 0.14	21.65 21.35	11.1 11.0	0.75	15.8 15.2	2.25	1.6 1.4	1.45 1.30	0.2	0.1	0.1	0.90 0.55	7° 0°
inches	0.13	0.012 0.004	0.12 0.11	0.01	0.017 0.012	0.0087 0.0055	0.85 0.84	0.44 0.43	0.0295	0.62 0.60	0.089	0.063 0.055	0.057 0.051	0.008	0.004	0.004	0.035 0.022	

Note

1. Plastic or metal protrusions of 0.3 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT190-1						~~96-04-02~~ 97-08-11

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *“IC Package Databook”* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all VSO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all VSO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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