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APPLICATION NOTE

Designing Expansion Boards for the Motorola MPC555EVB/ETAS ES200

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1 Introduction

The Motorola MPC555EVB/ETAS ES200 evaluation board was designed with multiple interfaces to allow flexibility for expansion. There are three sets of connectors for expansion. The MAPI-400+100 is on the bottom side of the board and has access to all signals required to interface to a user application board. The host communication expansion (HCE) connectors allow access to the bus of the MPC555. The customized communication expansion (CCE) allows access to some of the MPC555 on-chip communication ports. The HCE and the CCE are on the top side of the EVB555.

2 The Host Communication Expansion Connector (HCE)

The host communication expansion connectors on the EVB555 are designed for use as an expansion of the external bus of the MPC555. They could be used to add additional memory or additional peripherals. There are two 60-pin connectors (CO106 – A and CO107 – B) part number Samtec TFM-130-12-S-D-P. The matching connector required on the expansion board is SFM-130-02-S-D-P. The pin-out of the HCE is shown in **Table 1.** The two connectors are mounted on 1.8 inch (45.72 mm) centers. This allows for a board of approximately three square inches.

NOTE

An ETAS ETK interface may be mounted above the HCE board. The total height (including the connectors on the EVB555 and all components on the HCE board) must be below 0.6875 inches to allow clearance of the ETK board.

2.1 Memory Chips On The HCE

All 32 bits of the MPC555 data bus are available on the HCE connectors. Memory boards designed for these connectors should use all 32 bits for the best performance. On a full-featured board, utilizing memories less than 32 bits wide, the memory can be implemented with multiple chips. For 16-bit wide memories, two chips should be used. Provisions should be made on the expansion board to allow the second memory to be disabled to allow for smaller bus widths on the EVB555. 16-bit only memories should be connected to D0-D15 of the data bus. $\overline{CS}$[2] is available for use on the HCE board. If non-volatile memories are used, $\overline{CS}$[0] could also be used to allow for booting from the external memory. (It is not possible to boot from the Texas Instruments TMS28F033 on the EVB555.) If $\overline{CS}$[0] is used, the TMS28F033 can be disabled by using the $\overline{SGF\_SEL}$ signal on pin 160 of the ETK connector (CO508). A logic high (default) enables the EVB555 on-board external flash memory. In addition, $\overline{CSHCE}$ could be used if the chip timing is the same as used by the memory on the EVB555 and can fit in a 1-Mbyte memory size.

2.2 Peripherals On The HCE

Peripherals can also be added on to the HCE bus. Chip selects $\overline{CS}$[2] and $\overline{CS}$[3] are available on the HCE connectors. In addition, $\overline{CSHCE}$ could be used if the chip timing is the same as used by the memory on the EVB555 and can fit in a 1-Mbyte memory size. Peripherals that could be added include more serial ports, an ethernet adapter, or USB circuitry.

Table 1 Host Communication Expansion Connector

A (CO106)					B (CO107)				
PIN NAME				PIN NAME	PIN NAME				PIN NAME
VCC3_3	1	•	•	2	VCC3_3	VCC3_3	1	•	•	2	VCC3_3
VCC[5]	3	•	•	4	VCC[5]	VSTBY3_3	3	•	•	4	VCC5
SDATA[31]	5	•	•	6	SDATA[30]	SADDR[31]	5	•	•	6	SADDR30
SDATA[29]	7	•	•	8	SDATA[28]	SADDR[29]	7	•	•	8	SADDR28
SDATA[27]	9	•	•	10	SDATA[26]	SADDR[27]	9	•	•	10	SADDR26
SDATA[25]	11	•	•	12	SDATA[24]	SADDR[25]	11	•	•	12	SADDR24
SDATA[23]	13	•	•	14	SDATA[22]	SADDR[23]	13	•	•	14	SADDR22
SDATA[21]	15	•	•	16	SDATA[20]	SADDR[21]	15	•	•	16	SADDR20
SDATA[19]	17	•	•	18	SDATA[18]	SADDR[19]	17	•	•	18	SADDR18
SDATA[17]	19	•	•	20	SDATA[16]	SADDR[17]	19	•	•	20	SADDR16
SDATA[15]	21	•	•	22	SDATA[14]	SADDR[15]	21	•	•	22	SADDR14
SDATA[13]	23	•	•	24	SDATA[12]	SADDR[13]	23	•	•	24	SADDR12
SDATA[11]	25	•	•	26	SDATA[10]	SADDR[11]	25	•	•	26	SADDR10
SDATA[9]	27	•	•	28	SDATA[8]	SADDR[9]	27	•	•	28	SADDR8
SDATA[7]	29	•	•	30	SDATA[6]	GND	29	•	•	30	GND
SDATA[5]	31	•	•	32	SDATA[4]	N/C	31	•	•	32	$\overline{CSHCE}$
SDATA[3]	33	•	•	34	SDATA[2]	$\overline{CS}$[0]	33	•	•	34	$\overline{CS1}$
SDATA[1]	35	•	•	36	SDATA[0]	$\overline{CS}$[2]	35	•	•	36	$\overline{CS3}$
GND	37	•	•	38	GND	$\overline{OE}$	37	•	•	38	RD/$\overline{WE}$
N/C	39	•	•	40	N/C	N/C	39	•	•	40	N/C
$\overline{WE}$/AT[0]	41	•	•	42	$\overline{WE}$/AT[1]	$\overline{BURST}$	41	•	•	42	$\overline{BDIP}$
$\overline{WE}$/AT[2]	43	•	•	44	$\overline{WE}$/AT[3]	TP113	43	•	•	44	N/C
N/C	45	•	•	46	N/C	$\overline{TA}$	45	•	•	46	$\overline{TEA}$
TSIZ1	47	•	•	48	TSIZ0	$\overline{TS}$	47	•	•	48	$\overline{BI}$/$\overline{STS}$
N/C	49	•	•	50	N/C	TP114	49	•	•	50	N/C
$\overline{PORESET}$	51	•	•	52	$\overline{SRESET}$	$\overline{BB}$/VF[2]/IWP[3]	51	•	•	52	$\overline{BR}$/VF[1]/IWP[2]
N/C	53	•	•	54	TP108	$\overline{BG}$/VF[0]/LWP[1]	53	•	•	54	FRZ/PTR
TP109	55	•	•	56	TP110	CLKOUT	55	•	•	56	TP115
TP111	57	•	•	58	TP112/$\overline{DIS}$[1]	TP116	57	•	•	58	TP117
GND	59	•	•	60	GND	GND	59	•	•	60	GND

NOTES:

1. EVB555 boards (revision 1.1/1.2) can be modified by connecting pin 58 (TP112) to pin 78 ($\overline{DIS}$) of the TI Flash (IC400). This allows the TI Flash to be disabled and $\overline{CS}$[0] to be useable by other devices. TP112 can then be pulled to ground through a 2KΩ resistor. In addition, pin 6 of IC403 (/SGEOF) should be connected to pin 17 of RN303, a spare pullup resistor, to prevent the floating input of IC403.
   NOTE: these changes disable the external reset configuration word drivers on the EVB555 and may cause limitations with the ETAS ETK.

2.3 HCE Board Dimensions

Figure 1 and Table 2 show the maximum board dimensions for boards designed to interface to the HCE connectors. Surface mount components should be used to keep the total height of the HCE board and connectors to 0.6875 inches (17.46 mm) to avoid interference with the optional ETAS ETK interface.

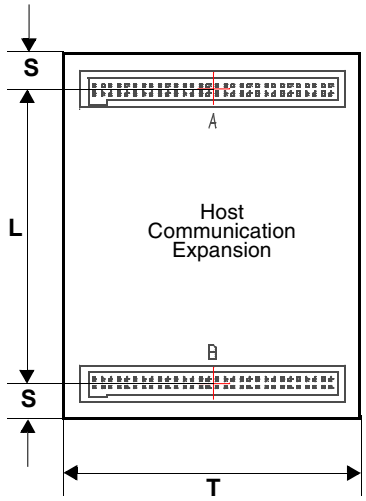

Figure 1 HCE Board Layout

Table 2 HCE Board Dimensions

Dimension	Millimeters	Inches
L	45.72	1.800
S	6.35	0.250
T	44.45	1.75

3 The Customized Communication Expansion Connectors (CCE)

The customized communication expansion connectors on the EVB555 allows access to the MPC555 on-chip communication ports. The EVB555 provides for RS-232 drivers and DB9 connector for the SCI1 channel of the MPC555. The CCE allows for customized connections to all of the MPC555 QSMCM and TouCAN interfaces. There are two 20-pin connectors (CO104 – A and CO105 – B) part number Samtec TFM-110-12-S-D-P. The matching connector required on the expansion board is SFM-110-02-S-D-P. The pin-out of the CCE is shown in Table 3.

NOTE

The TXD1 and RXD1 are, by default, connected to the on board RS-232 driver. These can optionally be brought to the TXD_CCE (7) and RXD_CCE (8) pins of connector CO105 by changing the position of the 0Ω resistors on BR100 and BR101 from position 1-2 to position 2-3.

Table 3 Customized Communication Expansion Connector

A (CO104)						B (CO105)					
PIN NAME					PIN NAME	PIN NAME					PIN NAME
VCC3_3	1	•	•	2	VCC3_3	VCC3_3	1	•	•	2	VCC3_3
VCC5	3	•	•	4	VCC5	VCC5	3	•	•	4	VSTBY3_3
N/C	5	•	•	6	CLKOUT	N/C	5	•	•	6	N/C
B_CNTX0	7	•	•	8	B_CNRX0	TXD_CCE	7	•	•	8	RXD_CCE
TP100	9	•	•	10	TP101	ECK	9	•	•	10	TP104
GND	11	•	•	12	GND	GND	11	•	•	12	GND
A_CNTX0	13	•	•	14	A_CNRX0	TP105	13	•	•	14	TP106
TP102	15	•	•	16	TP103	TXD2	15	•	•	16	RXD2
$\overline{\text{SRESET}}$	17	•	•	18	$\overline{\text{PORESET}}$	TP107	17	•	•	18	TP118
GND	19	•	•	20	GND	GND	19	•	•	20	GND

3.1 CCE Board Dimensions

Figure 2 and Table 4 show the maximum board dimensions for boards that attach the EVB555 CCE connector.

NOTE

Boards can extend off of the EVB for connectors. It is recommended that mounting hardware be supplied to attach the CCE board to the EVB.

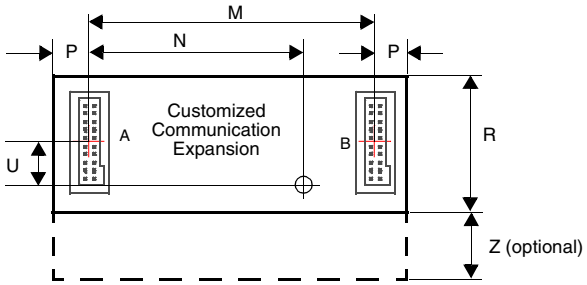

Figure 2 CCE Board Size

Table 4 CCE Board Dimensions

Dimension	Millimeters	Inches
M	44.45	1.750
N	32.385	1.275
U	6.35	0.25
P	6.35	0.250
R	22.23	0.875
Z	12.7	0.50

4 The MAPI-400+100 Connectors

The MAPI-400+100 is an extension of the Motorola MAPI-400 interface that is used on the Motorola M•Core products. An additional 100 pin connector was added to support the additional general purpose Input/Output pins from the Port Replacement Unit of the EVB555.

NOTE

Boards designed to interface to M•Core MAPI-400 boards may not work with the EVB555.

Use of the MAPI-400 signals on the EVB555 is described in the ETAS ***EVB555 Quick Reference Guide***.

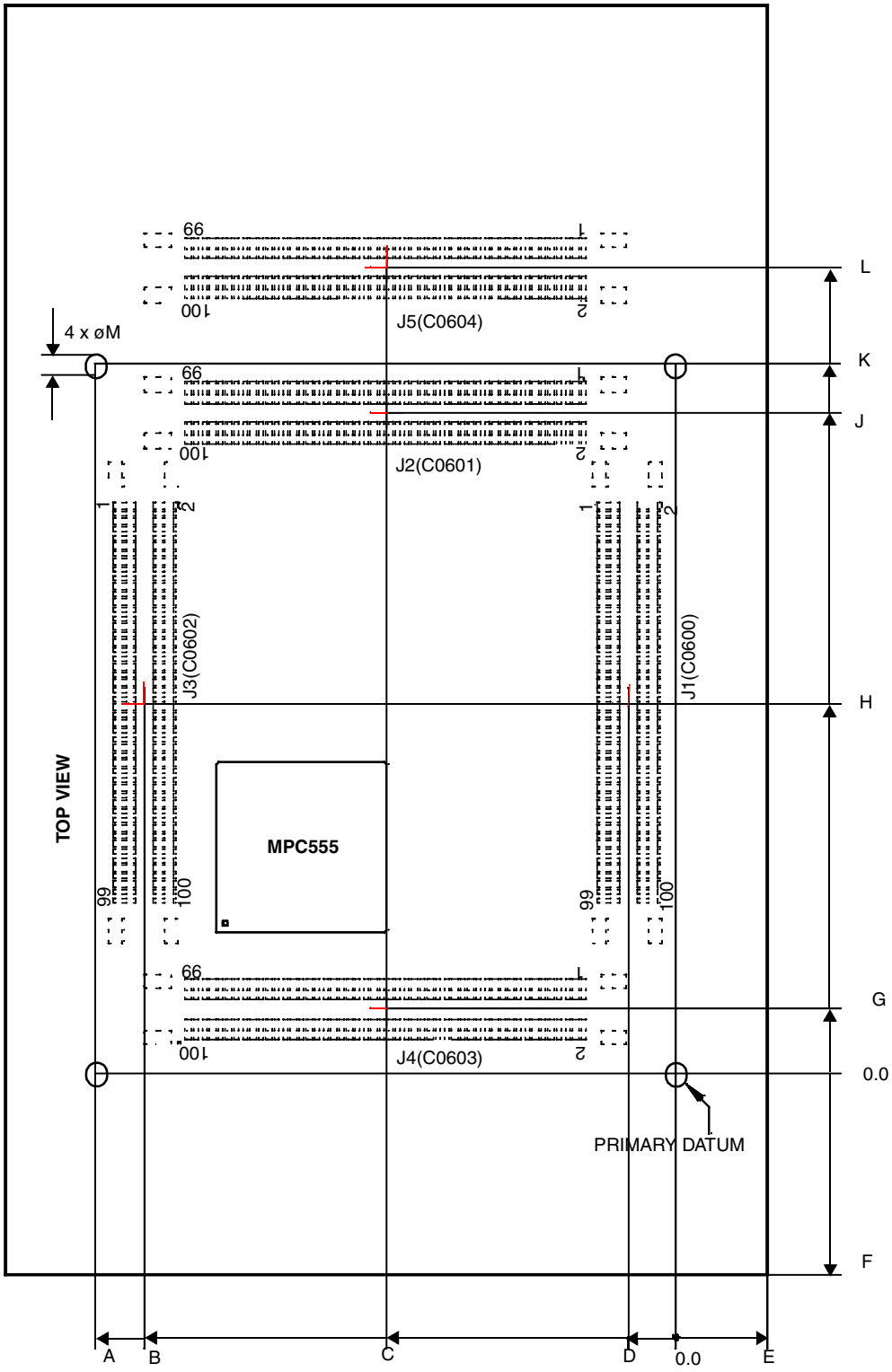

Figure 3 MAPI-400+100 Footprint

Table 5 MAPI-400+100 Dimensions

Dimension	Millimeters	Inches
A	91.45	3.60
B	83.82	3.300
C	45.72	1.800
D	7.62	0.300
E	14.22	0.560
F	31.78	1.250
G	10.16	0.400
H	58.42	2.300
J	104.14	4.100
K	111.76	4.400
L	127.00	5.000
M	3.20	0.126

Table 6 MAPI-400 Signal Definitions

J1 (CO600) PIN NAME				J1 (CO600) PIN NAME	J2 (CO601) PIN NAME			J2 (CO601) PIN NAME
AAN[51]/PQB[7]	1	•	• 2			1	• • 2	AAN50_PQB6
AAN[52]/PQA[0]	3	•	• 4			3	• • 4	AAN49_PQB5
AAN[53]/PQA[1]	5	•	• 6			5	• • 6	AAN48_PQB4
AAN[54]/PQA[2]	7	•	• 8			7	• • 8	AAN3_PQB3
AAN[55]/PQA[3]	9	•	• 10			9	• • 10	AAN2_PQB2
AAN[56]/PQA[4]	11	•	• 12			11	• • 12	AAN1_PQB1
AAN[57]/PQA[5]	13	•	• 14			13	• • 14	AAN0_PQB0
AAN[58]/PQA[6]	15	•	• 16			15	• • 16	
AAN[59]/PQA[7]	17	•	• 18		Ground	17	• • 18	Ground
	19	•	• 20			19	• • 20	
	21	•	• 22		MDA11	21	• • 22	MDA12
	23	•	• 24		MDA13	23	• • 24	MDA14
	25	•	• 26		MDA15	25	• • 26	MDA27
A_TPUCH[0]	27	•	• 28	Ground	MDA28	27	• • 28	MDA29
A_TPUCH[1]	29	•	• 30	MPWM[0]		29	• • 30	HRESETB
A_TPUCH[2]	31	•	• 32	MPWM[1]	ETRIG1	31	• • 32	EXTCLK
A_TPUCH[3]	33	•	• 34		ETRIG2	33	• • 34	BBB_IWP3
A_TPUCH[4]	35	•	• 36	MPWM[2]	BDIP	35	• • 36	BGB_LWP1
A_TPUCH[5]	37	•	• 38	MPWM[3]	BIB_STSB	37	• • 38	BRB_IWP2
A_TPUCH[6]	39	•	• 40		BURSTB	39	• • 40	SGP_IRQOUTB
Ground	41	•	• 42	MPWM[16]	TSB	41	• • 42	EPEE
A_TPUCH[7]	43	•	• 44	MPWM[17]	Ground	43	• • 44	
A_TPUCH[8]	45	•	• 46	Ground		45	• • 46	Ground
A_TPUCH[9]	47	•	• 48	MPWM[18]	ECK	47	• • 48	ENGCLK/BUCLK
A_TPUCH[10]	49	•	• 50	MPWM[19]	RXD1_QGPI	49	• • 50	TXD1_QGPO
A_TPUCH[11]	51	•	• 52		RXD2_QGPI	51	• • 52	TXD2_QGPO
A_TPUCH[12]	53	•	• 54	A_TPUCH[15]		53	• • 54	
A_TPUCH[13]	55	•	• 56	A_T2CLK		55	• • 56	
A_TPUCH[14]	57	•	• 58			57	• • 58	
	59	•	• 60			59	• • 60	
$\overline{\text{IRQ}}$[1]/SGP	61	•	• 62	$\overline{\text{IRQ}}$[0]/SGP	MDA30	61	• • 62	
$\overline{\text{IRQ}}$[3]/SGP	63	•	• 64	$\overline{\text{IRQ}}$[2]/SGP	Ground	63	• • 64	Ground
$\overline{\text{IRQ}}$[5]/SGP	65	•	• 66	$\overline{\text{IRQ}}$[4]/SGP	MDA31	65	• • 66	MPIO5
$\overline{\text{IRQ}}$[7]/mck3	67	•	• 68	$\overline{\text{IRQ}}$[6]/mck2	MPIO6	67	• • 68	MPIO7
	69	•	• 70		MPIO8	69	• • 70	MPIO9
Ground	71	•	• 72		MPIO10	71	• • 72	MPIO11
	73	•	• 74	Ground	MPIO12	73	• • 74	MPIO13
	75	•	• 76		MPIO14	75	• • 76	MPIO15
	77	•	• 78			77	• • 78	
	79	•	• 80			79	• • 80	
	81	•	• 82			81	• • 82	
	83	•	• 84		Ground	83	• • 84	Ground
	85	•	• 86			85	• • 86	
	87	•	• 88			87	• • 88	BAN0_PQB0
Ground	89	•	• 90			89	• • 90	BAN1_PQB1
	91	•	• 92	Ground		91	• • 92	BAN2_PQB2
	93	•	• 94			93	• • 94	BAN3_PQB3
	95	•	• 96			95	• • 96	BAN48_PQB4
	97	•	• 98			97	• • 98	BAN49_PQB5
	99	•	• 100	VPP		99	• • 100	BAN50_PQB6

Table 7 MAPI-400 Signal Definitions

J3 (CO602) PIN NAME				J3 (CO602) PIN NAME	J4 (CO603) PIN NAME			J4 (CO603) PIN NAME
	1	2		BAN51_PQB7		1	2	
	3	4		BAN52_PQA0	Data_SGP1	3	4	Data_SGP0
	5	6		BAN53_PQA1	Data_SGP3	5	6	Data_SGP2
	7	8		BAN54_PQA2	Data_SGP5	7	8	Data_SGP4
	9	10		BAN55_PQA3	Data_SGP7	9	10	Data_SGP6
	11	12		BAN56_PQA4	Data_SGP9	11	12	Data_SGP8
	13	14		BAN57_PQA5	Data_SGP11	13	14	Data_SGP10
	15	16		BAN58_PQA6	Ground	15	16	Ground
	17	18		BAN59_PQA7	Data_SGP13	17	18	Data_SGP12
	19	20			Data_SGP15	19	20	Data_SGP14
	21	22			Data_SGP17	21	22	Data_SGP16
	23	24			Data_SGP19	23	24	Data_SGP18
Ground	25	26		B_TPUCH0	Data_SGP21	25	26	Data_SGP20
A_CNRX0	27	28		B_TPUCH1	Ground	27	28	Ground
A_CNTX0	29	30		B_TPUCH2	Data_SGP23	29	30	Data_SGP22
	31	32		B_TPUCH3	Data_SGP25	31	32	Data_SGP24
B_CNRX0	33	34		B_TPUCH4	Data_SGP27	33	34	Data_SGP26
B_CNTX0	35	36		B_TPUCH5	Data_SGP29	35	36	Data_SGP28
	37	38		B_TPUCH6	Data_SGP31	37	38	Data_SGP30
SCK_QGP6	39	40		B_TPUCH7	Ground	39	40	Ground
MISO_QGP4	41	42		B_TPUCH8		41	42	
Ground	43	44		B_TPUCH9		43	44	
MOSI_QGP5	45	46		B_TPUCH10		45	46	
PCS0_QGP	47	48		B_TPUCH11		47	48	
	49	50		B_TPUCH12	ADDR_SGP9	49	50	ADDR_SGP8
PCS1QGP	51	52		B_TPUCH13	ADDR_SGP11	51	52	ADDR_SGP10
PCS2QGP	53	54		B_TPUCH14	ADDR_SGP13	53	54	ADDR_SGP12
	55	56		B_TPUCH15	ADDR_SGP15	55	56	ADDR_SGP14
PCS3QGP	57	58		B_T2CLK	Ground	57	58	Ground
	59	60			ADDR_SGP17	59	60	ADDR_SGP16
	61	62		VF0_MPIO0	ADDR_SGP19	61	62	ADDR_SGP18
	63	64		VF1_MPIO1	ADDR_SGP21	63	64	ADDR_SGP20
Ground	65	66		VF2_MPIO2	ADDR_SGP23	65	66	ADDR_SGP22
VFLS0_MPIO3	67	68		Ground	ADDR_SGP25	67	68	ADDR_SGP24
VFLS1_MPIO4	69	70			ADDR_SGP27	69	70	ADDR_SGP26
IWP0_VFLS	71	72			ADDR_SGP29	71	72	ADDR_SGP28
IWP1_VFLS	73	74			ADDR_SGP31	73	74	ADDR_SGP30
	75	76			Ground	75	76	Ground
PORESETB	77	78			TAB	77	78	TEAB
	79	80		TDO_DSDO		79	80	WEB_AT[0]
Ground	81	82		TDI_DSDI	RD_WRB	81	82	WEB_AT[1]
TMS	83	84			Ground	83	84	WEB_AT[2]
TCK_DSCK	85	86		TSIZ0	CS0B	85	86	WEB_AT[3]
TRST_B	87	88		TSIZ1	CS1B	87	88	OEB
SRESET	89	90		RSTCONF/TEXP	CS2B	89	90	
Ground	91	92			CS3B	91	92	
	93	94		FRZ_PTR	Ground	93	94	
Ground	95	96			CLKOUT	95	96	Ground
Ground	97	98			Ground	97	98	
	99	100				99	100	

Table 8 MAPI-400 +100 PRU Extended Signal Definitions

PIN NAME		J5 (CO605)			PIN NAME
B_PIO0	1	•	•	2	A_PIO0
B_PIO1	3	•	•	4	A_PIO1
B_PIO2	5	•	•	6	A_PIO2
B_PIO3	7	•	•	8	A_PIO3
B_PIO4	9	•	•	10	A_PIO4
B_PIO5	11	•	•	12	A_PIO5
B_PIO6	13	•	•	14	A_PIO6
Ground	15	•	•	16	Ground
B_PIO7	17	•	•	18	A_PIO7
B_PIO8	19	•	•	20	A_PIO8
B_PIO9	21	•	•	22	A_PIO9
B_PIO10	23	•	•	24	A_PIO10
B_PIO11	25	•	•	26	A_PIO11
Ground	27	•	•	28	Ground
B_PIO12	29	•	•	30	A_PIO12
B_PIO13	31	•	•	32	A_PIO13
B_PIO14	33	•	•	34	A_PIO14
B_PIO15	35	•	•	36	A_PIO15
B_PIO16	37	•	•	38	A_PIO16
Ground	39	•	•	40	Ground
B_PIO17	41	•	•	42	A_PIO17
B_PIO18	43	•	•	44	A_PIO18
B_PIO19	45	•	•	46	A_PIO19
B_PIO20	47	•	•	48	A_PIO20
B_PIO21	49	•	•	50	A_PIO21
B_PIO22	51	•	•	52	A_PIO22
B_PIO23	53	•	•	54	A_PIO23
B_PIO24	55	•	•	56	A_PIO24
Ground	57	•	•	58	Ground
B_PIO25	59	•	•	60	A_PIO25
B_PIO26	61	•	•	62	A_PIO26
B_PIO27	63	•	•	64	A_PIO27
B_PIO28	65	•	•	66	A_PIO28
B_PIO29	67	•	•	68	A_PIO29
B_PIO30	69	•	•	70	A_PIO30
B_PIO31	71	•	•	72	A_PIO31
	73	•	•	74	
Ground	75	•	•	76	Ground
	77	•	•	78	
	79	•	•	80	
	81	•	•	82	
Ground	83	•	•	84	
/EXTBUS	85	•	•	86	STANDBY
	87	•	•	88	
Ground	89	•	•	90	Ground
Ground	91	•	•	92	Ground
Ground	93	•	•	94	Ground
UB2	95	•	•	96	UB2
UB2	97	•	•	98	UB2
UB2	99	•	•	100	UB2

5 Lauterbach Trace Connector

The MPC555EVB includes a 64-pin connector to allow trace tools, such as Lauterbach's Trace-32, a simple connection to the signals required for trace.

Table 9 Lauterbach Universal MPC500/800 Family Trace Adapter Connector

PIN NAME		CO500			PIN NAME
ADDR20	1	•	•	2	ADDR21
ADDR11	3	•	•	4	ADDR22
ADDR19	5	•	•	6	ADDR23
ADDR18	7	•	•	8	ADDR24
ADDR17	9	•	•	10	ADDR12
DATA11	11	•	•	12	ADDR13
RD_$\overline{WR}$	13	•	•	14	ADDR14
DATA8	15	•	•	16	ADDR15
VCC3_3	17	•	•	18	ADDR16
DATA3	19	•	•	20	$\overline{WE}$_AT2
DATA2	21	•	•	22	IRQOUT_LWP0
DATA1	23	•	•	24	$\overline{WE}$_AT3
DATA0	25	•	•	26	$\overline{BR}$_VF1_IWP2
VCC5	27	•	•	28	DATA10
$\overline{WE}$_AT0	29	•	•	30	DATA9
GND	31	•	•	32	IWP0_VFLS0
CLKOUT	33	•	•	34	IWP1_VFLS1
$\overline{WE}$_AT1	35	•	•	36	$\overline{BG}$_VF0_LWP1
DATA7	37	•	•	38	$\overline{BB}$_VF2_LWP3
DATA6	39	•	•	40	ADDR10
DATA5	41	•	•	42	ADDR9
GND	43	•	•	44	ADDR8
DATA4	45	•	•	46	$\overline{BI}$_$\overline{STS}$
ADDR26	47	•	•	48	TS
ADDR29	49	•	•	50	$\overline{FRZ}$_PTR
ADDR30	51	•	•	52	VFLS0_MPIO3
ADDR27	53	•	•	54	VFLS1_MPIO4
ADDR31	55	•	•	56	VF1_MPIO1
ADDR28	57	•	•	58	VF0_MPIO0
ADDR25	59	•	•	60	VF2_MPIO2
$\overline{RSTCONF}$	61	•	•	62	$\overline{IRQ3}$_KR
$\overline{HRESET}$	63	•	•	64	$\overline{IRQ4}$_AT2

6 Mounting Holes

Figure 4 shows the mounting holes available to mount the EVB555 to other boards. Table 10 shows the dimensions of the connectors on the top side of the board.

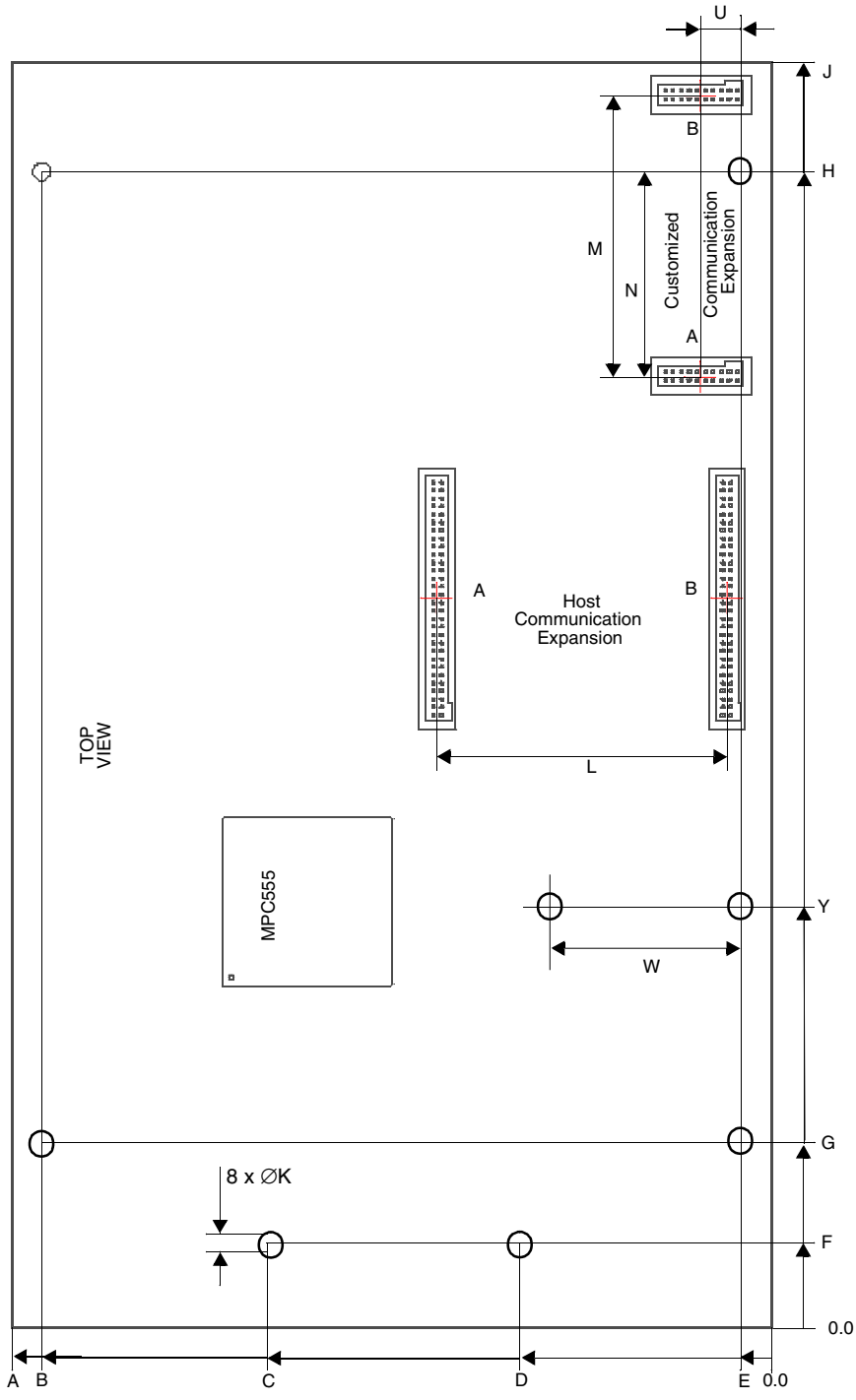

Figure 4 Mounting Holes and Top-Side Connector Dimensions

Table 10 Top Dimensions

Dimension	Millimeters	Inches
A	120.00	4.724
B	115.19	4.535
C	79.63	3.135
D	39.63	1.560
E	4.70	0.185
F	13.34	0.525
G	29.22	1.150
H	182.89	7.200
J	200.00	7.874
K	2.80	0.110
L	45.72	1.800
M	44.45	1.750
N	32.385	1.275
U	6.35	0.250
W	32.39	1.275
Y	66.675	2.625

7 Keep-Out Areas

All of the connectors on the top side of the EVB555 have keep-out areas associated with them to accommodate any board that could be connected to the expansion connectors. **Figure 5** shows the various keep-out areas.

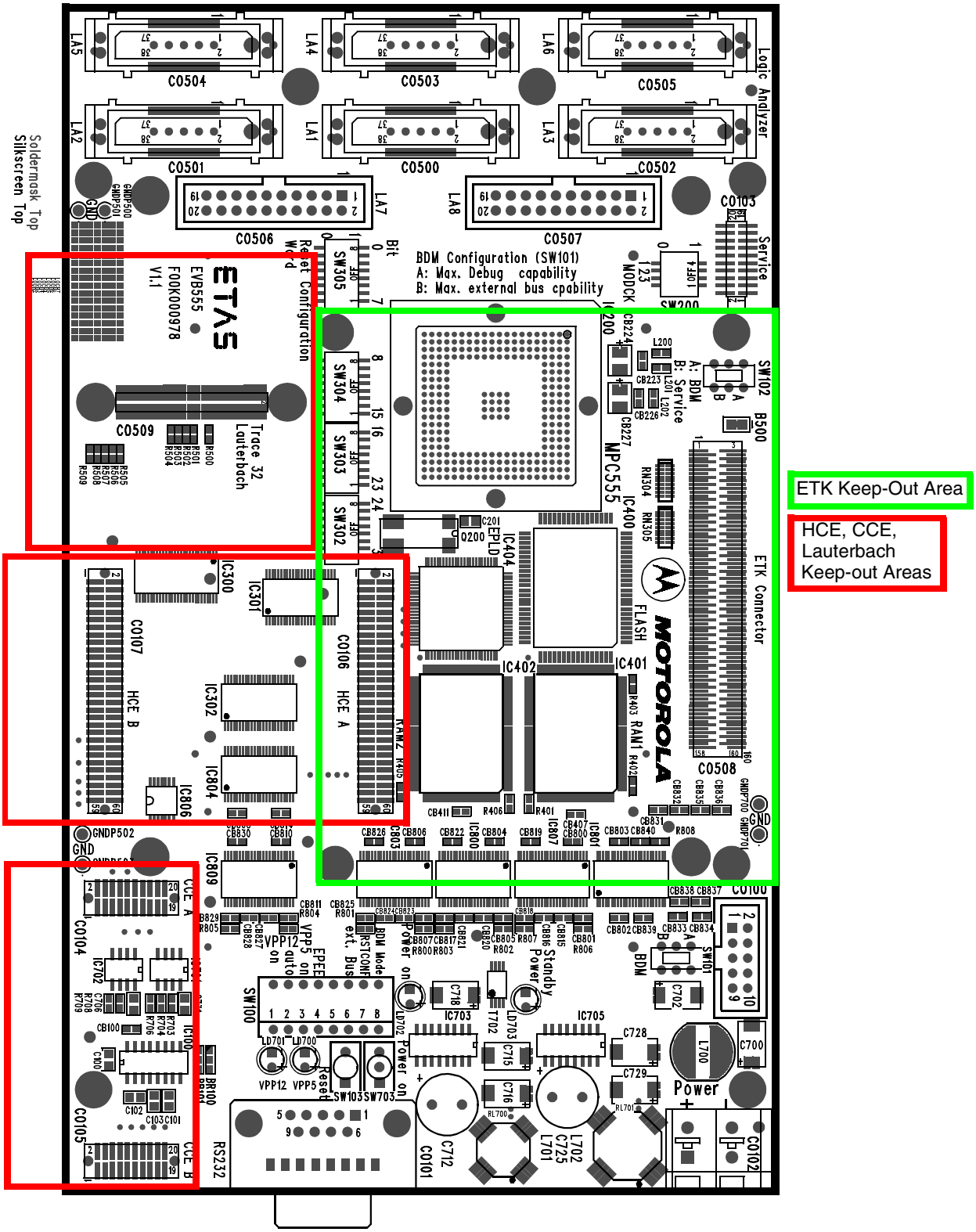

Figure 5 Expansion Board Keep-Out Areas

8 Summary of Connectors

Table 11 shows the number and types of each kind of user extension connectors on the EVB555. Shown are the part numbers for the connectors on the EVB555 and the part numbers for connectors that are required for a user board.

Table 11 Summary Of Connectors

Connector	Number of Connectors on Board	EVB555 Connector Part Number	User Board Connector Part Number (Surface Mount)	User Board Connector Part Number (Through Hole)
CO100 Background Debug Mode Interface	1 each	3M 925320-01-10-10	3M 8510-4500 JL (board mount)	3M CHG-2010-J01010-KCP (wire mount)
CO104/CO105 Customized Communication Expansion	2 each	Samtec TFM-110-12-S-D-P	Samtec SFM-110-02-S-D-P	
CO106/CO107 Host Communication Expansion	2 each	Samtec TFM-130-12-S-D-P	Samtec SFM-130-02-S-D-P	
CO500-505 Mictor Digital Logic Analyzer	6 each	AMP 767 004 product code 2429		
CO506/CO507 Analog Logic Analyzer	2 each	3M 925320-01-20-10	3M 8520-4500 (board mount)	3M CHG-2020-J01010-KCP (wire mount)
CO509 Lauterbach Interface	1 each	Samtec FTE-132-02-G-DV-P	Samtec CLE-132-01-G-DV-P	
CO600-604 MAPI-400+100	5 each	Robinson Nugent P50L-100 S-BS-TGF	Robinson Nugent P50L-100 P-AS-TGF	

9 Reference

For more information see the following reference material.

9.1 MPC555 User's Manual

The ***MPC555 User's Manual* (MPC555UM/AD)** is available from Motorola and describes the MPC555 device. The URL for the Motorola website is http://www.mcu.motsps.com/lit/mpc.html.

9.2 EVB555

MPC555 Evaluation Board Quick Reference, ETAS

9.3 SAMTEC Connectors

Samtec has board layout recommendations and specifications for all of their connectors available on-line. The URL for this website is http://www.samtec.com.

9.4 Robinson Nugent Connector

Further information on the Robinson Nugent connectors is available on-line. The URL for this website is http://www.robinsonnugent.com. At that site, search for P50L connectors.

9.5 Lauterbach

More information on the Lauterbach real-time trace module is available on-line. The URL for this web-site is http://www.lauterbach.de.

10 Revision History

Table 12 Revision History

Release Number	Date	Author	Sections Affected	Summary of Changes
1	31 July 01	Randy Dees	Table 5	Added dimension A to Table 5. Re-named dimension I in Table 5 to agree with Figure 3.

To obtain additional product information:

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