



100-MHz Pentium® II Clock Synthesizer/Driver with Spread Spectrum for Mobile PCs

Features

- Mixed 2.5V and 3.3V operation
- Complete clock solution for Pentium® II, and other similar processor-based motherboards
 - Two CPU clocks at 2.5V up to 100 MHz
 - Six synchronous PCI clocks, one free-running
 - Two 3.3V Reference clocks at 14.318 MHz
 - One 3.3V USB clock running at 48 MHz
 - One 3.3V USB/IO clock running at 48 MHz/24 MHz
- Spread Spectrum clocking for EMI control
- 1.5–4.0 ns delay between CPU and PCI clocks
- Power-down, CPU stop and PCI stop pins
- Low skew outputs, ≤ 175 ps between CPU clocks
- Early PCI clock leads PCI by 1–4 ns (-2 option)
- DIV4 allows dynamic shifting of CPU and PCI clocks from the default frequency to default/4 (-2 option)
- Factory-EPROM programmable output drive and slew rate for EMI customization
- Available in space-saving 28-pin SSOP package

Functional Description

The CY2285 is a clock synthesizer/driver for Pentium II, or other similar processor-based mobile PCs requiring up to 100-MHz support. The CY2285 outputs two CPU clocks at 2.5V. There are six PCI clocks, running at one-half or one-third the CPU clock frequency of 66.6 MHz and 100 MHz respectively. One of the PCI clocks is free-running. Additionally, the part outputs two 3.3V reference clocks at 14.318 MHz.

The CY2285 incorporates the Intel®-defined spread spectrum features. It provides a –0.6% downspread on the CPU and PCI clocks, which can help reduce EMI in certain high-speed systems.

The CY2285 possesses power-down, CPU stop, and PCI stop pins for power management control. The signals are synchronized on-chip, and ensure glitch-free transitions on the outputs. When the CPU_STOP input is asserted, the CPU clock outputs are driven LOW. When the PCI_STOP input is asserted, the PCI clock outputs (except the free-running PCI clock) are driven LOW. When the PWR_DWN pin is asserted, the reference oscillator and PLLs are shut down, and all outputs are driven LOW.

The CY2285-2 features an early PCI clock which leads the other PCI clocks by 1–4 ns. The CY2285-2 also features a DIV4 pin which allows for dynamic shifting of CPU and PCI clocks from the default frequency to the default/4.

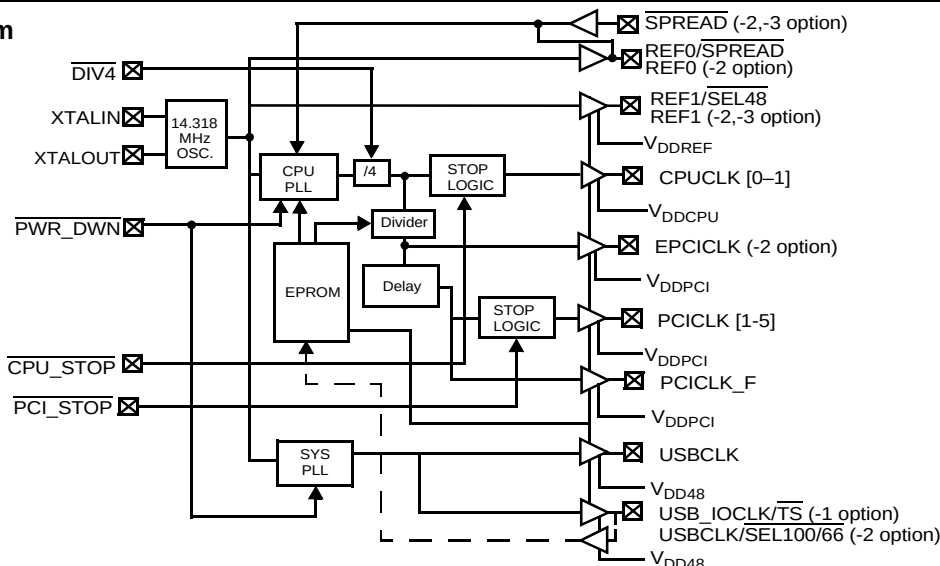
CY2285 Selector Guide

Clock Outputs	CY2285-1	CY2285-2	CY2285-3
CPU (66, 100 MHz)	2	2	2
PCI (CPU/2, CPU/3 MHz)	6 ^[1]	7 ^[1, 2]	6 ^[1]
Ref. (14.318 MHz)	2	2	1
USB (48 MHz)	1	1	1
USB/IO (48 MHz/24 MHz selectable)	1	N/A	1
CPU-PCI delay	1.5–4.0 ns	1.5–4.0 ns	1.5–4.0 ns
EPCI-PCI delay	N/A	1.0–4.0 ns	N/A
Spread Spectrum	–0.6% Downspread	–0.6% Downspread	–0.6% Downspread

Notes:

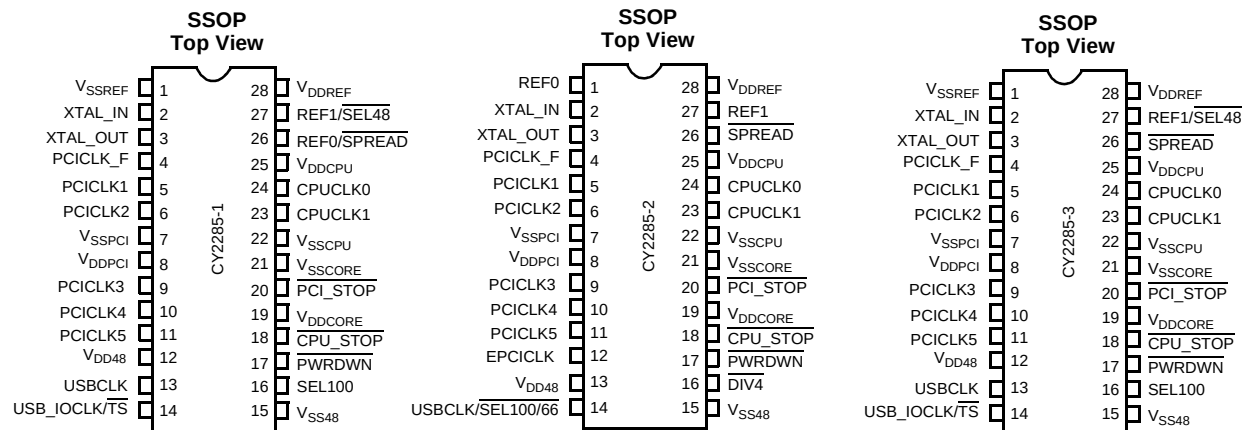
1. One free-running PCI clock.
2. One early PCI clock.

Logic Block Diagram



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Pin Configurations



Pin Summary: CY2285-1, CY2285-3

Name	Pins	Description
V _{DD}	8, 12, 19, 28	3.3V Power supply voltage
V _{DDCPU}	25	2.5V Power supply for CPU clocks
V _{SS}	1, 7, 15, 21, 22	Ground
XTALIN ^[3]	2	Reference crystal input
XTALOUT ^[3]	3	Reference crystal feedback
PCI_STOP	20	Active LOW control input to stop PCI clocks
CPU_STOP	18	Active LOW control input to stop CPU clocks
PWR_DWN	17	Active LOW control input to power down device
SEL100	16	Select for enabling 100-MHz or 66-MHz CPU clock HIGH = 100 MHz, LOW = 66 MHz
CPUCLK[0:1]	23, 24	2.5V CPU clock outputs
PCICLK[1:5]	5, 6, 9, 10, 11	3.3V PCI clock outputs
PCICLK_F	4	3.3V Free-running PCI clock output
REF0/SPREAD	26 (-1 option)	3.3V 14.318-MHz reference clock output and power-on spread spectrum enable strap option. Strap LOW = Spread Spectrum enable Strap HIGH = Spread Spectrum disable
SPREAD	26 (-3 option)	Active LOW control input to enable spread spectrum
REF1/SEL48	27	3.3V 14.318-MHz reference clock output and power-on 48-/24-MHz select strap option. Strap LOW = 48 MHz on pin14 Strap HIGH = 24 MHz on pin14
USBCLK	13	3.3V 48-MHz USB clock output
USB_I/OCLK/TS	14	3.3V 48-MHz or 24-MHz output and three-state strapping option. Strap LOW = Enter three-state mode for testing Strap HIGH = Normal Operation

Note:

3. For best accuracy, use a parallel-resonant crystal, C_{LOAD} = 18 pF.

Pin Summary: CY2285-2

Name	Pins	Description
V _{DD}	8, 13, 19, 28	3.3V Power supply
V _{DDCPU}	25	2.5V Power supply
V _{SS}	7, 15, 21, 22	Ground
XTALIN ^[3]	2	Reference crystal input
XTALOUT ^[3]	3	Reference crystal feedback
PCI_STOP	20	Active LOW control input to stop PCI clocks
CPU_STOP	18	Active LOW control input to stop CPU clocks
PWR_DWN	17	Active LOW control input to power down device
DIV4	16	Active LOW control input to enable divide-by-four option on CPU and PCI clocks
CPUCLK[0:1]	23, 24	2.5V CPU clock outputs
PCICLK[1:5]	5, 6, 9, 10, 11	3.3V PCI clock outputs
PCICLK_F	4	3.3V Free-running PCI clock output
EPCICLK	12	3.3V Early PCI clock output (Not Free-running)
REF0	1	3.3V 14.318-MHz reference clock output
REF1	27	3.3V 14.318-MHz reference clock output
USBCLK/SEL100/66	14	3.3V 48-MHz USB clock output or select input and frequency select strap option (use 10-k Ω external strap resistor) Strap LOW = 66.6-MHz CPU Frequency Strap HIGH = 100-MHz CPU Frequency
SPREAD	26	Active LOW control input to enable Spread Spectrum

Actual Clock Frequency Values

Clock Output	Target Frequency (MHz)	Actual Frequency (MHz)	PPM
CPUCLK	66.67	66.654	-240
CPUCLK	100	99.77	-2300
USB 48-MHz	48	48.008	+167

Power Management Logic

CPU_STOP	PCI_STOP	PWR_DWN	CPUCLK	PCICLK	PCICLK_F	Other Clocks	Osc.	PLLs
X	X	0	Low	Low	Low	Low	Off	Off
0	0	1	Low	Low	Running	Running	Running	Running
0	1	1	Low	Running	Running	Running	Running	Running
1	0	1	Running	Low	Running	Running	Running	Running
1	1	1	Running	Running	Running	Running	Running	Running

Function Table: CY2285-1

SEL100	$\overline{\text{SEL48}}^{[4]}$	$\overline{\text{TS}}^{[4]}$	$\overline{\text{SPREAD}}^{[4]}$	CPUCLK[0:1]	PCICLK[1:5], PCICLK_F	USB_IOCLK	USBCLK	REFCLK [0-1]
X	X	0	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0	1	1	1 (no spread)	66.6 MHz	33.3 MHz	24 MHz	48 MHz	14.318 MHz
0	0	1	0 (–0.6% downspread)	66.6 MHz	33.3 MHz	48 MHz	48 MHz	14.318 MHz
1	1	1	1 (no spread)	100 MHz	33.3 MHz	24 MHz	48 MHz	14.318 MHz
1	0	1	0 (–0.6% downspread)	100 MHz	33.3 MHz	48 MHz	48 MHz	14.318 MHz

Function Table: CY2285-2

$\overline{\text{SEL100/66}}^{[4]}$	$\overline{\text{SPREAD}}$	DIV4	CPUCLK [0:1]	PCICLK[1:5], PCICLK_F, EPCICLK	USBCLK	REFCLK[0:1]
0	0 (–0.6% downspread)	1	66.67 MHz	33.3 MHz	48 MHz	14.318 MHz
0	1 (no spread)	1	66.67 MHz	33.3 MHz	48 MHz	14.318 MHz
1	0 (–0.6% downspread)	1	100 MHz	33.3 MHz	48 MHz	14.318 MHz
1	1 (no spread)	1	100 MHz	33.3 MHz	48 MHz	14.318 MHz
0	0 (–0.6% downspread)	0	16.67 MHz	8.33 MHz	48 MHz	14.318 MHz
0	1 (no spread)	0	16.67 MHz	8.33 MHz	48 MHz	14.318 MHz
1	0 (–0.6% downspread)	0	25.0 MHz	8.33 MHz	48 MHz	14.318 MHz
1	1 (no spread)	0	25.0 MHz	8.33 MHz	48 MHz	14.318 MHz

Function Table: CY2285-3

SEL100	$\overline{\text{SEL48}}^{[4]}$	$\overline{\text{TS}}^{[4]}$	$\overline{\text{SPREAD}}^{[4]}$	CPUCLK[0:1]	PCICLK[1:5], PCICLK_F	USB_IOCLK	USBCLK	REFCLK1
X	X	0	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0	1	1	1 (no spread)	66.6 MHz	33.3 MHz	24 MHz	48 MHz	14.318 MHz
0	0	1	0 (–0.6% downspread)	66.6 MHz	33.3 MHz	48 MHz	48 MHz	14.318 MHz
1	1	1	1 (no spread)	100 MHz	33.3 MHz	24 MHz	48 MHz	14.318 MHz
1	0	1	0 (–0.6% downspread)	100 MHz	33.3 MHz	48 MHz	48 MHz	14.318 MHz

Note:

4. Power-on strap option.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage -0.5 to +7.0V

Input Voltage -0.5V to $V_{DD}+0.5$

Storage Temperature (Non-Condensing) ... -65°C to +150°C

Junction Temperature +150°C

Static Discharge Voltage >2000V
(per MIL-STD-883, Method 3015, like V_{DD} pins tied together)

Operating Conditions^[5]

Parameter	Description	Min.	Max.	Unit
V_{DD}	Analog and Digital 3.3V Supply Voltage	3.135	3.465	V
V_{DDCPU}	CPU Supply Voltage	2.375	2.625	V
T_A	Operating Temperature, Ambient	0	70	°C
C_L	Max. Capacitive Load on CPUCLK PCICLK REF		20 30 35	pF
$f_{(REF)}$	Reference Frequency, Oscillator Nominal Value	14.318	14.318	MHz
t_{PU}	Power-up time for all V_{DD} 's to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{IH}	High-level Input Voltage	Except Crystal Inputs ^[6]			2.0		V
V_{IL}	Low-level Input Voltage	Except Crystal Inputs ^[6]				0.8	V
V_{OH}	High-level Output Voltage	$V_{DDCPU} = 2.375V$	$I_{OH} = 12\text{ mA}$	CPUCLK	2.0		V
V_{OL}	Low-level Output Voltage	$V_{DDCPU} = 2.375V$	$I_{OL} = 12\text{ mA}$	CPUCLK		0.4	V
V_{OH}	High-level Output Voltage	$V_{DDPCI}, AV_{DD}, V_{DDREF} = 3.135V$	$I_{OH} = 14.5\text{ mA}$	PCICLK	2.4		V
			$I_{OH} = 16\text{ mA}$	REF			
			$I_{OH} = 36\text{ mA}$	REF ^[7]			
V_{OL}	Low-level Output Voltage	$V_{DDPCI}, AV_{DD}, V_{DDREF} = 3.135V$	$I_{OL} = 9.4\text{ mA}$	PCICLK		0.4V	V
			$I_{OL} = 9\text{ mA}$	REF			
			$I_{OL} = 29\text{ mA}$	REF ^[7]			
I_{IH}	Input High Current	$V_{IH} = V_{DD}$			-10	+10	μA
I_{IL}	Input Low Current	$V_{IL} = 0V$				10	μA
I_{OZ}	Output Leakage Current	Three-state			-10	+10	μA
I_{DD25}	Power Supply Current for 2.5V clocks	$V_{DDCPU} = 2.625V, V_{IN} = 0\text{ or }V_{DD}, \text{ Loaded Outputs, CPU} = 66.6\text{ MHz}$				70	mA
I_{DD25}	Power Supply Current for 2.5V clocks	$V_{DDCPU} = 2.625V, V_{IN} = 0\text{ or }V_{DD}, \text{ Loaded Outputs, CPU} = 100\text{ MHz}$				100	mA
I_{DD33}	Power Supply Current for 3.3V clocks	$V_{DD} = 3.465V, V_{IN} = 0\text{ or }V_{DD}, \text{ Loaded Outputs}$				170	mA
I_{DDS}	Powerdown Current	Current draw in powerdown state				500	μA

Notes:

5. Electrical parameters are guaranteed with these operating conditions.
6. Crystal Inputs have CMOS thresholds, nominally $V_{DD}/2$.
7. CY2285-2 option only.

Switching Characteristics^[8] Over the Operating Range

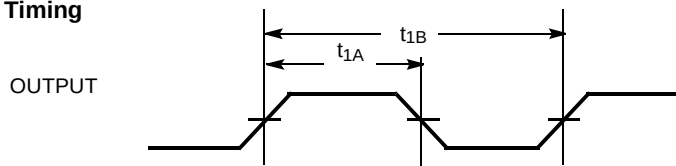
Parameter	Output	Description	Test Conditions	Min.	Typ.	Max.	Unit
t_1	All	Output Duty Cycle ^[9]	$t_1 = t_{1A} \div t_{1B}$	45	50	55	%
t_2	CPUCLK	CPU Clock Rising and Falling Edge Rate	Between 0.4V and 2.0V	1.0		4.0	V/ns
t_2	PCICLK	PCI Clock Rising and Falling Edge Rate	Between 0.4V and 2.4V	1.0		4.0	V/ns
t_2	REF	REF Clock Rising and Falling Edge Rate	Between 0.4V and 2.4V	0.5		2.0	V/ns
t_3	CPUCLK	CPU Clock Rise Time	Between 0.4V and 2.0V	0.4		1.6	ns
t_4	CPUCLK	CPU Clock Fall Time	Between 2.0V and 0.4V	0.4		1.6	ns
t_5	CPUCLK	CPU-CPU Clock Skew	Measured at 1.25V		100	175	ps
t_6	CPUCLK, PCICLK	CPU-PCI Clock Skew	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks	1.5		4.0	ns
t_7	PCICLK, PCICLK	PCI-PCI Clock Skew	Measured at 1.5V			250	ps
t_7	EPCICLK, PCICLK	EPCI-PCI Clock Skew ^[7]	Measured at 1.5V	1.0		4.0	ns
t_{10}	CPUCLK	Cycle-Cycle Clock Jitter	Measured at 1.25V			700	ps
t_{11}	PCICLK	Cycle-Cycle Clock Jitter	Measured at 1.5V			500	ps
t_{12}	CPUCLK, PCICLK	Power-up Time	CPU and PCI clock stabilization from power-up			3	ms
t_{13}	CPUCLK, PCICLK	1/4 Frequency Slew Time ^[7]	Time for CPU, EPCI, and PCI clock frequency to change from f to f/4 after select input change		10	25	cycles

Notes:

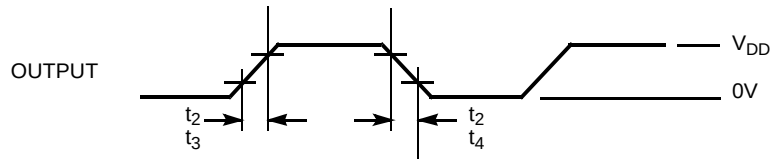
8. All parameters specified with loaded outputs.
9. Duty cycle is measured at 1.5V when $V_{DD} = 3.3V$. When $V_{DD} = 2.5V$, duty cycle is measured at 1.25V.

Switching Waveforms

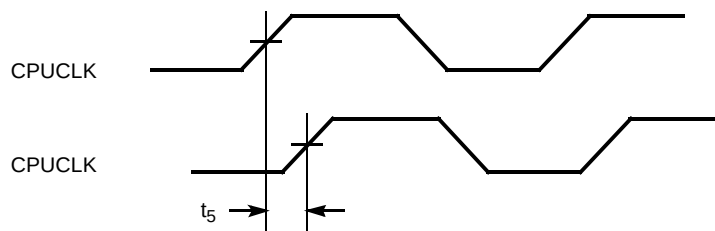
Duty Cycle Timing



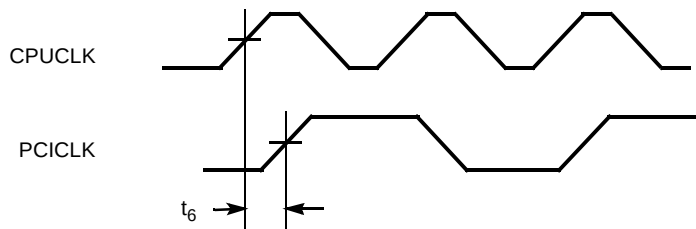
All Outputs Rise/Fall Time



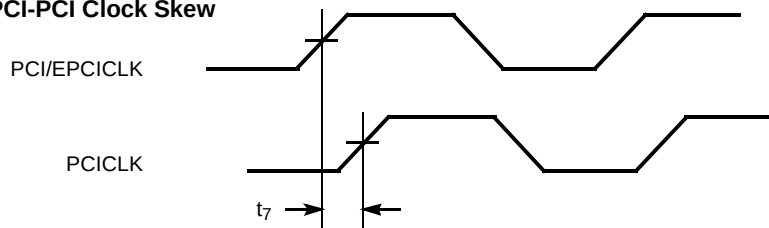
CPU-CPU Clock Skew



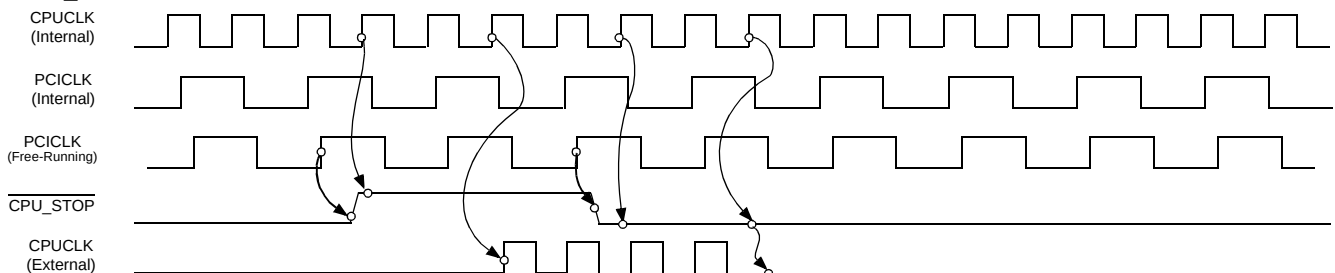
CPU-PCI Clock Skew



PCI/EPCI-PCI Clock Skew

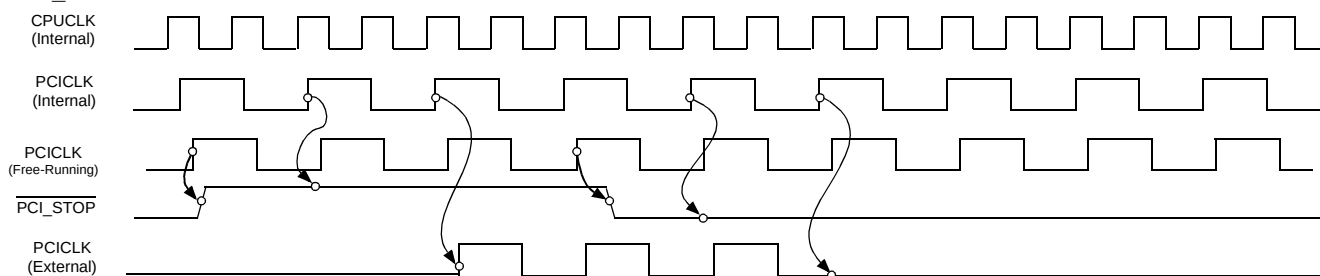


CPU_STOP

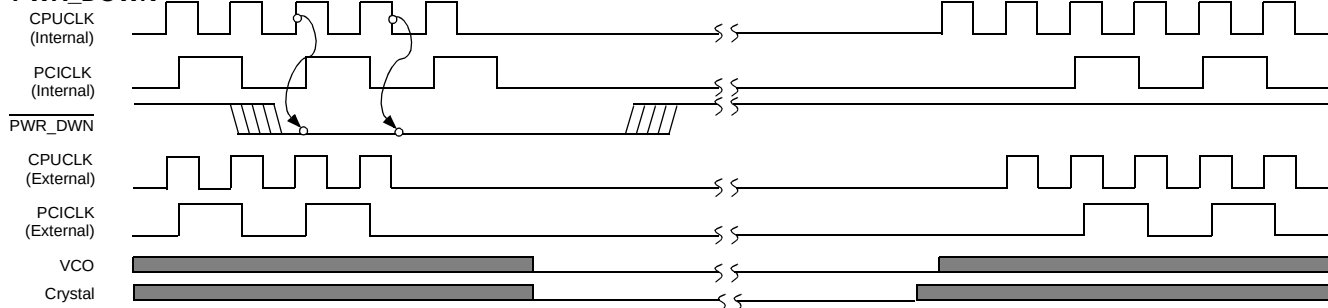


Switching Waveforms (continued)

PCI_STOP



PWR_DOWN



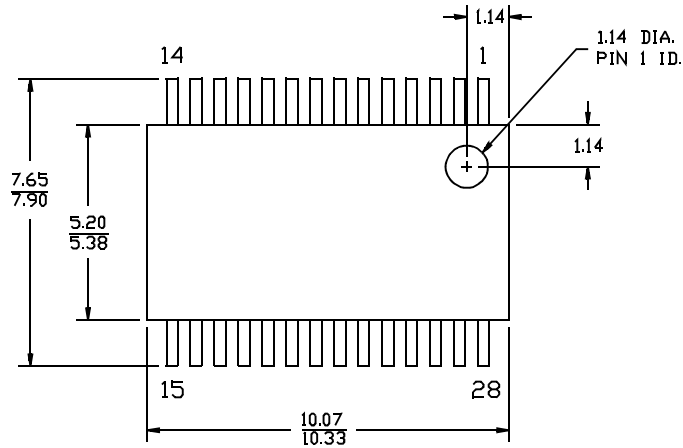
Shaded section on the VCO and Crystal waveforms indicates that the VCO and crystal oscillator are active, and there is a valid clock.

Ordering Information

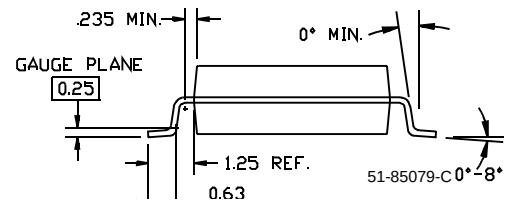
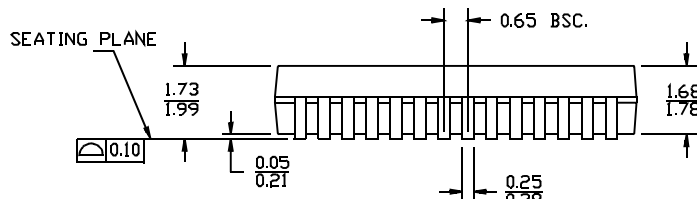
Ordering Code	Package Name	Package Type	Operating Range
CY2285PVC-1	O28	28-Pin SSOP	Commercial
CY2285PVC-2	O28	28-Pin SSOP	Commercial
CY2285PVC-3	O28	28-Pin SSOP	Commercial

Package Diagram

28-Lead (210-Mil) Shrunk Small Outline Package O28



DIMENSIONS IN MILLIMETERS MIN.
MAX.



Revision History

Document Title: CY2285 100-MHz Pentium® II Clock Synthesizer/Driver with Spread Spectrum for Mobile PCs Document Number: 38-07205				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	111725	12/16/01	DSG	Change from Spec number: 38-00732 to 38-07205
*A	121840	12/14/02	RBI	Power up requirements added to Operating Conditions Information



100-MHz Pentium® II Clock Synthesizer/Driver with Spread Spectrum for Mobile PCs

Features

- Mixed 2.5V and 3.3V operation
- Complete clock solution for Pentium® II, and other similar processor-based motherboards
 - Two CPU clocks at 2.5V up to 100 MHz
 - Six synchronous PCI clocks, one free-running
 - Two 3.3V Reference clocks at 14.318 MHz
 - One 3.3V USB clock running at 48 MHz
 - One 3.3V USB/IO clock running at 48 MHz/24 MHz
- Spread Spectrum clocking for EMI control
- 1.5–4.0 ns delay between CPU and PCI clocks
- Power-down, CPU stop and PCI stop pins
- Low skew outputs, ≤ 175 ps between CPU clocks
- Early PCI clock leads PCI by 1–4 ns (-2 option)
- DIV4 allows dynamic shifting of CPU and PCI clocks from the default frequency to default/4 (-2 option)
- Factory-EPROM programmable output drive and slew rate for EMI customization
- Available in space-saving 28-pin SSOP package

Functional Description

The CY2285 is a clock synthesizer/driver for Pentium II, or other similar processor-based mobile PCs requiring up to 100-MHz support. The CY2285 outputs two CPU clocks at 2.5V. There are six PCI clocks, running at one-half or one-third the CPU clock frequency of 66.6 MHz and 100 MHz respectively. One of the PCI clocks is free-running. Additionally, the part outputs two 3.3V reference clocks at 14.318 MHz.

The CY2285 incorporates the Intel®-defined spread spectrum features. It provides a –0.6% downspread on the CPU and PCI clocks, which can help reduce EMI in certain high-speed systems.

The CY2285 possesses power-down, CPU stop, and PCI stop pins for power management control. The signals are synchronized on-chip, and ensure glitch-free transitions on the outputs. When the CPU_STOP input is asserted, the CPU clock outputs are driven LOW. When the PCI_STOP input is asserted, the PCI clock outputs (except the free-running PCI clock) are driven LOW. When the PWR_DWN pin is asserted, the reference oscillator and PLLs are shut down, and all outputs are driven LOW.

The CY2285-2 features an early PCI clock which leads the other PCI clocks by 1–4 ns. The CY2285-2 also features a DIV4 pin which allows for dynamic shifting of CPU and PCI clocks from the default frequency to the default/4.

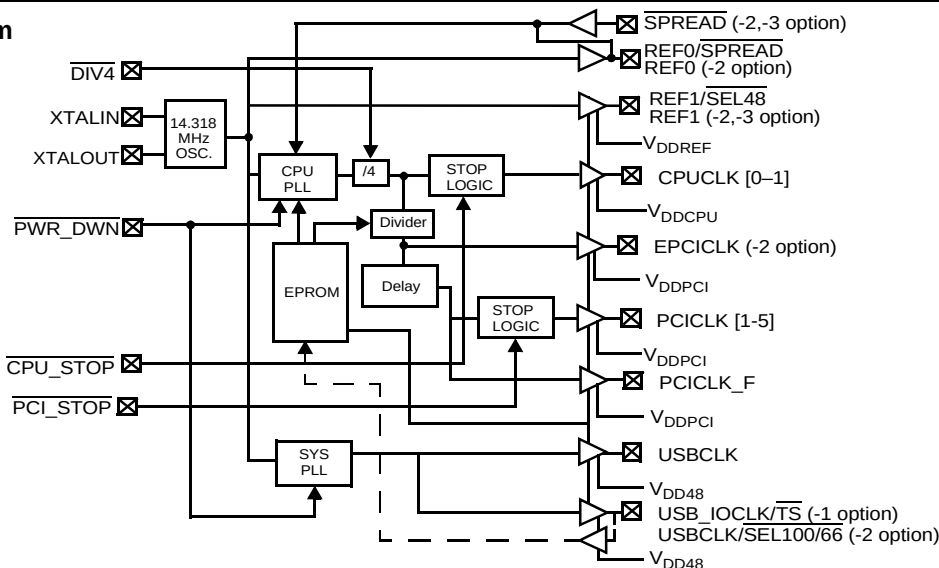
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PCI (CPU/2, CPU/3 MHz)	6 ^[1]	7 ^[1, 2]	6 ^[1]
Ref. (14.318 MHz)	2	2	1
USB (48 MHz)	1	1	1
USB/IO (48 MHz/24 MHz selectable)	1	N/A	1
CPU-PCI delay	1.5–4.0 ns	1.5–4.0 ns	1.5–4.0 ns
EPCI-PCI delay	N/A	1.0–4.0 ns	N/A
Spread Spectrum	–0.6% Downspread	–0.6% Downspread	–0.6% Downspread

Notes:

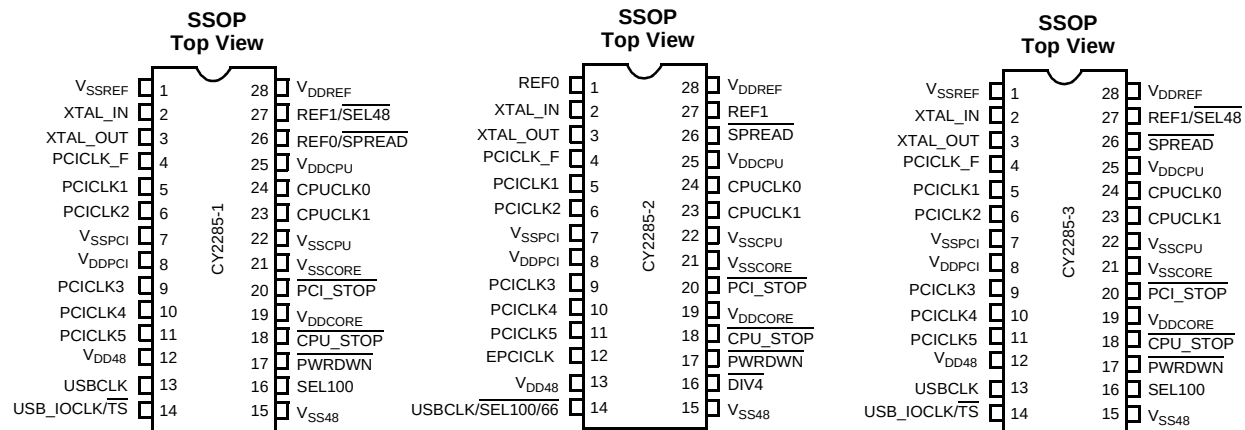
1. One free-running PCI clock.
2. One early PCI clock.

Logic Block Diagram



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Pin Configurations



Pin Summary: CY2285-1, CY2285-3

Name	Pins	Description
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V _{DDCPU}	25	2.5V Power supply for CPU clocks
V _{SS}	1, 7, 15, 21, 22	Ground
XTALIN ^[3]	2	Reference crystal input
XTALOUT ^[3]	3	Reference crystal feedback
PCI_STOP	20	Active LOW control input to stop PCI clocks
CPU_STOP	18	Active LOW control input to stop CPU clocks
PWR_DWN	17	Active LOW control input to power down device
SEL100	16	Select for enabling 100-MHz or 66-MHz CPU clock HIGH = 100 MHz, LOW = 66 MHz
CPUCLK[0:1]	23, 24	2.5V CPU clock outputs
PCICLK[1:5]	5, 6, 9, 10, 11	3.3V PCI clock outputs
PCICLK_F	4	3.3V Free-running PCI clock output
REF0/SPREAD	26 (-1 option)	3.3V 14.318-MHz reference clock output and power-on spread spectrum enable strap option. Strap LOW = Spread Spectrum enable Strap HIGH = Spread Spectrum disable
SPREAD	26 (-3 option)	Active LOW control input to enable spread spectrum
REF1/SEL48	27	3.3V 14.318-MHz reference clock output and power-on 48-/24-MHz select strap option. Strap LOW = 48 MHz on pin14 Strap HIGH = 24 MHz on pin14
USBCLK	13	3.3V 48-MHz USB clock output
USB_I/OCLK/TS	14	3.3V 48-MHz or 24-MHz output and three-state strapping option. Strap LOW = Enter three-state mode for testing Strap HIGH = Normal Operation

Note:

3. For best accuracy, use a parallel-resonant crystal, C_{LOAD} = 18 pF.

Pin Summary: CY2285-2

Name	Pins	Description
V _{DD}	8, 13, 19, 28	3.3V Power supply
V _{DDCPU}	25	2.5V Power supply
V _{SS}	7, 15, 21, 22	Ground
XTALIN ^[3]	2	Reference crystal input
XTALOUT ^[3]	3	Reference crystal feedback
PCI_STOP	20	Active LOW control input to stop PCI clocks
CPU_STOP	18	Active LOW control input to stop CPU clocks
PWR_DWN	17	Active LOW control input to power down device
DIV4	16	Active LOW control input to enable divide-by-four option on CPU and PCI clocks
CPUCLK[0:1]	23, 24	2.5V CPU clock outputs
PCICLK[1:5]	5, 6, 9, 10, 11	3.3V PCI clock outputs
PCICLK_F	4	3.3V Free-running PCI clock output
EPCICLK	12	3.3V Early PCI clock output (Not Free-running)
REF0	1	3.3V 14.318-MHz reference clock output
REF1	27	3.3V 14.318-MHz reference clock output
USBCLK/SEL100/66	14	3.3V 48-MHz USB clock output or select input and frequency select strap option (use 10-kΩ external strap resistor) Strap LOW = 66.6-MHz CPU Frequency Strap HIGH = 100-MHz CPU Frequency
SPREAD	26	Active LOW control input to enable Spread Spectrum

Actual Clock Frequency Values

Clock Output	Target Frequency (MHz)	Actual Frequency (MHz)	PPM
CPUCLK	66.67	66.654	-240
CPUCLK	100	99.77	-2300
USB 48-MHz	48	48.008	+167

Power Management Logic

CPU_STOP	PCI_STOP	PWR_DWN	CPUCLK	PCICLK	PCICLK_F	Other Clocks	Osc.	PLLs
X	X	0	Low	Low	Low	Low	Off	Off
0	0	1	Low	Low	Running	Running	Running	Running
0	1	1	Low	Running	Running	Running	Running	Running
1	0	1	Running	Low	Running	Running	Running	Running
1	1	1	Running	Running	Running	Running	Running	Running

Function Table: CY2285-1

SEL100	$\overline{\text{SEL48}}^{[4]}$	$\overline{\text{TS}}^{[4]}$	$\overline{\text{SPREAD}}^{[4]}$	CPUCLK[0:1]	PCICLK[1:5], PCICLK_F	USB_IOCLK	USBCLK	REFCLK [0-1]
X	X	0	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0	1	1	1 (no spread)	66.6 MHz	33.3 MHz	24 MHz	48 MHz	14.318 MHz
0	0	1	0 (–0.6% downspread)	66.6 MHz	33.3 MHz	48 MHz	48 MHz	14.318 MHz
1	1	1	1 (no spread)	100 MHz	33.3 MHz	24 MHz	48 MHz	14.318 MHz
1	0	1	0 (–0.6% downspread)	100 MHz	33.3 MHz	48 MHz	48 MHz	14.318 MHz

Function Table: CY2285-2

$\overline{\text{SEL100/66}}^{[4]}$	$\overline{\text{SPREAD}}$	DIV4	CPUCLK [0:1]	PCICLK[1:5], PCICLK_F, EPCICLK	USBCLK	REFCLK[0:1]
0	0 (–0.6% downspread)	1	66.67 MHz	33.3 MHz	48 MHz	14.318 MHz
0	1 (no spread)	1	66.67 MHz	33.3 MHz	48 MHz	14.318 MHz
1	0 (–0.6% downspread)	1	100 MHz	33.3 MHz	48 MHz	14.318 MHz
1	1 (no spread)	1	100 MHz	33.3 MHz	48 MHz	14.318 MHz
0	0 (–0.6% downspread)	0	16.67 MHz	8.33 MHz	48 MHz	14.318 MHz
0	1 (no spread)	0	16.67 MHz	8.33 MHz	48 MHz	14.318 MHz
1	0 (–0.6% downspread)	0	25.0 MHz	8.33 MHz	48 MHz	14.318 MHz
1	1 (no spread)	0	25.0 MHz	8.33 MHz	48 MHz	14.318 MHz

Function Table: CY2285-3

SEL100	$\overline{\text{SEL48}}^{[4]}$	$\overline{\text{TS}}^{[4]}$	$\overline{\text{SPREAD}}^{[4]}$	CPUCLK[0:1]	PCICLK[1:5], PCICLK_F	USB_IOCLK	USBCLK	REFCLK1
X	X	0	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0	1	1	1 (no spread)	66.6 MHz	33.3 MHz	24 MHz	48 MHz	14.318 MHz
0	0	1	0 (–0.6% downspread)	66.6 MHz	33.3 MHz	48 MHz	48 MHz	14.318 MHz
1	1	1	1 (no spread)	100 MHz	33.3 MHz	24 MHz	48 MHz	14.318 MHz
1	0	1	0 (–0.6% downspread)	100 MHz	33.3 MHz	48 MHz	48 MHz	14.318 MHz

Note:

4. Power-on strap option.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage -0.5 to +7.0V

Input Voltage -0.5V to $V_{DD}+0.5$

Storage Temperature (Non-Condensing) ... -65°C to +150°C

Junction Temperature +150°C

Static Discharge Voltage >2000V
(per MIL-STD-883, Method 3015, like V_{DD} pins tied together)

Operating Conditions^[5]

Parameter	Description	Min.	Max.	Unit
V_{DD}	Analog and Digital 3.3V Supply Voltage	3.135	3.465	V
V_{DDCPU}	CPU Supply Voltage	2.375	2.625	V
T_A	Operating Temperature, Ambient	0	70	°C
C_L	Max. Capacitive Load on CPUCLK PCICLK REF		20 30 35	pF
$f_{(REF)}$	Reference Frequency, Oscillator Nominal Value	14.318	14.318	MHz
t_{PU}	Power-up time for all V_{DD} 's to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{IH}	High-level Input Voltage	Except Crystal Inputs ^[6]			2.0		V
V_{IL}	Low-level Input Voltage	Except Crystal Inputs ^[6]				0.8	V
V_{OH}	High-level Output Voltage	$V_{DDCPU} = 2.375V$	$I_{OH} = 12\text{ mA}$	CPUCLK	2.0		V
V_{OL}	Low-level Output Voltage	$V_{DDCPU} = 2.375V$	$I_{OL} = 12\text{ mA}$	CPUCLK		0.4	V
V_{OH}	High-level Output Voltage	$V_{DDPCI}, AV_{DD}, V_{DDREF} = 3.135V$	$I_{OH} = 14.5\text{ mA}$	PCICLK	2.4		V
			$I_{OH} = 16\text{ mA}$	REF			
			$I_{OH} = 36\text{ mA}$	REF ^[7]			
V_{OL}	Low-level Output Voltage	$V_{DDPCI}, AV_{DD}, V_{DDREF} = 3.135V$	$I_{OL} = 9.4\text{ mA}$	PCICLK		0.4V	V
			$I_{OL} = 9\text{ mA}$	REF			
			$I_{OL} = 29\text{ mA}$	REF ^[7]			
I_{IH}	Input High Current	$V_{IH} = V_{DD}$			-10	+10	μA
I_{IL}	Input Low Current	$V_{IL} = 0V$				10	μA
I_{OZ}	Output Leakage Current	Three-state			-10	+10	μA
I_{DD25}	Power Supply Current for 2.5V clocks	$V_{DDCPU} = 2.625V, V_{IN} = 0\text{ or }V_{DD}, \text{ Loaded Outputs, CPU} = 66.6\text{ MHz}$				70	mA
I_{DD25}	Power Supply Current for 2.5V clocks	$V_{DDCPU} = 2.625V, V_{IN} = 0\text{ or }V_{DD}, \text{ Loaded Outputs, CPU} = 100\text{ MHz}$				100	mA
I_{DD33}	Power Supply Current for 3.3V clocks	$V_{DD} = 3.465V, V_{IN} = 0\text{ or }V_{DD}, \text{ Loaded Outputs}$				170	mA
I_{DDS}	Powerdown Current	Current draw in powerdown state				500	μA

Notes:

5. Electrical parameters are guaranteed with these operating conditions.
6. Crystal Inputs have CMOS thresholds, nominally $V_{DD}/2$.
7. CY2285-2 option only.

Switching Characteristics^[8] Over the Operating Range

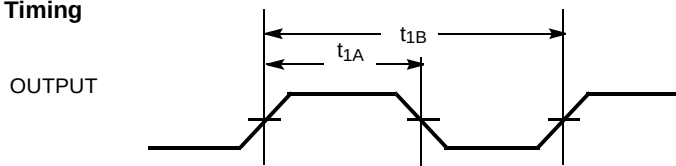
Parameter	Output	Description	Test Conditions	Min.	Typ.	Max.	Unit
t_1	All	Output Duty Cycle ^[9]	$t_1 = t_{1A} \div t_{1B}$	45	50	55	%
t_2	CPUCLK	CPU Clock Rising and Falling Edge Rate	Between 0.4V and 2.0V	1.0		4.0	V/ns
t_2	PCICLK	PCI Clock Rising and Falling Edge Rate	Between 0.4V and 2.4V	1.0		4.0	V/ns
t_2	REF	REF Clock Rising and Falling Edge Rate	Between 0.4V and 2.4V	0.5		2.0	V/ns
t_3	CPUCLK	CPU Clock Rise Time	Between 0.4V and 2.0V	0.4		1.6	ns
t_4	CPUCLK	CPU Clock Fall Time	Between 2.0V and 0.4V	0.4		1.6	ns
t_5	CPUCLK	CPU-CPU Clock Skew	Measured at 1.25V		100	175	ps
t_6	CPUCLK, PCICLK	CPU-PCI Clock Skew	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks	1.5		4.0	ns
t_7	PCICLK, PCICLK	PCI-PCI Clock Skew	Measured at 1.5V			250	ps
t_7	EPCICLK, PCICLK	EPCI-PCI Clock Skew ^[7]	Measured at 1.5V	1.0		4.0	ns
t_{10}	CPUCLK	Cycle-Cycle Clock Jitter	Measured at 1.25V			700	ps
t_{11}	PCICLK	Cycle-Cycle Clock Jitter	Measured at 1.5V			500	ps
t_{12}	CPUCLK, PCICLK	Power-up Time	CPU and PCI clock stabilization from power-up			3	ms
t_{13}	CPUCLK, PCICLK	1/4 Frequency Slew Time ^[7]	Time for CPU, EPCI, and PCI clock frequency to change from f to f/4 after select input change		10	25	cycles

Notes:

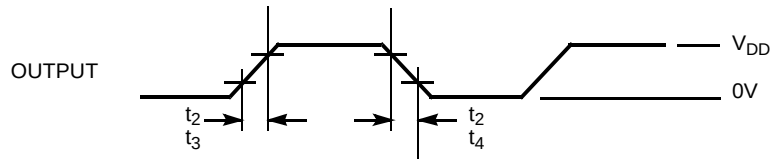
8. All parameters specified with loaded outputs.
9. Duty cycle is measured at 1.5V when $V_{DD} = 3.3V$. When $V_{DD} = 2.5V$, duty cycle is measured at 1.25V.

Switching Waveforms

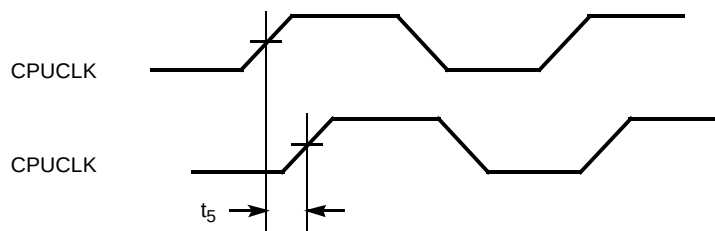
Duty Cycle Timing



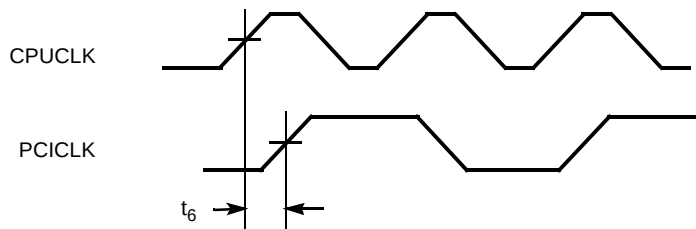
All Outputs Rise/Fall Time



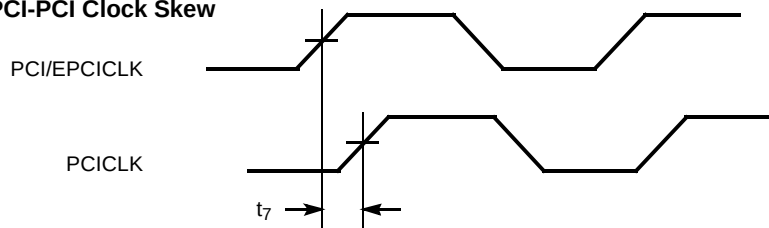
CPU-CPU Clock Skew



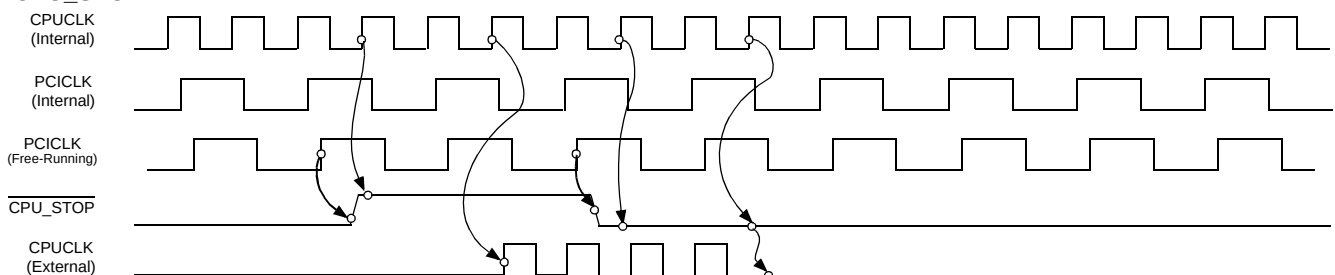
CPU-PCI Clock Skew

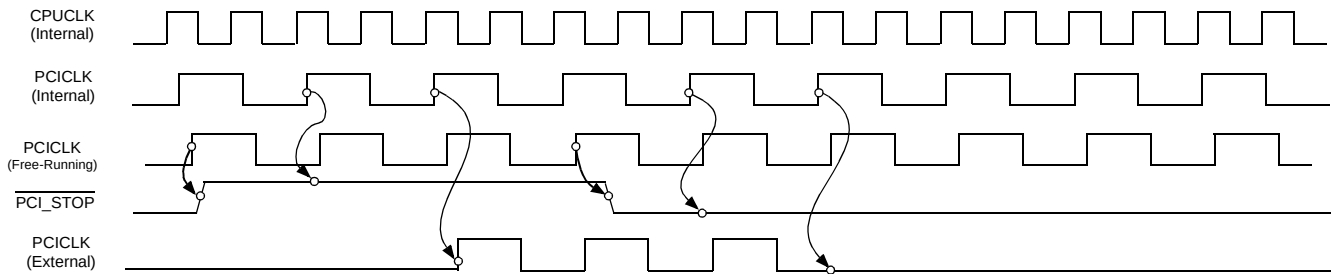
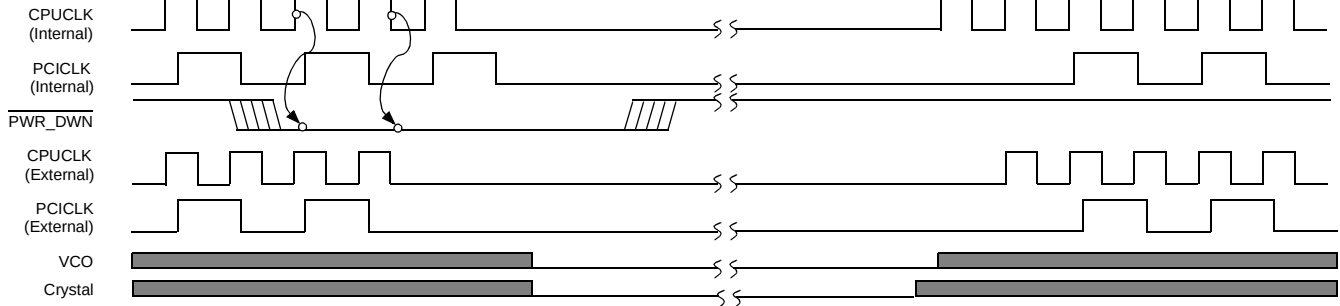


PCI/EPCI-PCI Clock Skew



CPU_STOP



Switching Waveforms (continued)
PCI_STOP

PWR_DOWN


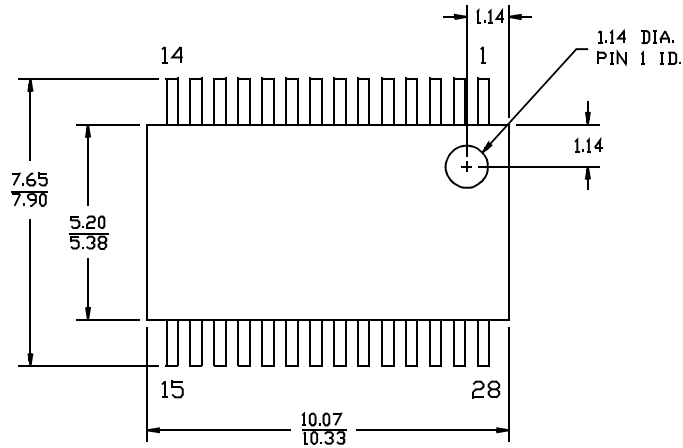
Shaded section on the VCO and Crystal waveforms indicates that the VCO and crystal oscillator are active, and there is a valid clock.

Ordering Information

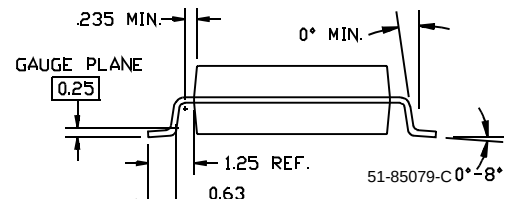
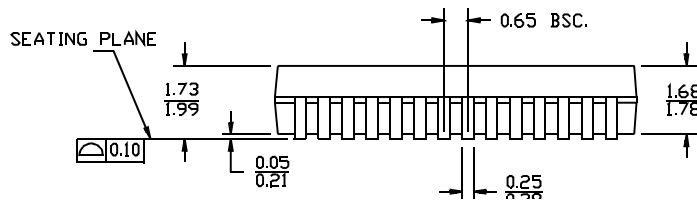
Ordering Code	Package Name	Package Type	Operating Range
CY2285PVC-1	O28	28-Pin SSOP	Commercial
CY2285PVC-2	O28	28-Pin SSOP	Commercial
CY2285PVC-3	O28	28-Pin SSOP	Commercial

Package Diagram

28-Lead (210-Mil) Shrunk Small Outline Package O28



DIMENSIONS IN MILLIMETERS MIN. MAX.



Revision History

Document Title: CY2285 100-MHz Pentium® II Clock Synthesizer/Driver with Spread Spectrum for Mobile PCs Document Number: 38-07205				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	111725	12/16/01	DSG	Change from Spec number: 38-00732 to 38-07205
*A	121840	12/14/02	RBI	Power up requirements added to Operating Conditions Information