HD74HC189 ● 64-bit Random Access Memory

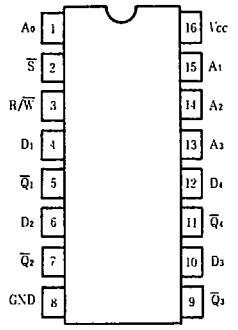
Information to be stored in the memory is written into the selected address location when the chip-select ($\overline{S}$) and the write-enable (R/$\overline{W}$) inputs are low. While the write-enable input is low, the memory outputs are off high-impedance. When a number of outputs are bus-connected, this off state neither loads nor drives the data bus; however, it permits the bus line to be driven by other active outputs or a passive pull-up.

Information stored in the memory (see function table for input/output phase relationship) is available at the outputs when the write-enable input is high and the chip-select input is low. When the chip-select input is high, the outputs will be off.

■ FEATURES

- High Speed Operation
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage: V_{CC}=2~6V
- Low Input Current: 1μA max.
- Low Quiescent Supply Current: I_{CC} (static)=4μA max. (Ta=25°C)

■ PIN ARRANGEMENT



(Top View)

■ FUNCTION TABLE

Function	Inputs		Outputs
	Chip Select	Write Enable	
Write	L	L	Z
Read	L	H	Complement of Data Entered
Inhibit	H	X	Z

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage Range	V_{CC}	−0.5~+7.0	V
Input Voltage	V_{IN}	−0.5~V_{CC}+0.5	V
Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Output Current	I_{OUT}	±35	mA
DC Current Drain per V_{CC}, GND	I_{CC}, I_{GND}	±75	mA
DC Input Diode Current	I_{IK}	±20	mA
DC Output Diode Current	I_{OK}	±20	mA
Power Dissipation per Package	P_T	500	mW
Storage Temperature	T_{stg}	−65~+150	°C

■ DC CHARACTERISTICS

Item	Symbol	V_{CC}(V)	Test Conditions		Ta=25°C min	Ta=25°C typ	Ta=25°C max	Ta=−40~+85°C min	Ta=−40~+85°C max	Unit
Input Voltage	V_{IH}	2.0			1.5	−	−	1.5	−	V
		4.5			3.15	−	−	3.15	−	
		6.0			4.2	−	−	4.2	−	
	V_{IL}	2.0			−	−	0.5	−	0.5	V
		4.5			−	−	1.35	−	1.35	
		6.0			−	−	1.8	−	1.8	
Output Voltage	V_{OH}	2.0	V_{in}=V_{IH} or V_{IL}	I_{OH}=−20μA	1.9	2.0	−	1.9	−	V
		4.5			4.4	4.5	−	4.4	−	
		6.0			5.9	6.0	−	5.9	−	
		4.5		I_{OH}=−6mA	4.18	−	−	4.13	−	
		6.0		I_{OH}=−7.8mA	5.68	−	−	5.63	−	
	V_{OL}	2.0	V_{in}=V_{IH} or V_{IL}	I_{OL}=20μA	−	0.0	0.1	−	0.1	V
		4.5			−	0.0	0.1	−	0.1	
		6.0			−	0.0	0.1	−	0.1	
		4.5		I_{OL}=6mA	−	−	0.26	−	0.33	
		6.0		I_{OL}=7.8mA	−	−	0.26	−	0.33	
Off-state output current	I_{OZ}	6.0	V_{in}=V_{IH} or V_{IL}, V_{out}=V_{CC} or GND		−	−	±0.5	−	±5.0	μA
Input Current	I_{in}	6.0	V_{in}=V_{CC} or GND		−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	6.0	V_{in}=V_{CC} or GND, I_{out}=0μA		−	−	4.0	−	40	μA

HITACHI
Hitachi America Ltd. • 2210 O'Toole Avenue • San Jose, CA 95131 • (408) 435-8300

■ AC CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

Item	Symbol	Vcc(V)	Test Conditions	Ta=25°C min.	Ta=25°C typ.	Ta=25°C max.	Ta=−40~+85°C min.	Ta=−40~+85°C max.	Unit
Access Time from Address	$t_{a(ad)}$	2.0		—	—	400	—	500	ns
		4.5		—	—	80	—	100	
		6.0		—	—	68	—	86	
Access Time from Chip Select (Enable Time)	$t_{a(s)}$	2.0		—	—	300	—	380	ns
		4.5		—	—	60	—	76	
		6.0		—	—	52	—	66	
Sense Recovery Time	t_{SR}	2.0		—	—	450	—	560	ns
		4.5		—	—	90	—	112	
		6.0		—	—	76	—	96	
Disable Time from High or Low Level	t_{PXZ}	2.0	from $\overline{S}$	—	—	250	—	315	ns
		4.5		—	—	50	—	63	
		6.0		—	—	43	—	54	
	t_{PXZ}	2.0	from R/$\overline{W}$	—	—	300	—	380	ns
		4.5		—	—	60	—	76	
		6.0		—	—	52	—	66	
Setup Time	t_{su}	2.0	Address to R/$\overline{W}$	100	—	—	125	—	ns
		4.5		20	—	—	25	—	
		6.0		17	—	—	21	—	
	t_{su}	2.0	Data to R/$\overline{W}$	300	—	—	380	—	ns
		4.5		60	—	—	76	—	
		6.0		52	—	—	66	—	
	t_{su}	2.0	Chip Select to R/$\overline{W}$	300	—	—	380	—	ns
		4.5		60	—	—	76	—	
		6.0		52	—	—	66	—	
Hold Time	t_h	2.0	R/$\overline{W}$ to Address	50	—	—	65	—	ns
		4.5		10	—	—	13	—	
		6.0		9	—	—	11	—	
	t_h	2.0	R/$\overline{W}$ to Data	50	—	—	65	—	ns
		4.5		10	—	—	13	—	
		6.0		9	—	—	11	—	
	t_h	2.0	R/$\overline{W}$ to Chip Select	50	—	—	65	—	ns
		4.5		10	—	—	13	—	
		6.0		9	—	—	11	—	
Output Rise/Fall Time	t_{TLH} t_{THL}	2.0		—	—	60	—	75	ns
		4.5		—	—	12	—	15	
		6.0		—	—	10	—	13	
Input Capacitance	C_{in}	—		—	5	10	—	10	pF

PACKAGE INFORMATION

T-90-20

In the HD74HC series of HS-CMOS logic, either of plastic DIP and small outline packages can be selected.
For your ordering, please refer to the following package code.

●Package code of HS-CMOS Logic

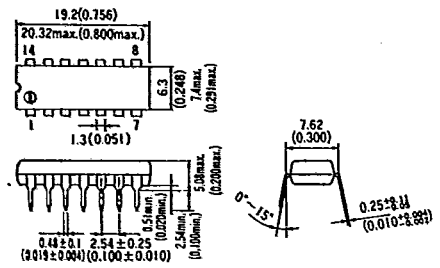
HD74HC XXXX P

- P : Package code (P : Plastic DIP, FP : Small outline package)
- XXXX : Individual device code
- HC : Series code of HS-CMOS logic
- HD74 : Initial code of Hitachi digital IC

■PLASTIC DIP PACKAGE [Unit: mm(inch), scale: 1/1]

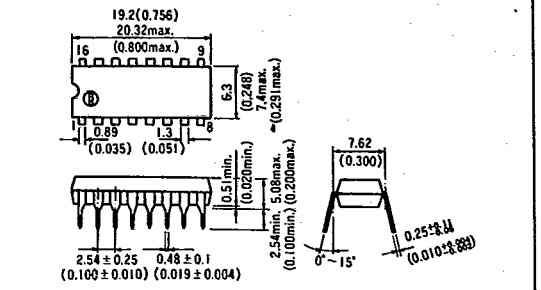
●14-pin type

DP-14



●16-pin type

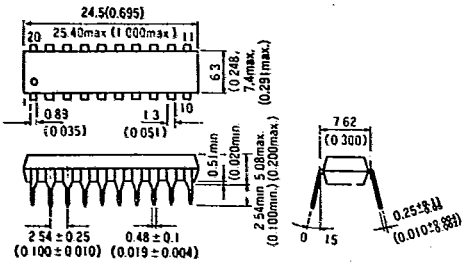
DP-16



Note) For the present, both packages of 0.89 and 1.3 can be used. Please refer to the Technical Marketing Dept. for further details.

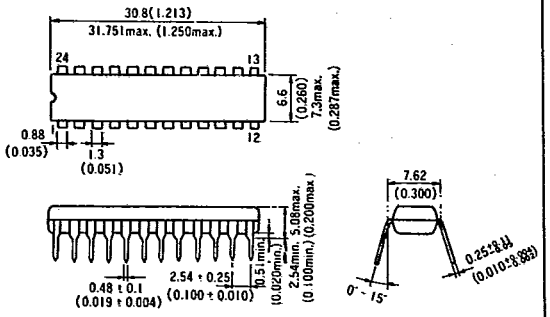
●20-pin type

DP-20N



●24-pin type

DP-24N



Note) Because this is under development, the dimentions may be changed partly.

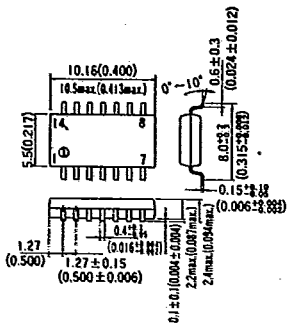
0571 F-06

PACKAGE INFORMATION

■SMALL OUTLINE PACKAGE [Unit: mm(inch), scale: 1½]

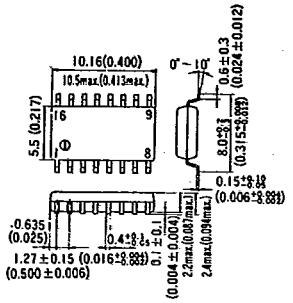
●14—pin type

FP—14D



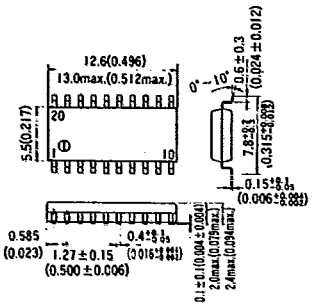
●16—pin type

FP—16D



●20—pin type

FP—20DN



Note) Preliminary

HITACHI
Hitachi America Ltd. • 2210 O'Toole Avenue • San Jose, CA 95131 • (408) 435-8300