HY5117404B Series

4M x 4-bit CMOS DRAM with Extended Data Out

PRELIMINARY

DESCRIPTION

The HY5117404B is the new generation and fast dynamic RAM organized 4,194,304 x 4-bit. The HY5117404B utilizes Hyundai's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins to the users. Multiplexed address inputs permit the HY5117404B to be packaged in standard 24/26 pin plastic SOJ, TSOP-II and Reverse TSOP-II.
The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipments. System oriented feature includes single power supply of 5V ±10% tolerance and direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- **Low power dissipation**
  Max. battery back-up 2.75mW (SL-part)
  Max. CMOS standby 2.2mW (SL-part)
  5.5mW
  Max. TTL standby 11.0mW
  Max. operating

Speed	Power
50	798mW
60	660mW
70	550mW

- **Single power supply of 5V±10%**
- **TTL compatible inputs and outputs**
- **Fast access and cycle time**

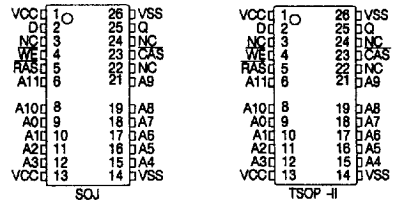
Speed	tRAC	tCAC	tHPC
50	50ns	13ns	20ns
60	60ns	15ns	25ns
70	70ns	18ns	30ns

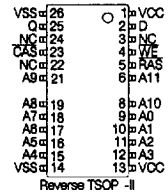
- **Extended data out operation**
- **Multi-bit test capability**
- **Read-Modify-Write capability**
- **$\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only, Hidden refresh and Self Refresh capability**
- **2048 refresh cycles / 256ms (SL-part)**
  2048 refresh cycles / 32ms

PIN DESCRIPTION

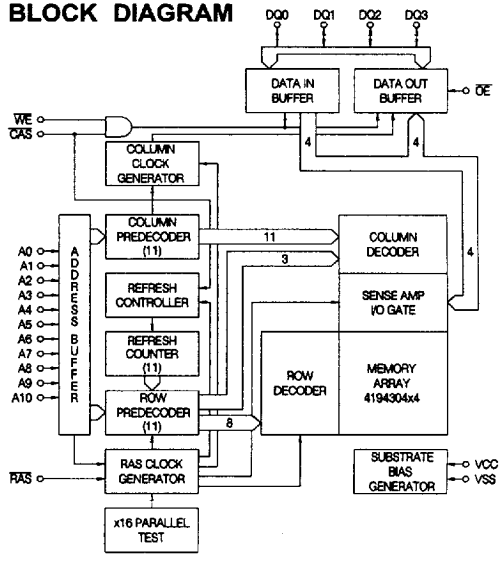
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
A0-A10	Address input
DQ0-DQ3	Data Input/Output
Vcc	Power (+5V)
Vss	Ground

PIN CONNECTION





BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	-55 to 150	°C
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to Vss	-1.0 to 7.0	V
V_{CC}	Voltage on Vcc Relative to Vss	-1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	1.0	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec

NOTE: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	-	Vcc+1.0	V
V_{IL}	Input Low Voltage	-1.0	-	0.8	V

NOTE: All Voltage are referenced to V_{SS}.

DC CHARACTERISTICS

(T_A=0°C to 70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
I_{LI}	Input Leakage Current (Any Input Pins)	$V_{SS} \le V_{IN} \le V_{CC}$+1.0, All other pins not under test = Vss		-10	10	µA	
I_{LO}	Output Leakage Current (High impedance State)	$V_{SS} \le V_{OUT} \le V_{CC}$ $\overline{RAS}$ & $\overline{CAS}$ at V_{IH}		-10	10	µA	
I_{CC1}	Vcc Supply Current, Operating	t_{RC} = t_{RC} (min.)	50 60 70	- - -	145 120 100	mA	1,2,3
I_{CC2}	Vcc Supply Current, Operating.	$\overline{RAS}$ & $\overline{CAS}$ at V_{IH}(min.), other inputs ≥ V_{SS}		-	2	mA	
I_{CC3}	Vcc Supply Current, $\overline{RAS}$-only refresh	t_{RC} = t_{RC} (min.)	50 60 70	- - -	145 120 100	mA	1,3
I_{CC4}	Vcc Supply Current, EDO mode	t_{PC} = t_{PC} (min.)	50 60 70	- - -	130 110 90	mA	1,2,3
I_{CC5}	Vcc Supply Current, CMOS Standby	$\overline{RAS}$ & $\overline{CAS}$ ≤ Vcc-0.2V	 SL-part	- -	1 0.4	mA	5
I_{CC6}	Vcc Supply Current, $\overline{CAS}$-before- $\overline{RAS}$ refresh	t_{RC} = t_{RC} (min.)	50 60 70	- - -	145 120 100	mA	1,3
I_{CC7}	Vcc Supply Current, Battery Back up (SL-part only)	t_{RC} = 125µs, $\overline{CAS}$ = CBR cycling or 0.2V, WE = Vcc-0.2V, A0-A10 = Vcc-0.2V or 0.2V, DQ0-D Q3 = 0.2V, Vcc-0.2V or open	t_{RAS} ≤ 300ns t_{RAS} ≤ 1 µs	- -	300 500	µA	1,4,5
I_{CC8}	Vcc Supply Current Self Refresh (SL-part only)	$\overline{RAS}$ & $\overline{CAS}$ ≤ 0.2V $\overline{OE}$ & $\overline{WE}$ & A0-A10= Vcc-0.2V or 0.2V, DQ0-DQ3=Vcc-0.2V,0.2V or open		-	300	µA	5
V_{OL}	Output Low Voltage	I_{OL} = 4.2mA		-	0.4	V	
V_{OH}	Output High Voltage	I_{OH} = -5.0mA		2.4	-	V	

NOTE :

1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} and I_{CC7} depend on cycle rates.
2. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on output loading. Specified values are obtained with the output open.
3. I_{CC} is specified as average current. I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. I_{CC4}, Address can be changed maximum once while $\overline{CAS}$=V_{IH}.
4. t_{RAS}(max.)=1µs is only applied to refresh of battery backup but t_{RAS}(max.)=10µs is applied to normal functional operation .
5. I_{CC5}(max.) =0.4mA and I_{CC7} and I_{CC8} are applied to SL-parts only.

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{CC}=5V ±10%, V_{SS}=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	HY5117404BJC/TC/RC/SLJC/SLT/SLRC						UNIT	NOTE
			-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	84	-	104	-	124	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	113	-	137	-	160	-	ns	
3	tHPC	EDO Mode Cycle Time	20	-	25	-	30	-	ns	15
4	tHPRWC	EDO Mode Read-Modify-Write Cycle Time	61	-	70	-	78	-	ns	15
5	tRAC	Access Time from $\overline{RAS}$	-	50	-	60	-	70	ns	4,9,10
6	tCAC	Access Time from $\overline{CAS}$	-	13	-	15	-	18	ns	4,9
7	tAA	Access Time from Column Address	-	25	-	30	-	35	ns	4,10
8	tCPA	Access Time from $\overline{CAS}$ Precharge	-	30	-	35	-	40	ns	4
9	tCLZ	$\overline{CAS}$ to Output Low Impedance	3	-	3	-	3	-	ns	4
10	tCEZ	Output Buffer Turn-off Delay Time from $\overline{CAS}$	3	13	3	15	3	18	ns	5
11	tT	Transition Time (Rise and Fall)	2	50	2	50	2	50	ns	3
12	tRP	$\overline{RAS}$ Precharge Time	30	-	40	-	50	-	ns	
13	tRAS	$\overline{RAS}$ Pulse Width	50	10K	60	10K	70	10K	ns	
14	tRASP	$\overline{RAS}$ Pulse Width (EDO Mode)	50	200K	60	200K	70	200K	ns	
15	tRSH	$\overline{RAS}$ Hold Time	13	-	15	-	18	-	ns	
16	tCSH	$\overline{CAS}$ Hold Time	40	-	45	-	50	-	ns	
17	tCAS	$\overline{CAS}$ Pulse width	8	10K	11	10K	14	10K	ns	
18	tRCD	$\overline{RAS}$ to $\overline{CAS}$ Delay	18	37	20	45	20	52	ns	9
19	tRAD	$\overline{RAS}$ to Column Address Delay Time	10	25	15	30	15	35	ns	10
20	tCRP	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	ns	
21	tCP	$\overline{CAS}$ Precharge Time	8	-	10	-	12	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold time	8	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	10	-	10	-	10	-	ns	
26	tAR	Column Address Hold Time from $\overline{RAS}$	50	-	50	-	50	-	ns	
27	tRAL	Column Address to $\overline{RAS}$ Lead Time	25	-	30	-	35	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to $\overline{CAS}$	0	-	0	-	0	-	ns	6
30	tRRH	Read Command Hold Time Referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	6
31	tWCH	Write Command Hold Time	8	-	10	-	10	-	ns	
32	tWCR	Write Command Hold Time from $\overline{RAS}$	45	-	50	-	55	-	ns	
33	tWP	Write Command Pulse Width	8	-	10	-	10	-	ns	
34	tRWL	Write Command to $\overline{RAS}$ Lead Time	10	-	12	-	12	-	ns	
35	tCWL	Write Command to $\overline{CAS}$ Lead Time	10	-	12	-	12	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	10	-	10	-	10	-	ns	7
38	tDHR	Data-In Hold Time Referenced to $\overline{RAS}$	50	-	50	-	50	-	ns	
39	tREF	Refresh Period (2048 cycles)	-	32	-	32	-	32	ms	12
		SL-part	-	256	-	256	-	256	ms	11
40	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	8

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HY5117404BJ/T/R/SLJ/SLT/SLR						UNIT	NOTE
			-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCWD	$\overline{CAS}$ to $\overline{WE}$ Delay Time	30	-	34	-	40	-	ns	8
42	tRWD	$\overline{RAS}$ to $\overline{WE}$ Delay Time	67	-	79	-	92	-	ns	8
43	tAWD	Column Address to $\overline{WE}$ Delay Time	42	-	49	-	57	-	ns	8
44	tCSR	$\overline{CAS}$ Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	
45	tCHR	$\overline{CAS}$ Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
46	tRPC	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	-	5	-	5	-	ns	
47	tCPT	$\overline{CAS}$ Precharge Time (CBR Counter Test)	15	-	20	-	25	-	ns	
48	tROH	$\overline{RAS}$ Hold Time Reference to $\overline{OE}$	10	-	10	-	10	-	ns	
49	tOEA	$\overline{OE}$ Access Time	-	13	-	15	-	18	ns	
50	tOED	$\overline{OE}$ to Data Delay	13	-	15	-	18	-	ns	
51	tOEZ	Output Buffer Turn Off Delay Time from $\overline{OE}$	3	13	3	15	3	18	ns	5
52	tOEH	$\overline{OE}$ Command Hold Time	13	-	15	-	18	-	ns	
53	tCPWD	$\overline{WE}$ Delay Time from $\overline{CAS}$ Precharge	47	-	54	-	62	-	ns	8
54	tRHCP	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	30	-	35	-	40	-	ns	
55	tWRP	$\overline{WE}$ to $\overline{RAS}$ Precharge Time (CBR Cycle)	10	-	10	-	10	-	ns	
56	tWRH	$\overline{WE}$ to $\overline{RAS}$ Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
57	tWTS	Write Command Set-up Time (Test Mode In)	10	-	10	-	10	-	ns	
58	tWTH	Write Command Hold Time (Test Mode In)	10	-	10	-	10	-	ns	
59	tRASS	$\overline{RAS}$ Pulse Width (Self Refresh Cycle)	100	-	100	-	100	-	ns	
60	tRPS	$\overline{RAS}$ Precharge Time (Self Refresh Cycle)	90	-	110	-	130	-	ns	
61	tCHS	$\overline{CAS}$ Hold Time (Self Refresh Cycle)	-50	-	-50	-	-50	-	ns	
62	tDOH	Output Data Hold Time	5	-	5	-	5	-	ns	
63	tREZ	Output Buffer Turn Off Delay Time from $\overline{RAS}$	3	13	3	15	3	18	ns	5
64	tWEZ	Output Buffer Turn Off Delay Time from $\overline{WE}$	3	13	3	15	3	18	ns	5
65	tWED	$\overline{WE}$ to Data Delay Time	13	-	15	-	18	-	ns	
66	tOEP	$\overline{OE}$ Hige Pulse Width	5	-	5	-	8	-	ns	
67	tWPE	$\overline{WE}$ Pulse Width (Hyper Page Cycle)	5	-	5	-	8	-	ns	
68	tOCH	$\overline{OE}$ to $\overline{CAS}$ Hold Time	0	-	0	-	0	-	ns	
69	tCHO	$\overline{CAS}$ Hold Time to $\overline{OE}$	5	-	5	-	8	-	ns	

AC CHARACTERISTICS IN TEST MODE

NOTE 13

#	SYMBOL	PARAMETER	HY5117404BJC/TC/RC/SLJC/SLTC/SLR						UNIT	NOTE
			-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX		
1	tRC	Random Read or Write Cycle Time	95	-	115	-	135	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	140	-	160	-	185	-	ns	
3	tPC	Fast Page Mode Cycle Time	25	-	30	-	35	-	ns	
4	tHPRWC	Fast Page Mode Read-Modify-Write Cycle Time	70	-	80	-	90	-	ns	
5	tRAC	Access Time from $\overline{RAS}$	-	55	-	65	-	75	ns	4,9,10
6	tCAC	Access Time from $\overline{CAS}$	-	18	-	20	-	23	ns	4,9
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	4,10
8	tCPA	Access Time from $\overline{CAS}$ Precharge	-	35	-	40	-	45	ns	4
13	tRAS	$\overline{RAS}$ Pulse Width	55	10K	65	10K	75	10K	ns	
14	tRASP	$\overline{RAS}$ Pulse Width (Fast Page Mode)	55	200K	65	200K	75	200K	ns	
15	tRSH	$\overline{RAS}$ Hold Time	18	-	20	-	23	-	ns	
16	tCSH	$\overline{CAS}$ Hold Time	45	-	50	-	55	-	ns	
17	tCAS	$\overline{CAS}$ Pulse Width	18	10K	20	10K	23	10K	ns	
27	tRAL	Column Address to $\overline{RAS}$ Lead Time	30	-	35	-	40	-	ns	
41	tCWD	$\overline{CAS}$ to $\overline{WE}$ Delay Time	40	-	45	-	50	-	ns	8
42	tRWD	$\overline{RAS}$ to $\overline{WE}$ Delay Time	75	-	90	-	100	-	ns	8
43	tAWD	Column Address to $\overline{WE}$ Delay Time	50	-	60	-	65	-	ns	8
49	tOEA	$\overline{OE}$ Access Time	-	18	-	20	-	23	ns	
50	tOED	$\overline{OE}$ to Data Delay	18	-	20	-	23	-	ns	
52	tOEH	$\overline{OE}$ Command Hold Time	18	-	20	-	23	-	ns	

NOTE:

1. An initial pause of 200μs is required after power-up followed by any 8 refresh ($\overline{RAS}$ only $\overline{CAS}$-before-$\overline{RAS}$ refresh) cycle before proper device operation is achieved.
2. If $\overline{RAS}$=Vss during power-up, the device could begin an active cycle. These condition results in higher current than necessary which is demanded from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with Vcc during power-up or be held at a valid V_{IH} in order to minimize the power-up current.
3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH}(min.) and V_{IL}(max.), and are assumed to be 5ns for all inputs.
4. Measured at V_{OH}=2.0V and V_{OL}=0.8V with a load equivalent to 2 TTL loads and 100pF.
5. These parameters define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and $\overline{WE}$ leading edge in Read-Modify-Write cycles.
8. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.), and $t_{CPWD} \geq t_{CPWD}$(min.), the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminated.
9. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
10. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
11. t_{REF}(max.)=256ms is applied to SL-Parts (HY5117404BSLJ, HY5117404BSLT and HY5117404BSLR).
12. A burst of 2048 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles must be executed within 64ms(256ms for SL-part) after exiting self refresh.
13. These specifications are applied to the test Mode.
14. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high befoer $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
15. $t_{ASC} \geq t_{CP}$ (min.), Assume tT= 2ns

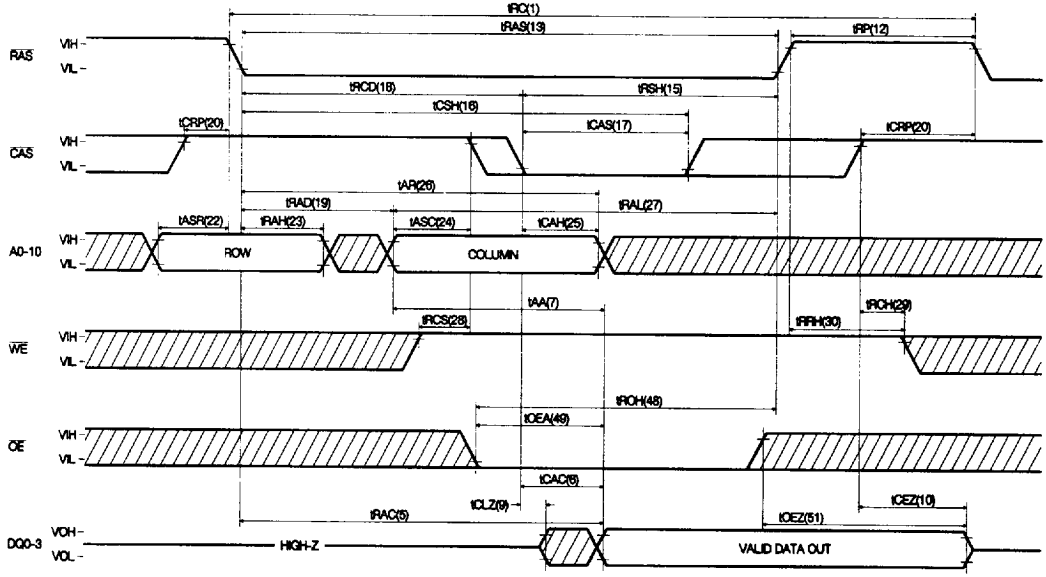
CAPACITANCE

(T_A=25°C, Vcc=5V±10%, Vss=0V, f=1MHz, unless otherwise noted.)

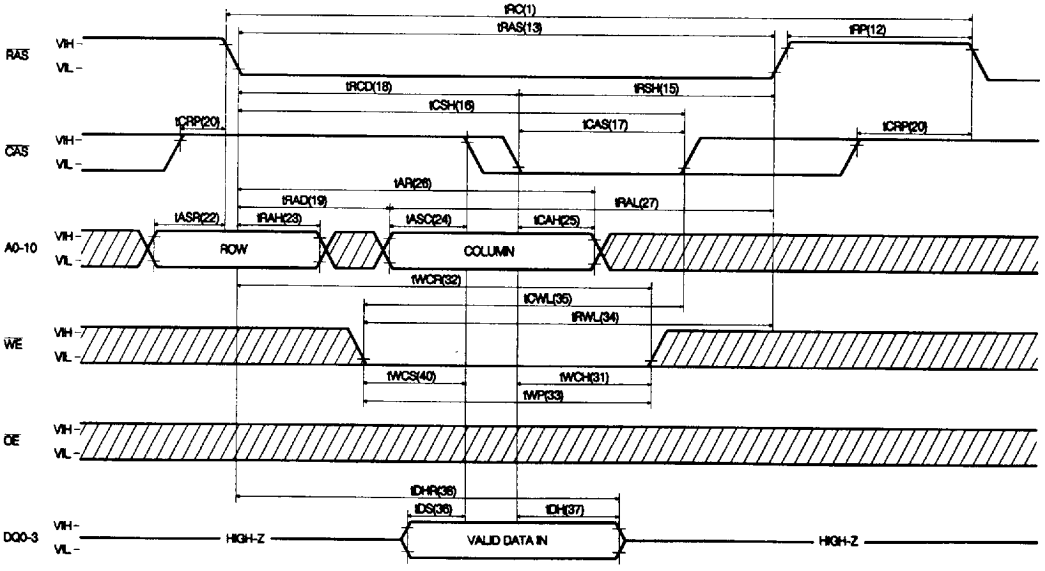
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance (A0-A10)	-	5	pF
C_{IN2}	Input Capacitance ($\overline{RAS}$,$\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	-	7	pF
C_{DQ}	Data Input/Output Capacitance (DQ0-DQ3)	-	7	pF

TIMING DIAGRAM

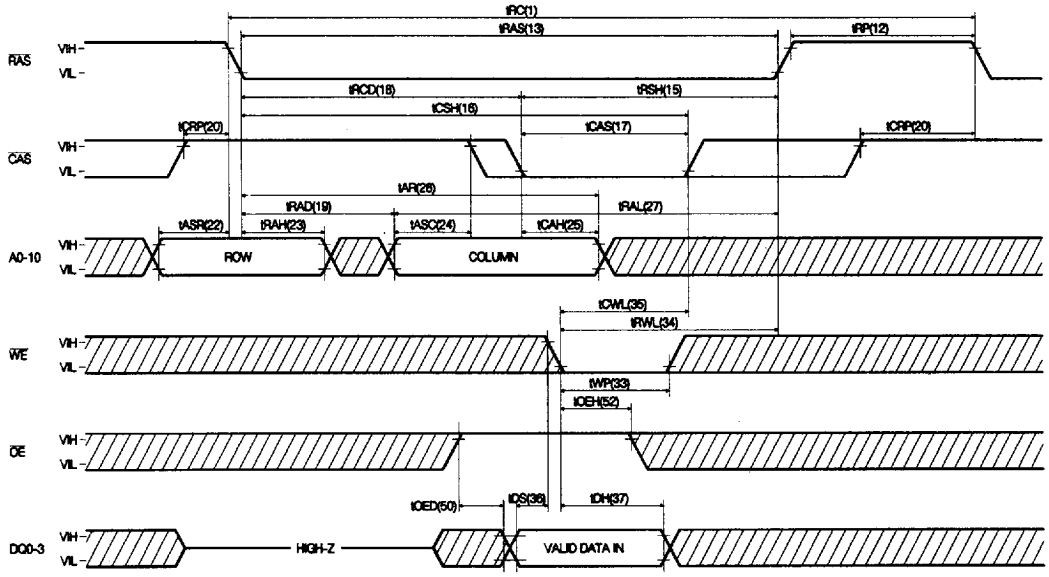
READ CYCLE



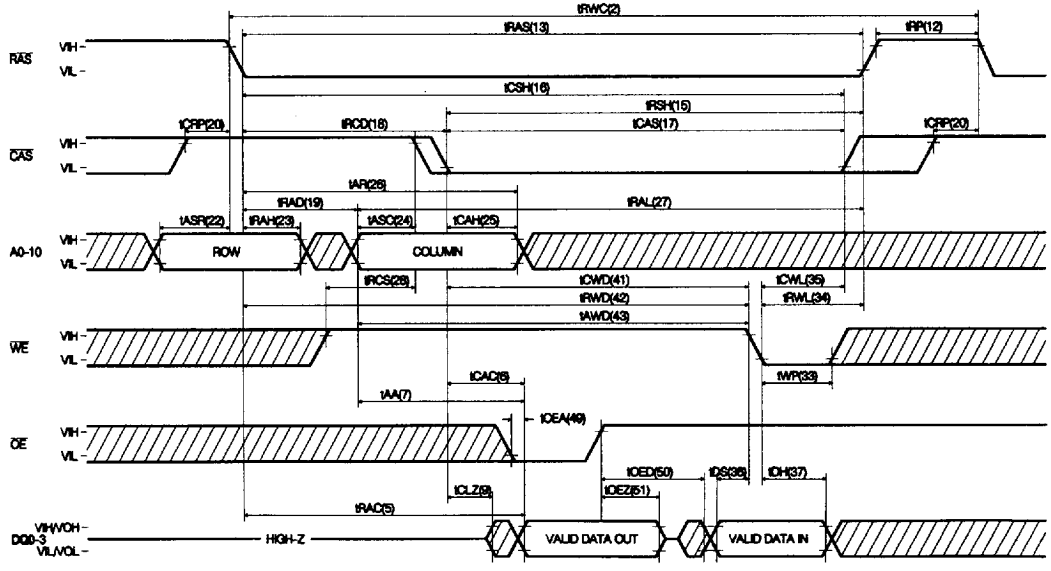
EARLY WRITE CYCLE



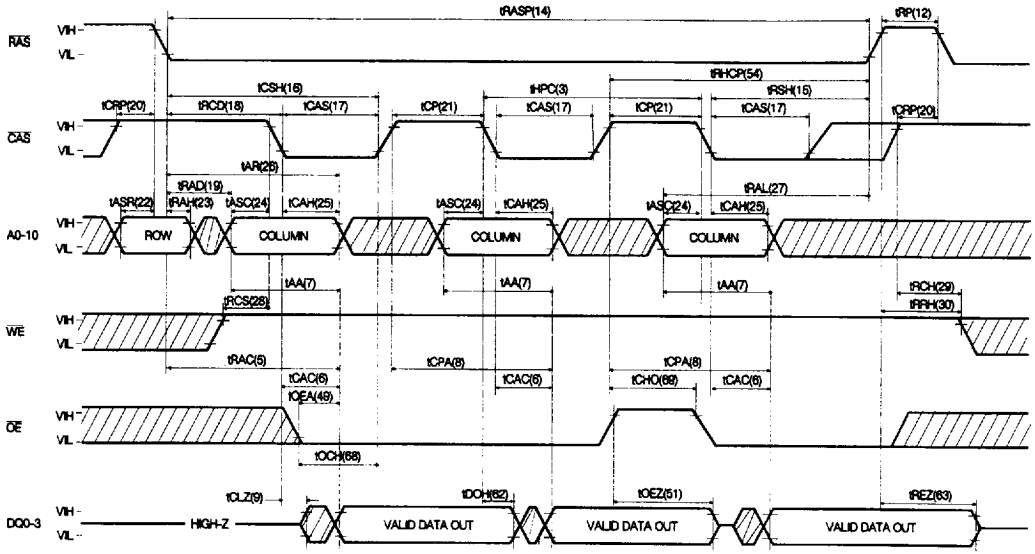
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



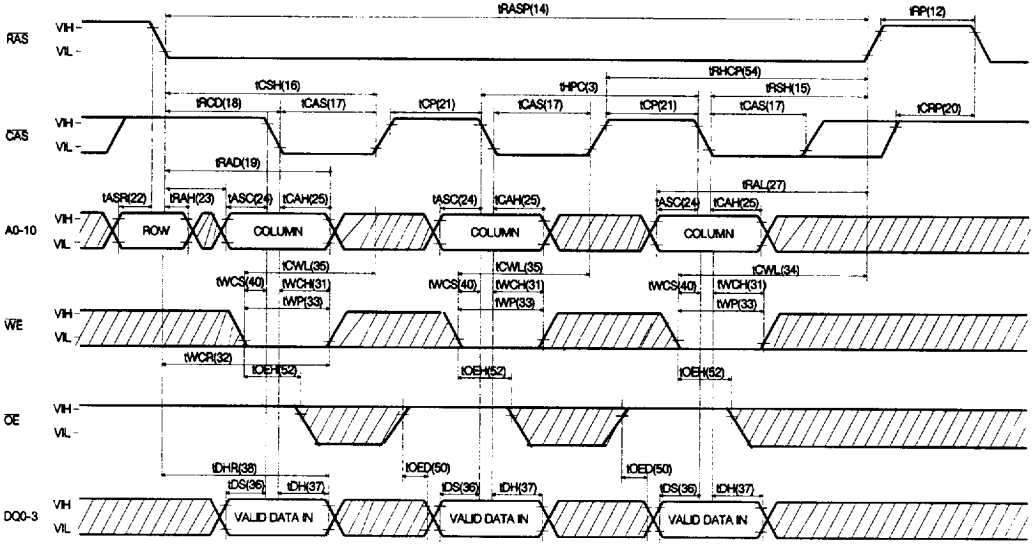
READ-MODIFY-WRITE CYCLE



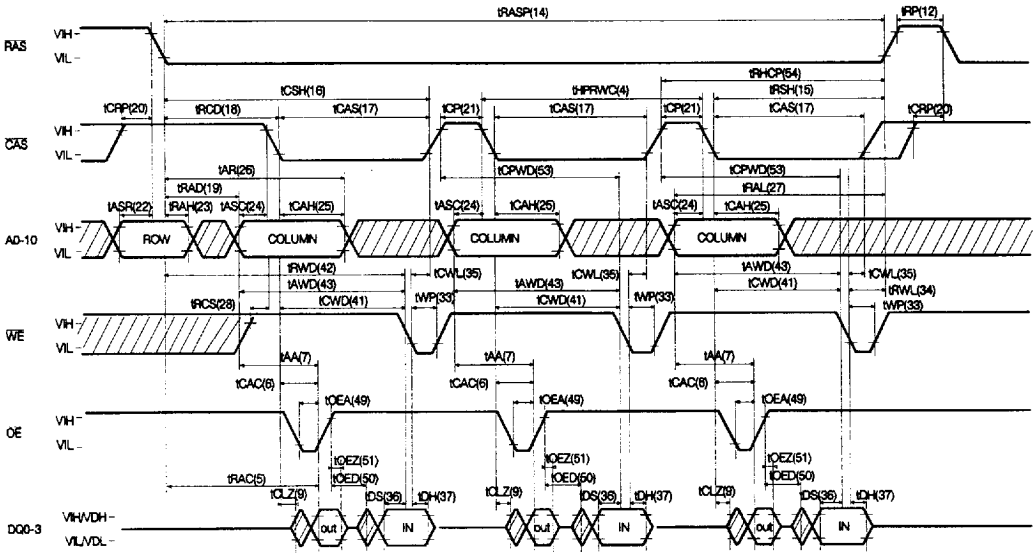
EDO MODE READ CYCLE



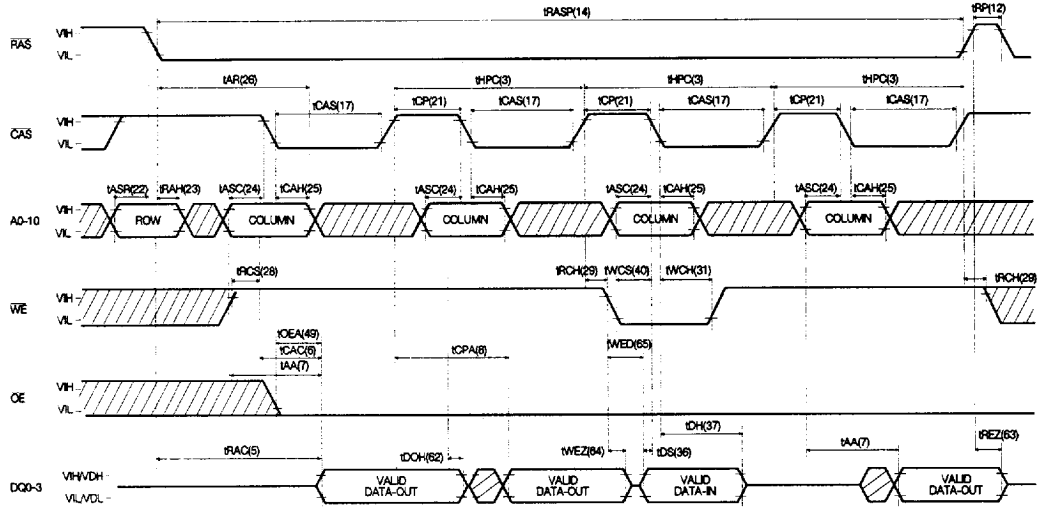
EDO MODE EARLY WRITE CYCLE



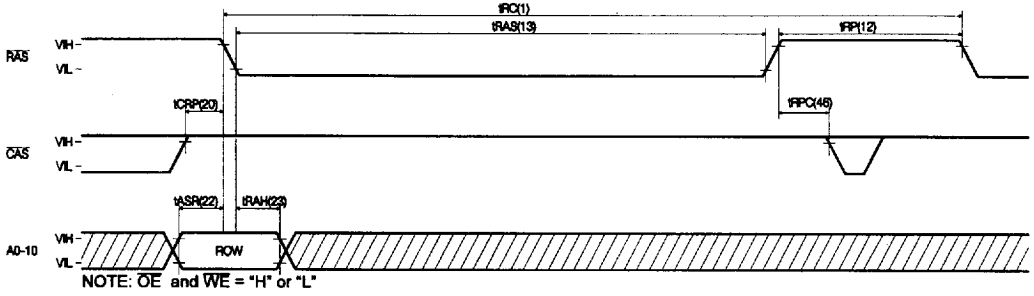
EDO MODE READ-MODIFY-WRITE CYCLE



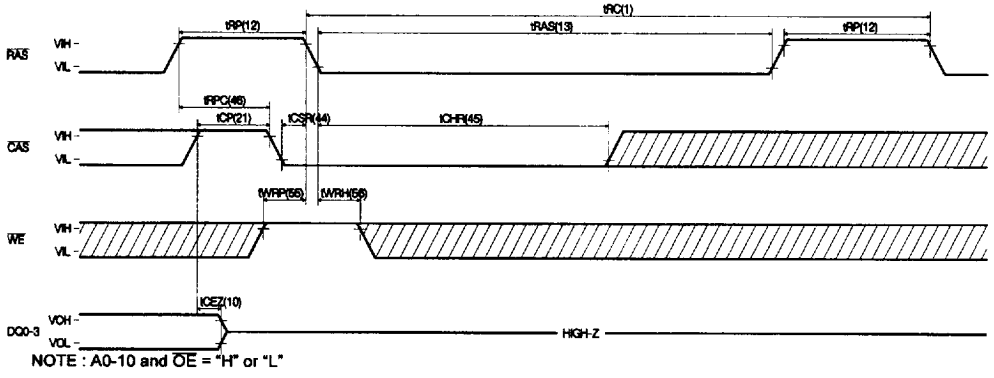
EDO MODE READ AND WRITE MIXED CYCLE



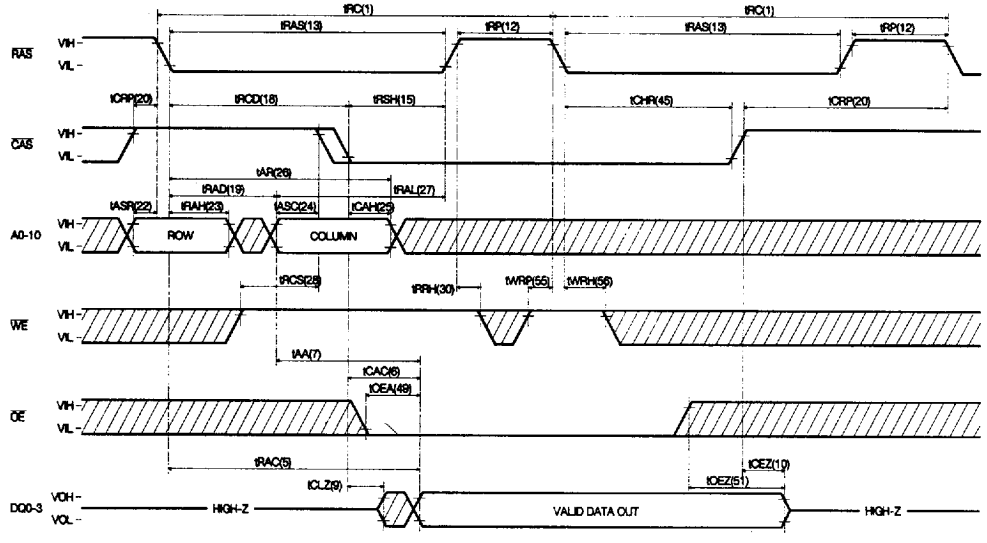
$\overline{RAS}$-ONLY REFRESH CYCLE



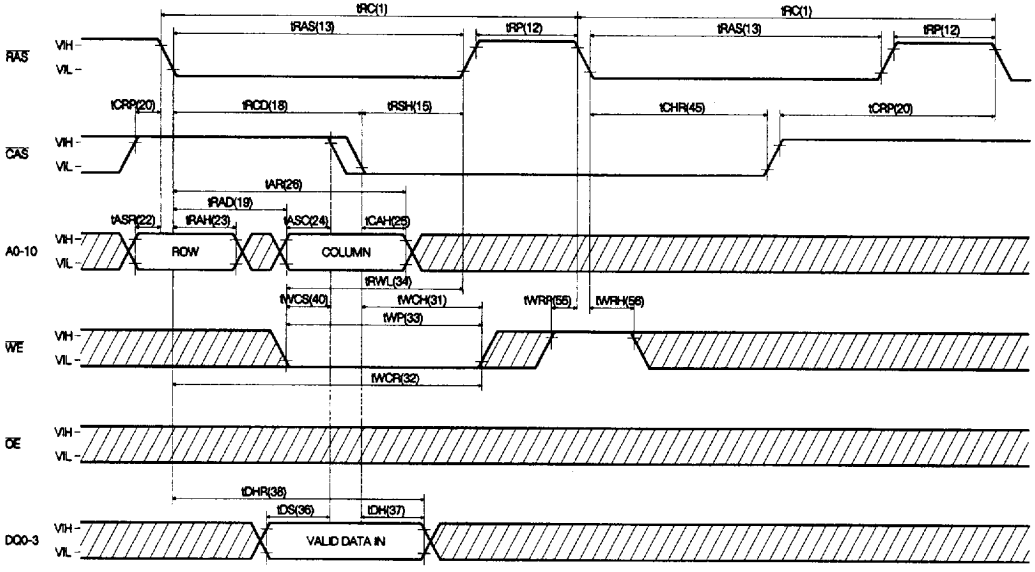
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



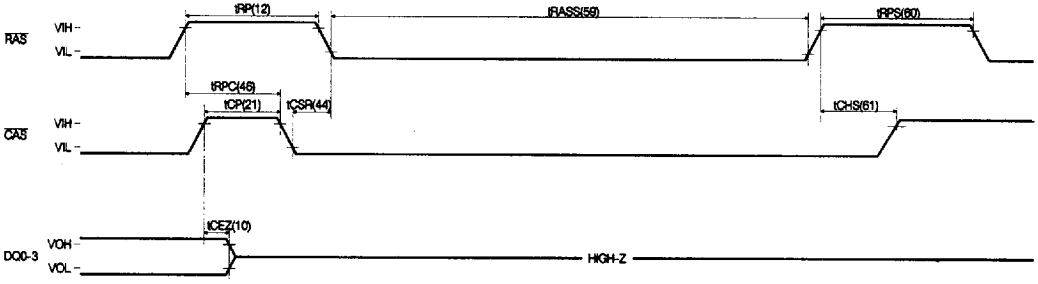
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

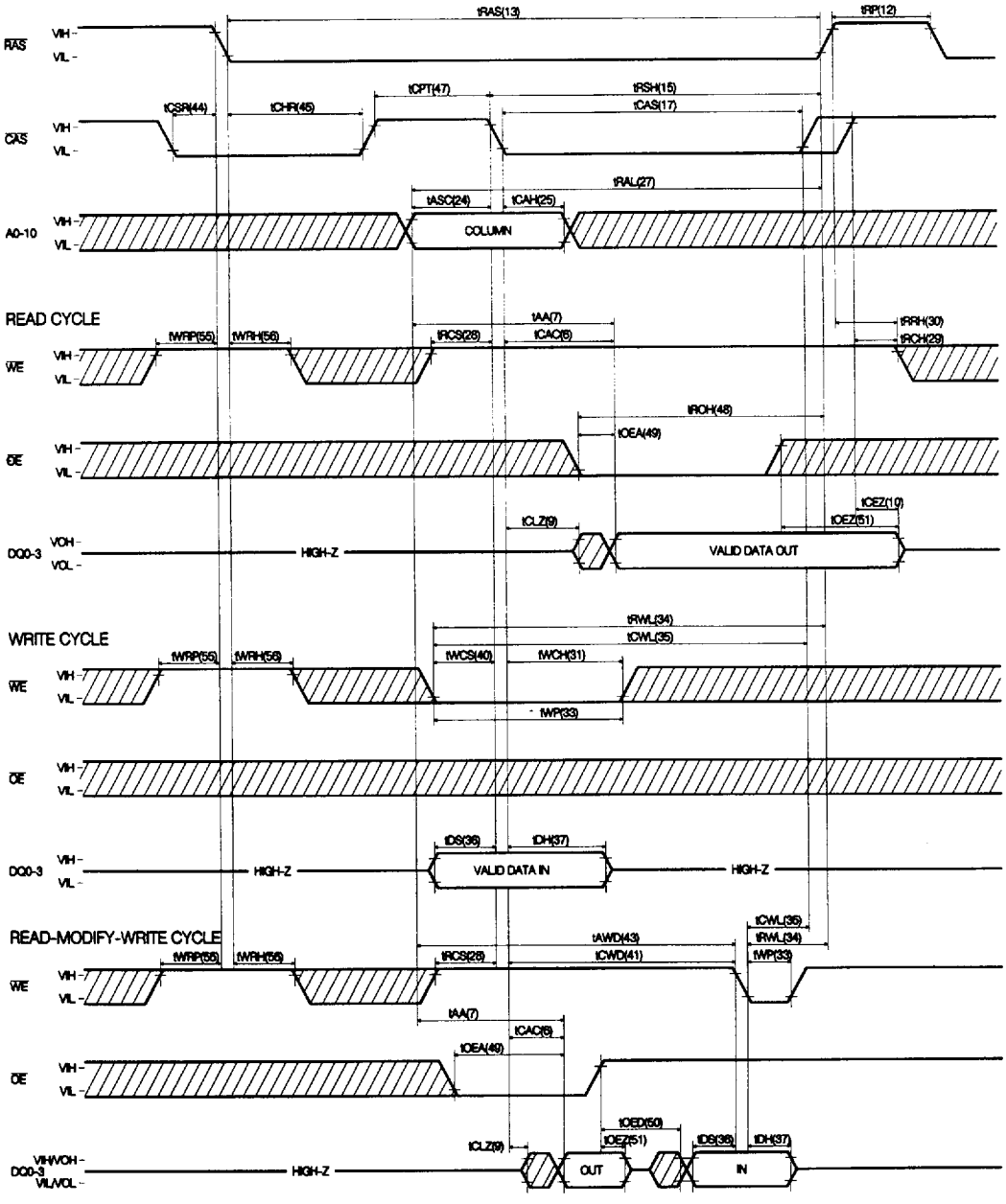


CAS-BEFORE-RAS SELF REFRESH CYCLE



NOTE : A0-10 $\overline{OE}$ and $\overline{WE}$ ="H" or "L"

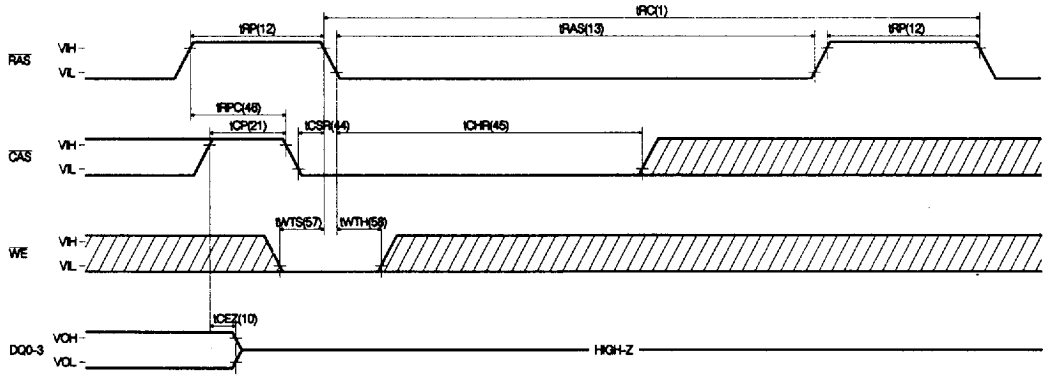
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



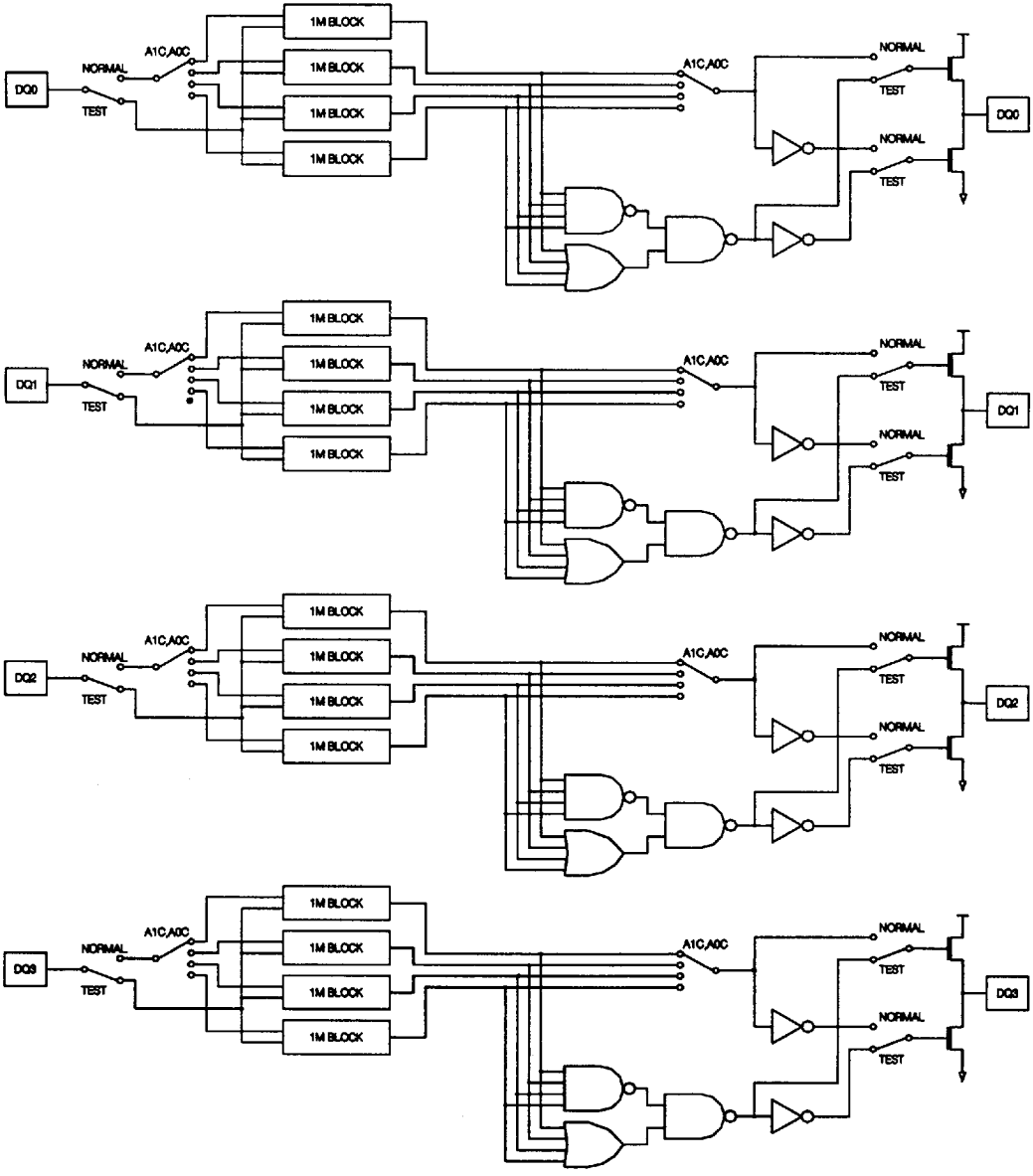
TEST MODE

The HY511704B is a DRAM organized 4,194,304 x 4-bit. It is internally organized 1,048,576 x 16-bit. In Test Mode, data are written into 16 sectors (Each is composed of 1M bits) in parallel and retrieved the same way. Column address A0 and A1 are not used. If, upon reading, 4-bit data from 4 sectors connected to one DQ pin are equal (all "1"s or "0"s), the DQ pin indicates a "1". If they are not equal, the DQ pin indicates a "0". Belowing shows the timing diagram of the HY5117404B to enter Test Mode. In Test Mode, the 4M x 4 DRAM can be tested as if it were a 1M x 4 DRAM. $\overline{WE}$, $\overline{CAS}$-before-$\overline{RAS}$ cycle (Test Mode In Cycle) puts the HY5117404B into Test Mode and $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$-only refresh cycle puts it back into Normal Model. In Test Mode, $\overline{WE}$, $\overline{CAS}$-before-$\overline{RAS}$ cycle shall be used for the refresh operation. The Test Mode function refuces test time(1/4 in case of N test pattern).

TEST MODE IN CYCLE

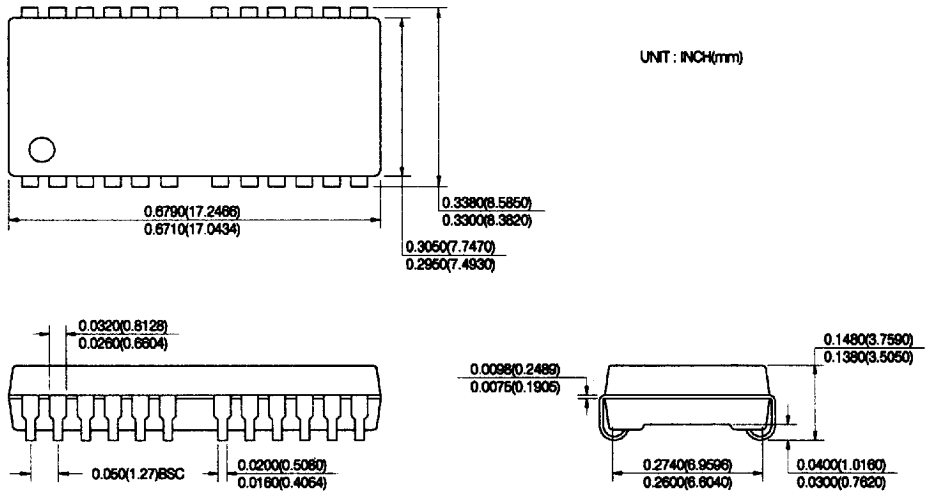


BLOCK DIAGRAM IN TEST MODE

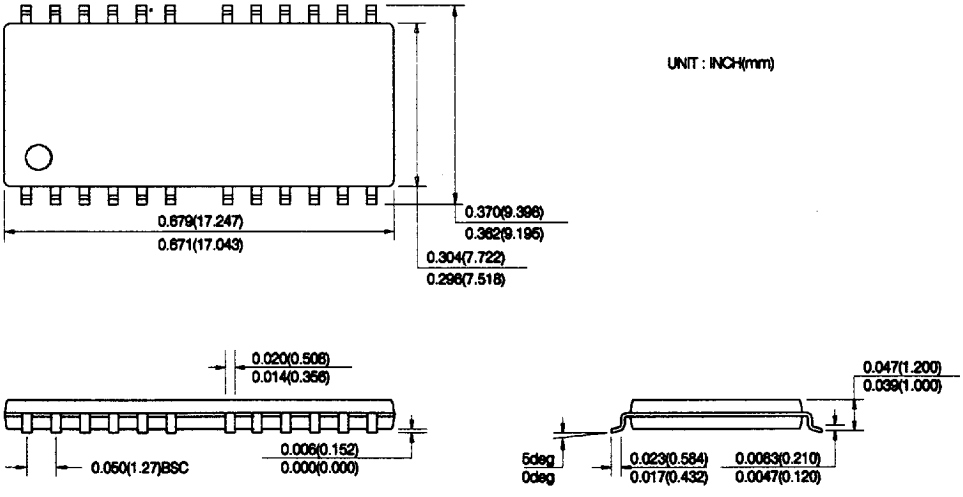


PACKAGE INFORMATION

300 mil 24/26 pin Small Outline J-form Package (J)



300 mil 24/26 pin Thin Small Outline Package (T) (R)



ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE
HY5117404BJ	50/60/70		SOJ
HY5117404BLJ	50/60/70	SL-part	SOJ
HY5117404BAT	50/60/70		TSOP-II
HY5117404BSLT	50/60/70	SL-part	TSOP-II
HY5117404BR	50/60/70		TSOP-II(R)
HY5117404BSLR	50/60/70	SL-part	TSOP-II(R)