Integrated Circuit Systems, Inc.

ICS9123

Preliminary Product Preview

High Resolution Frequency Generator

General Description

The **ICS9123** is a multiple output frequency generator utilizing PLL (Phase-Lock Loop) frequency synthesis. It contains three PLL frequency synthesizers and an internal crystal oscillator reference circuit. Thus, with only an external crystal and the necessary power supply decoupling capacitors, four different output clock frequencies can be provided.

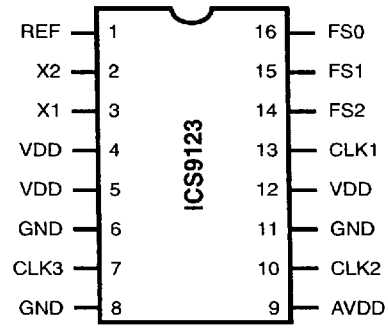
PLL1 of the device has the ability to provide high output frequency resolution (±50 ppm). This makes it suitable for providing clocks for system functions such as modems, eth-ernet, and sound synthesis. PLL2 and PLL3 provide output clocks for other system applications such as microprocessors and DSP chips. For example, in modem applications, the **ICS9123** generates the high resolution clock generator for the A/D converter and two lower resolution clocks for the micro-processor and DSP.

Each of the PLL clock generators has a ROM based frequency selection table which is addressed through device input pins. PLL1 has eight frequency select locations; PLL2 and PLL3 each has four. The ROM based tables are preprogrammed. However, they can be customized for the user specific applications.

Features

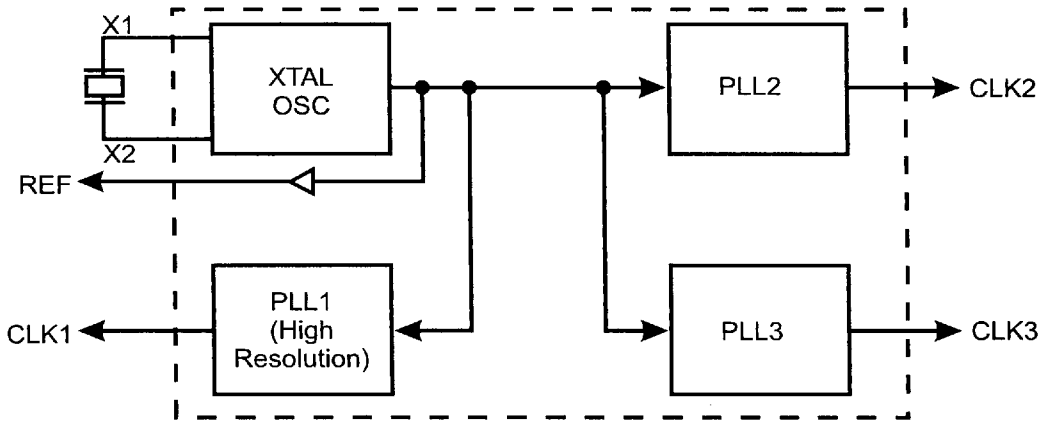
- Cost effective solution for MODEM, ETHERNET and AD1848 applications
- Three independent PLLs
- Four clock frequencies generated from one crystal
- One high resolution PLL provides ±50 ppm accuracy
- Eight ROM based frequency selections for the high resolution PLL1
- Four ROM based frequency selections each for PLL2 and PLL3
- 3.3V or 5V power supply
- On-chip loop filter components
- Low power CMOS technology
- 20- or 16-pin PDIP or SOIC package

Pin Configuration



16-Pin PDIP or SOIC

Block Diagram



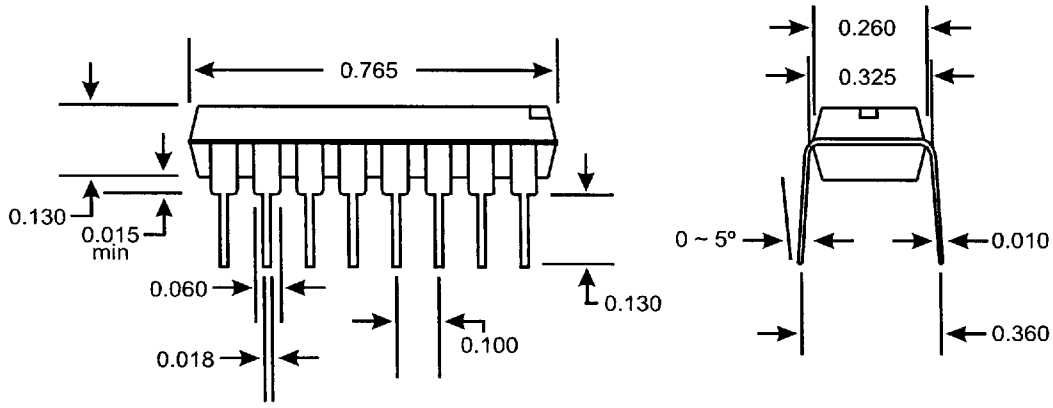
Pin Descriptions for ICS9123

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	REF	OUT	Crystal buffered output.
2	X2	OUT	Connect crystal.
3	X1	OUT	Connect crystal.
4, 5, 12	VDD	PWR	3V or 5V power supply.
6, 8, 11	GND	PWR	Ground.
7	CLK3	OUT	Output frequency one of 3 PLLs.
9	AVDD	PWR	Analog 3V or 5V power supply.
10	CLK2	OUT	Output frequency one of 3 PLLs.
13	CLK1	OUT	Output frequency of the high resolution PLL.
14	FS2	IN	CPU clock frequency. (has pull-up)
15	FS1	IN	CPU clock frequency. (has pull-up)
16	FS0	IN	CPU clock frequency. (has pull-up)

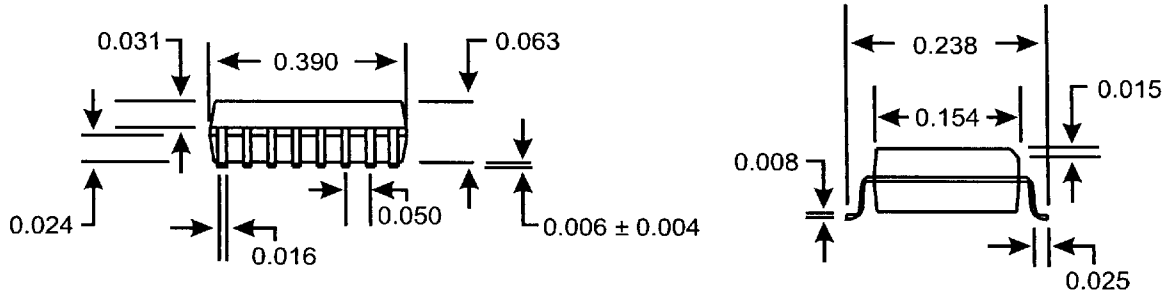
Functionality

(Using 14.318MHz Input Frequency)

FS2	FS1	FS0	CLK1	CLK2	CLK3
0	0	0	8.06400	19.7	29.5
0	0	1	19.66080	29.5	8.06
0	1	0	29.49120	8.06	19.7
0	1	1	11.05920	14.6	16.5
1	0	0	13.82400	19.7	29.5
1	0	1	3.68640	29.5	8.06
1	1	0	14.74560	8.06	19.7
1	1	1	16.00031	14.6	16.5



16-Pin PDIP



16-Pin SOIC

Ordering Information

ICS9123N-01 or ICS9123M-01

Example:

ICS XXXX M-PPP

- **Pattern Number(2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  M=SOIC, N=DIP (Plastic)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS=Standard Device