



No. 1095A

**LC6599**C MOS LSI  
EVALUATION CHIP FOR APPLICATION DEVELOPMENT**General Description**

The LC6599 is an evaluation chip for CMOS single-chip 4-bit microcomputer LC6500 series. (SANYO Original)

The LC6599 is a CPU that contains all the functions (ROM: Connected externally) of the LC6500 series plus the functions, such as break, step functions and built-in RAM capacity control function, required for an evaluation chip. It is used for program debug, hardware simulation when performing the application development of the LC6500 series microcomputers.

**Features of LC6599**

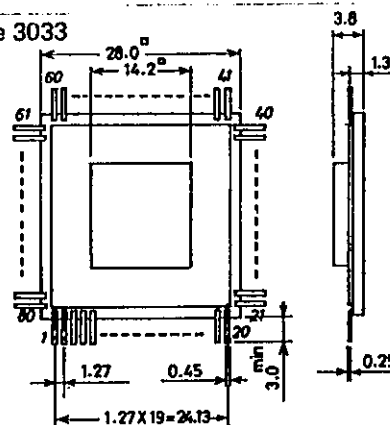
- (1) Capable of performing hardware simulation for all Type Nos. of the LC6500 series.
- (2) Provides the instruction set covering all instructions used by the LC6500 series.
- (3) Program memory of 4096 x 8 bits max. is connectable externally.
- (4) Built-in data RAM capacity can be set as required for the Type No. to be evaluated.
- (5) Abundant evaluation functions
  - Break function to stop execution of program
  - Single-step program execution function
  - Capable of outputting the contents of internal registers (AC, PC, DP) to pins
- (6) Has built-in clock generator (C, R or ceramic resonator: Connected externally)
- (7) +5 V single power supply
- (8) 80-pin flat QIP

**Note:** The LC6599 is designed for application development tool of the LC6500 series microcomputers. It should be noted that it is not suited for use under high-temperature, high-humidity conditions.

**LC6500 series and LC6599**

| Type No. | ROM                      | RAM                        | Package                     | Remarks         |
|----------|--------------------------|----------------------------|-----------------------------|-----------------|
| LC6502C  | 2048 bytes               | 128 x 4 bits               | DIP-42<br>DIP-42S<br>QIP-64 |                 |
| LC6505C  | 1024 bytes               | 64 x 4 bits                | DIP-42<br>DIP-42S<br>QIP-64 |                 |
| LC6599   | External 4096 bytes max. | Built-in 192 x 4 bits max. | QIP-80                      | Evaluation chip |

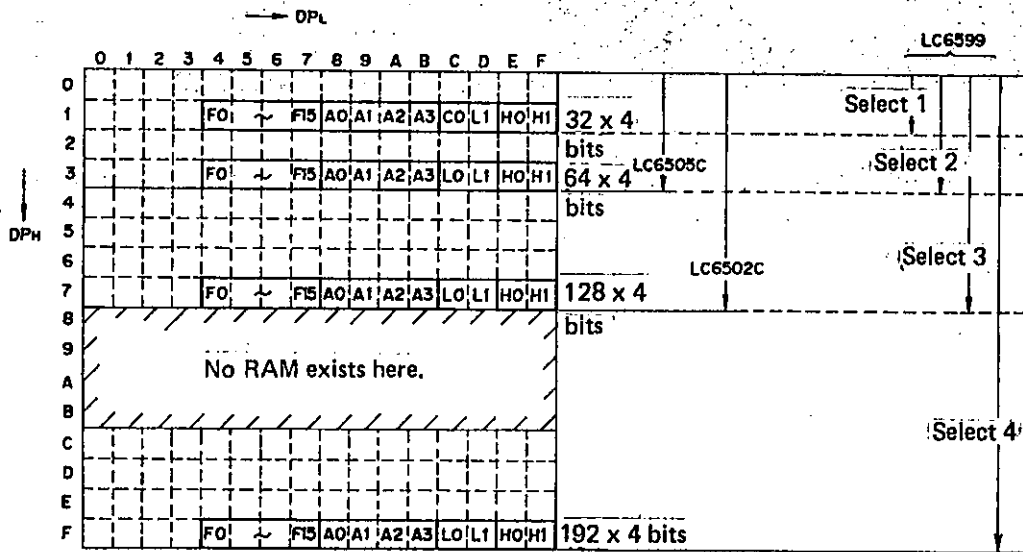
Case Outline 3033  
(unit: mm)



These specifications are subject to change without notice.

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**Built-in RAM capacity control function**



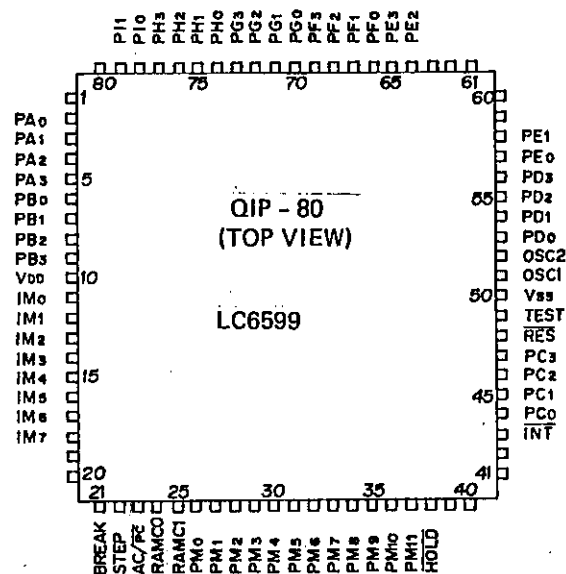
RAM capacity and locations of flags, working registers by Type Nos.

How to set built-in RAM capacity

| RAM Select | RAM Control Pins |       | RAM capacity |
|------------|------------------|-------|--------------|
|            | RAMC1            | RAMC0 |              |
| Select 1   | 1                | 1     | 32 x 4 bits  |
| Select 2   | 1                | 0     | 64 x 4 bits  |
| Select 3   | 0                | 1     | 128 x 4 bits |
| Select 4   | 0                | 0     | 192 x 4 bits |

Note) 0: "L" level input  
1: "H" level input

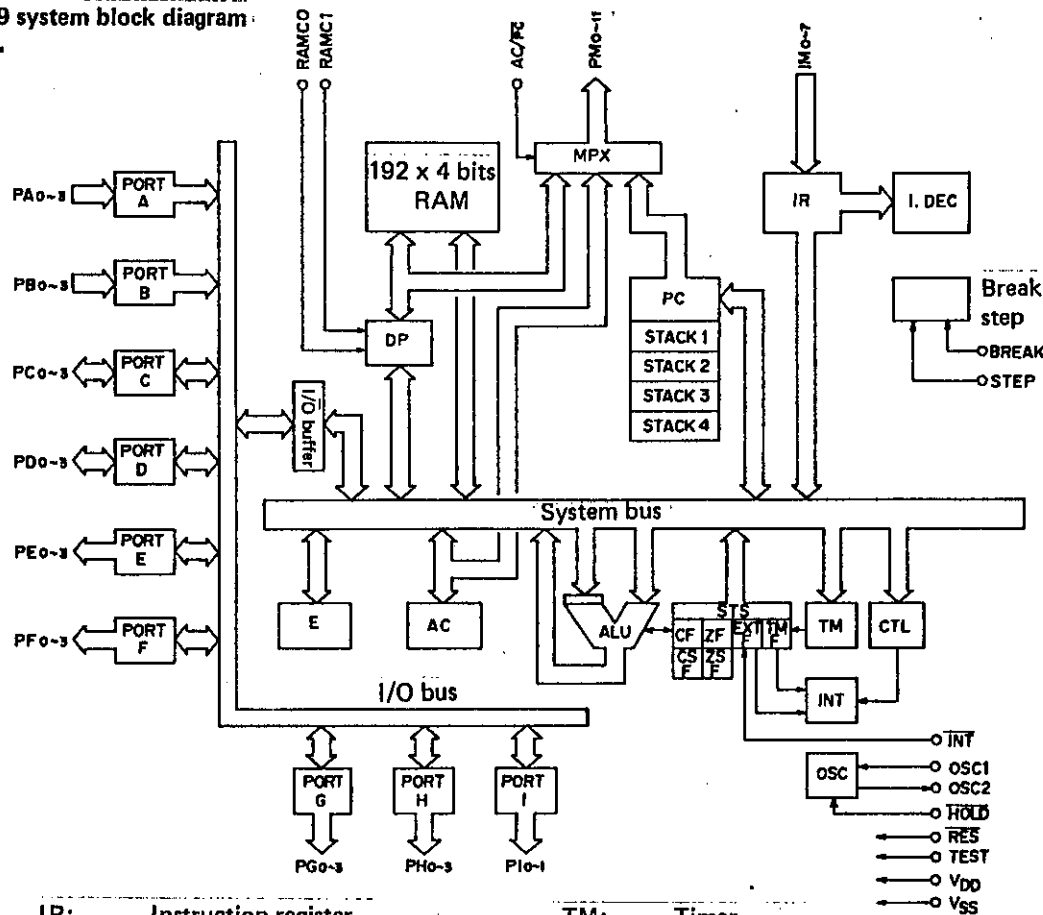
**Pin assignment and functions**



# Pin Description

| Pin name             | Input/output | Functions                                                                                                                                                           |                                                                                    |
|----------------------|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------|
| IM <sub>0</sub> – 7  | Input        | Instruction outputted from external program memory is inputted.                                                                                                     |                                                                                    |
| PM <sub>0</sub> – 11 | Output       | PC contents are outputted during program execution. In break mode, PC contents and AC, DP contents are outputted at AC/ $\overline{PC}$ = "L" and "H" respectively. |                                                                                    |
| AC/ $\overline{PC}$  | Input        | Output contents at PM <sub>0</sub> – 11 are changed-over in break mode.                                                                                             |                                                                                    |
| BREAK                | Input        | Program is executed at "L" level. Break mode occurs at "H" level.                                                                                                   |                                                                                    |
| STEP                 | Input        | Each time "H" level is applied in break mode, program is executed by one step.                                                                                      |                                                                                    |
| RAMC0                | Input        | Built-in RAM capacity/organization are controlled.                                                                                                                  |                                                                                    |
| RAMC1                | Input        |                                                                                                                                                                     |                                                                                    |
| $\overline{INT}$     | Input        | Interrupt request input                                                                                                                                             |                                                                                    |
| $\overline{HOLD}$    | Input        | Hold mode request input                                                                                                                                             |                                                                                    |
| $\overline{RES}$     | Input        | Reset input                                                                                                                                                         |                                                                                    |
| PA <sub>0</sub> – 3  | Input        | Input ports A <sub>0</sub> – 3. Halt mode release input                                                                                                             |                                                                                    |
| PB <sub>0</sub> – 3  | Input        | Input ports B <sub>0</sub> – 3                                                                                                                                      |                                                                                    |
| PC <sub>0</sub> – 3  | Input/output | Input/output common ports C <sub>0</sub> – 3                                                                                                                        |                                                                                    |
| PD <sub>0</sub> – 3  | Input/output | Input/output common ports D <sub>0</sub> – 3                                                                                                                        |                                                                                    |
| PE <sub>0</sub> – 3  | Output       | Output ports E <sub>0</sub> – 3                                                                                                                                     |                                                                                    |
| PF <sub>0</sub> – 3  | Output       | Output ports F <sub>0</sub> – 3                                                                                                                                     |                                                                                    |
| PG <sub>0</sub> – 3  | Output       | Output ports G <sub>0</sub> – 3                                                                                                                                     |                                                                                    |
| PH <sub>0</sub> – 3  | Output       | Output ports H <sub>0</sub> – 3                                                                                                                                     |                                                                                    |
| PI <sub>0</sub> – 1  | Output       | Output ports I <sub>0</sub> – 1                                                                                                                                     |                                                                                    |
| OSC1                 | Input        | External clock is inputted to this pin.                                                                                                                             | Pins for externally connecting ceramic resonator, CR for internal clock generation |
| OSC2                 | Output       |                                                                                                                                                                     |                                                                                    |
| TEST                 | Input        | LC6599 test pin. Normally, connected to V <sub>SS</sub> (0 V)                                                                                                       |                                                                                    |
| V <sub>DD</sub>      | Input        | +5 V                                                                                                                                                                | Power supply pin                                                                   |
| V <sub>SS</sub>      | —            | 0 V                                                                                                                                                                 |                                                                                    |

LC6599 system block diagram



IR: Instruction register  
 I-DEC: Instruction decoder  
 PC: Program counter  
 MPX: PM output multiplexer  
 DP: Data pointer  
 AC: Accumulator  
 ALU: Arithmetic and logic unit

TM: Timer  
 CTL: Control register  
 INT: Interrupt control  
 OSC: Oscillator  
 STS: Status register  
 E: E register

The LC6599 is designed for application development tool of the LC6500 series microcomputers. It should be noted that it is not suited for use under high-temperature, high-humidity conditions. The specifications are subject to change without notice.

#### Absolute Maximum Ratings/ $T_a = 25^\circ\text{C}$ , $V_{SS} = 0\text{ V}$

|                       |           | min  | typ | max          | unit             | Remarks               |
|-----------------------|-----------|------|-----|--------------|------------------|-----------------------|
| Supply voltage        | $V_{DD}$  | -0.3 |     | +7           | V                |                       |
| Input voltage         | $V_{IN}$  | -0.3 |     | $V_{DD}+0.3$ | V                | Note 1                |
| Output voltage        | $V_{OUT}$ | -0.3 |     | $V_{DD}+0.3$ | V                |                       |
| Peak output current   | $I_O$ (1) | -2.0 |     | +2.0         | mA               | Each pin of C-I ports |
|                       | $I_O$ (2) | -26  |     | +26          | mA               | All pins of C-I ports |
|                       | $I_O$ (3) | -0.2 |     | +0.2         | mA               | Each pin of           |
|                       | $I_O$ (4) | -2.4 |     | +2.4         | mA               | PM0 ~ 11              |
|                       |           |      |     |              |                  | All pins of           |
|                       |           |      |     |              |                  | PM0 ~ 11              |
| Power dissipation     | $P_d$ max |      |     | 350          | mW               |                       |
| Operating temperature | $T_{opg}$ | 0    |     | +50          | $^\circ\text{C}$ |                       |
| Storage temperature   | $T_{stg}$ | -55  |     | +125         | $^\circ\text{C}$ |                       |

Note1: For OSC1 pin, up to oscillation amplitude is allowable which appears when causing internal oscillation under the recommended conditions at the recommended circuit in Fig. 3.

| Recommended Operating Conditions/ $T_a = 25^\circ\text{C}$ , $V_{SS} = 0\text{ V}$ |                     |                                                   | min          | typ               | max      | unit          | Remarks                                                                                                            |
|------------------------------------------------------------------------------------|---------------------|---------------------------------------------------|--------------|-------------------|----------|---------------|--------------------------------------------------------------------------------------------------------------------|
| Recommended operating supply voltage                                               | $V_{DD}$ (1)        |                                                   | 4.5          | 5.0               | 5.5      | V             |                                                                                                                    |
| Power-down supply voltage                                                          | $V_{DD}$ (2)        | $\overline{\text{HOLD}} = V_{IL}$ (3)             | 2.0          |                   | 5.5      | V             | At HOLD mode                                                                                                       |
| "H" level input voltage                                                            | $V_{IH}$ (1)        | $V_{DD} = 5\text{ V} \pm 10\%$                    | $0.7V_{DD}$  |                   | $V_{DD}$ | V             | Input pins other than $\overline{\text{INT}}$ , $\overline{\text{RES}}$ , $\overline{\text{HOLD}}$ , OSC1 (Note 2) |
|                                                                                    | $V_{IH}$ (2)        | $V_{DD} = 5\text{ V} \pm 10\%$                    | $0.75V_{DD}$ |                   | $V_{DD}$ | V             | $\overline{\text{INT}}$ , $\overline{\text{RES}}$ , $\overline{\text{HOLD}}$ , OSC1 pins                           |
| "L" level input voltage                                                            | $V_{IL}$ (1)        | $V_{DD} = 5\text{ V} \pm 10\%$                    | $V_{SS}$     | $0.3V_{DD}$       | $V_{DD}$ | V             | Input pins other than $\overline{\text{INT}}$ , $\overline{\text{RES}}$ , $\overline{\text{HOLD}}$ , OSC1 pins     |
|                                                                                    | $V_{IL}$ (2)        | $V_{DD} = 5\text{ V} \pm 10\%$                    | $V_{SS}$     | $0.25V_{DD}$      | $V_{DD}$ | V             | $\overline{\text{INT}}$ , $\overline{\text{RES}}$ , OSC1 pins                                                      |
|                                                                                    | $V_{IL}$ (3)        | $V_{DD} = 2 \sim 5.5\text{ V}$                    | $V_{SS}$     | $0.3V_{DD} - 0.3$ | $V_{DD}$ | V             | $\overline{\text{HOLD}}$ pin                                                                                       |
|                                                                                    | $V_{IL}$ (4)        | $V_{DD} = 5\text{ V} \pm 10\%$                    | $V_{SS}$     | $0.3V_{DD}$       | $V_{DD}$ | V             | TEST pin                                                                                                           |
| Operating clock frequency                                                          | $f_{\text{extosc}}$ | For external clock $V_{DD} = 5\text{ V} \pm 10\%$ | 20           |                   | 420      | kHz           | Input at OSC1 pin Refer to Fig. 1                                                                                  |
| "H" level clock pulse width                                                        | $t_{w\phi H}$       | do.                                               | 0.5          |                   |          | $\mu\text{s}$ | do.                                                                                                                |
| "L" level clock pulse width                                                        | $t_{w\phi L}$       | do.                                               | 0.5          |                   |          | $\mu\text{s}$ | do.                                                                                                                |
| Clock input rise time                                                              | $t_{\text{oscR}}$   | do.                                               |              |                   | 0.2      | $\mu\text{s}$ | do.                                                                                                                |
| Clock input fall time                                                              | $t_{\text{oscF}}$   | do.                                               |              |                   | 0.2      | $\mu\text{s}$ | do.                                                                                                                |
| External capacitor value for CR oscillation                                        | $C_{\text{ext}}$    |                                                   |              | $33 \pm 5\%$      |          | pF            | Refer to Fig. 2                                                                                                    |
| External resistance value for CR oscillation                                       | $R_{\text{ext}}$    |                                                   |              | $100 \pm 1\%$     |          | k $\Omega$    |                                                                                                                    |
| External capacitance value for ceramic oscillation                                 | C1                  | CSB400P                                           |              | $33 \pm 10\%$     |          | pF            | Refer to Fig. 3.                                                                                                   |
|                                                                                    |                     | KBR400B                                           |              | $33 \pm 10\%$     |          | pF            |                                                                                                                    |
|                                                                                    | C2                  | CSB400P                                           |              | $33 \pm 10\%$     |          | pF            |                                                                                                                    |
|                                                                                    |                     | KBR400B                                           |              | $33 \pm 10\%$     |          | pF            |                                                                                                                    |
| External resistance value for ceramic oscillation                                  | R1                  |                                                   |              | $4700 \pm 5\%$    |          | k $\Omega$    |                                                                                                                    |
|                                                                                    | R2                  |                                                   |              | $3.9 \pm 5\%$     |          | k $\Omega$    |                                                                                                                    |
| Power-down $\overline{\text{HOLD}}$ setup time                                     | $t_{\text{HOLD S}}$ |                                                   | 2            |                   |          | ms            | Refer to Fig. 6.                                                                                                   |
| Power-down $\overline{\text{HOLD}}$ hold time                                      | $t_{\text{HOLD H}}$ |                                                   | 2            |                   |          | ms            |                                                                                                                    |

Note 2: TEST pin is for LSI test only. It is not included in "input pin" unless otherwise specified.

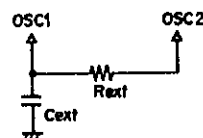


Fig. 2 Recommended oscillator circuit for CR oscillation

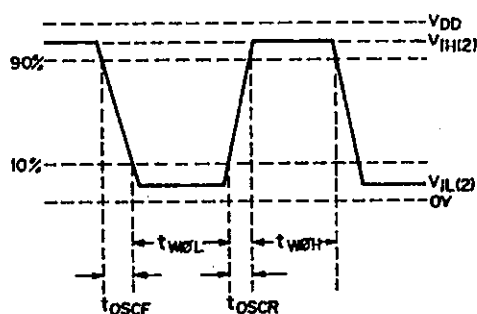


Fig. 1 Input waveform at OSC1 pin

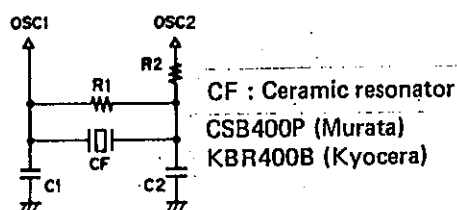
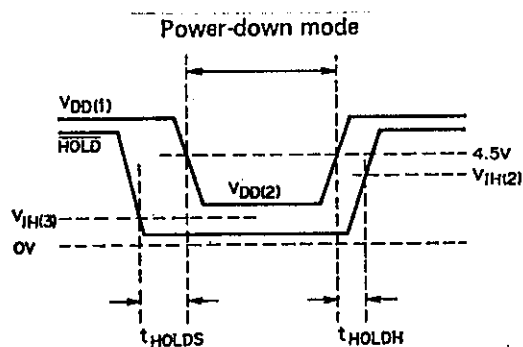


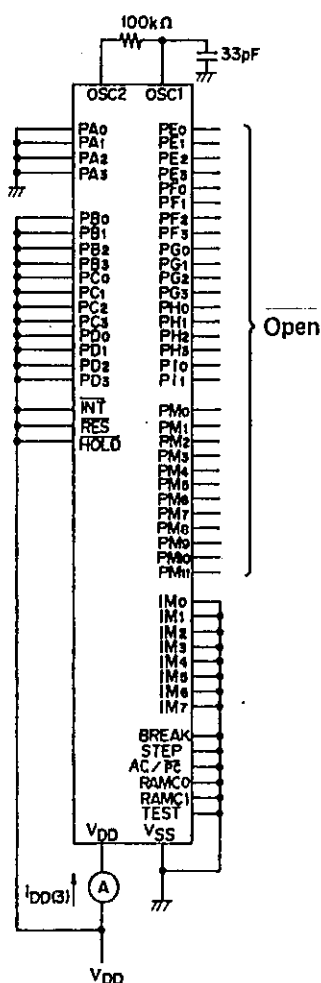
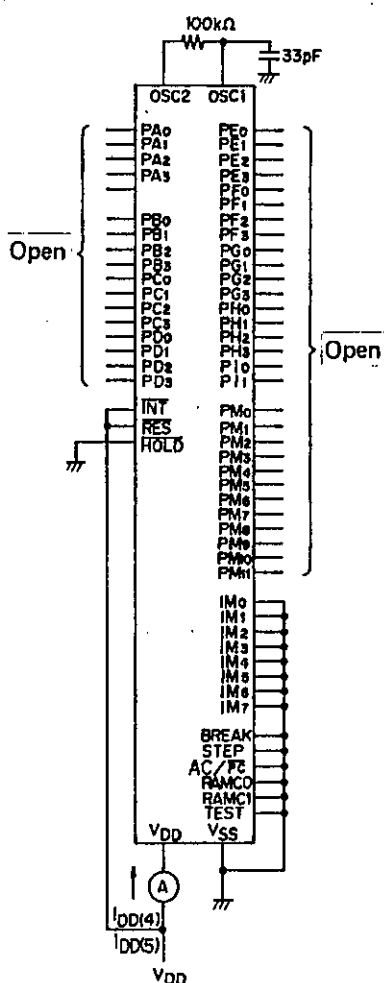
Fig. 3 Recommended oscillator circuit for ceramic oscillation

CF : Ceramic resonator  
CSB400P (Murata)  
KBR400B (Kyocera)

| Electrical Characteristics/ $T_a = 25^{\circ}\text{C}$ , $V_{DD} = 5\text{ V} \pm 10\%$ , $V_{SS} = 0\text{ V}$ |               |                                                                                                                 |                |     |     |   | min           | typ                                         | max | unit | Remarks        |
|-----------------------------------------------------------------------------------------------------------------|---------------|-----------------------------------------------------------------------------------------------------------------|----------------|-----|-----|---|---------------|---------------------------------------------|-----|------|----------------|
| "H" level input current                                                                                         | $I_{IH}$      | $V_{IN} = V_{DD}$                                                                                               |                |     |     | 1 | $\mu\text{A}$ | All input pins                              |     |      | each input pin |
| "L" level input current                                                                                         | $I_{IL}$      | $V_{IN} = V_{SS}$                                                                                               | -1             |     |     |   | $\mu\text{A}$ |                                             |     |      |                |
| "H" level output voltage                                                                                        | $V_{OH} (1)$  | $I_{OH} = -1\text{ mA}$                                                                                         | $V_{DD} - 2$   |     |     |   | V             | Output pins other than OSC2, PM0 to PM11    |     |      |                |
|                                                                                                                 | $V_{OH} (2)$  | $I_{OH} = -100\text{ }\mu\text{A}$                                                                              | $V_{DD} - 0.5$ |     |     |   | V             | Output pins other than OSC2, PM0 to PM11    |     |      |                |
|                                                                                                                 | $V_{OH} (3)$  | $I_{OH} = -100\text{ }\mu\text{A}$                                                                              | $V_{DD} - 2$   |     |     |   | V             | PM0 to PM11 pins                            |     |      |                |
| "L" level output voltage                                                                                        | $V_{OL} (1)$  | $I_{OL} = 1\text{ mA}$                                                                                          |                |     | 0.4 |   | V             | Output pins other than OSC2, PM0 to PM11    |     |      |                |
|                                                                                                                 | $V_{OL} (2)$  | $I_{OL} = 100\text{ }\mu\text{A}$                                                                               |                |     | 0.4 |   | V             | PM0 to PM11 pins                            |     |      |                |
| Output off leak current                                                                                         | $I_{OFF} (1)$ | $V_{OUT} = V_{DD}$                                                                                              |                |     | 1   |   | $\mu\text{A}$ | Output pins other than OSC2, PM0 to PM11    |     |      |                |
|                                                                                                                 | $I_{OFF} (2)$ | $V_{OUT} = V_{SS}$                                                                                              | -1             |     |     |   | $\mu\text{A}$ | Output pins other than OSC2, PM0 to PM11    |     |      |                |
| Clock oscillation frequency for ceramic oscillation                                                             | $f_{XOSC}$    | Recommended conditions for ceramic oscillation                                                                  | 384            | 400 | 417 |   | kHz           | Oscillator in Fig. 3                        |     |      |                |
| Clock oscillation frequency for CR oscillation                                                                  | $f_{CROSC}$   | $C_{ext} = 33\text{ pF} \pm 5\%$<br>$R_{ext} = 100\text{ k}\Omega \pm 1\%$                                      | 230            | 300 | 390 |   | kHz           | Oscillator in Fig. 2                        |     |      |                |
| Current dissipation                                                                                             | $I_{DD} (1)$  | $C_{ext} = 33\text{ pF}$<br>$R_{ext} = 100\text{ k}\Omega$<br>Output pin open<br>Input pin<br>$V_{IN} = V_{DD}$ |                | 0.4 | 1.0 |   | mA            | At CR oscillation                           |     |      |                |
|                                                                                                                 | $I_{DD} (2)$  | Recommended condition for ceramic oscillation<br>Output pin open<br>Input pin<br>$V_{IN} = V_{DD}$              |                | 0.5 | 1.0 |   | mA            | At ceramic oscillation                      |     |      |                |
|                                                                                                                 | $I_{DD} (3)$  | $V_{DD} = 5\text{ V} \pm 10\%$<br>Test circuit in Fig. 4                                                        |                | 0.5 | 10  |   | $\mu\text{A}$ | At halt mode<br>Refer to Fig. 4.            |     |      |                |
|                                                                                                                 | $I_{DD} (4)$  | $V_{DD} = 5\text{ V} \pm 10\%$<br>Test circuit in Fig. 5                                                        |                | 0.5 | 10  |   | $\mu\text{A}$ | At hold mode<br>Refer to Fig. 5.            |     |      |                |
|                                                                                                                 | $I_{DD} (5)$  | $V_{DD} = 2\text{ V}$<br>Test circuit in Fig. 5                                                                 |                | 0.1 | 2   |   | $\mu\text{A}$ | Hold mode<br>Power-down<br>Refer to Fig. 5. |     |      |                |
| Input capacitance                                                                                               | $C_{IN}$      | $f = 200\text{ kHz}$                                                                                            |                | 5   |     |   | pF            | Other than IM0 to IM7, PM0 to PM11 pins     |     |      |                |
| Output capacitance                                                                                              | $C_{OUT}$     | $f = 200\text{ kHz}$<br>Output high impedance                                                                   |                | 10  |     |   | pF            | Other than IM0 to IM7, PM0 to PM11 pins     |     |      |                |
| Input/output capacitance                                                                                        | $C_{IO}$      | $f = 200\text{ kHz}$<br>Output high impedance                                                                   |                | 10  |     |   | pF            |                                             |     |      |                |



### Fig. 6 Power-down mode timing

Fig. 4  $I_{DD}$  (3) test circuit :Fig. 5  $I_{DD}$  (4),  $I_{DD}$  (5) test circuit

Input/output common ports C, D : Output inhibit  
HALT instruction is executed and HALT mode is entered.

#### Application Development Tools

- SDS-410 System

This consists of a CPU with two floppy disk units provided, a CRT, and a printer, and makes it possible to speedily and efficiently prepare the application development program of a microcomputer in assembly language.

- EVA-410

This is an evaluation kit having the EPROM writer function and parallel/serial data communication function that transfers data to and from external equipment (SDS-410, etc.), and makes it possible to correct and debug the application development program on machine language level.

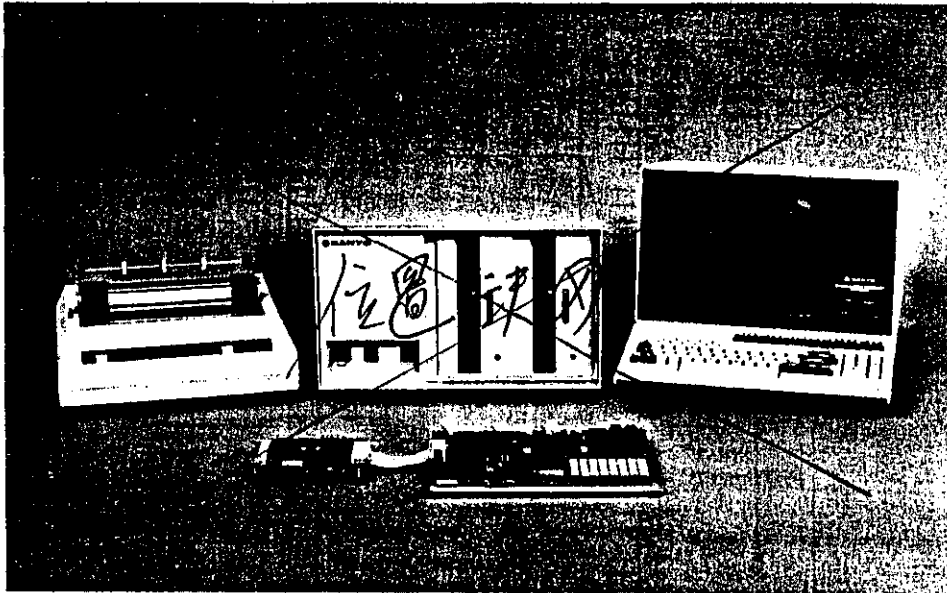
By replacing the target board, the EVA-410 can be also used for the application development of the N channel microcomputer LM6400 series.

- EVA-402

This consists of an EPROM and the LC6599 mounted on a board, and is used for checking the operation of a set or making a set by way of trial when the application development program is finished.

- LC65PG99

This is a simulation chip having a 24-pin socket for EPROM on the package surface. The package is DIP-42 which is pin compatible with the LC6502C/LC6505C. By mounting this chip on the user's application equipment, mounting evaluation can be performed easily. (Under development)



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## APPENDIX I LC6500 SERIES INSTRUCTION SET (BY FUNCTIONS)

## Notations

AC : Accumulator  
 ACt : Accumulator bit t  
 CF : Carry flag  
 CTL : Control register  
 DP : Data pointer  
 E : E register  
 EXTf : External interrupt request flag  
 Fn : Flag bit n  
 M : Memory

M(DP) : Memory addressed by DP  
 P(DP<sub>L</sub>) : Input/output port addressed by DP<sub>L</sub>  
 PC : Program counter  
 STACK : Stack register  
 TM : Timer  
 TMf : Timer (internal) interrupt request flag  
 At, Ha, La : Working register  
 ZF : Zero flag

( I, I ) : Contents  
 ← : Transfer and direction  
 + : Addition  
 - : Subtraction  
 ∧ : AND  
 ∨ : Exclusive OR

| Instruction                                  | Mnemonic                                    |                                                                     | Instruction code                                            |                                                             |   |                                    | Bytes                                                                                                                                                                                                                                                                                                                                                              | Cycles                                                                                                                                                                                                                                                                                                                             | Function          | Description                                                                                                          | Status flag affected | Remarks        |   |                      |                |   |                      |                |   |       |       |
|----------------------------------------------|---------------------------------------------|---------------------------------------------------------------------|-------------------------------------------------------------|-------------------------------------------------------------|---|------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|----------------------------------------------------------------------------------------------------------------------|----------------------|----------------|---|----------------------|----------------|---|----------------------|----------------|---|-------|-------|
|                                              |                                             |                                                                     | D <sub>7</sub> D <sub>6</sub> D <sub>5</sub> D <sub>4</sub> | D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub> |   |                                    |                                                                                                                                                                                                                                                                                                                                                                    |                                                                                                                                                                                                                                                                                                                                    |                   |                                                                                                                      |                      |                |   |                      |                |   |                      |                |   |       |       |
| Accumulator manipulation instructions        | CLA                                         | Clear AC                                                            | 1 1 0 0                                                     | 0 0 0 0                                                     | 1 | 1                                  | AC ← 0                                                                                                                                                                                                                                                                                                                                                             | The AC contents are cleared.                                                                                                                                                                                                                                                                                                       | ZF                | * 1                                                                                                                  |                      |                |   |                      |                |   |                      |                |   |       |       |
|                                              | CLC                                         | Clear CF                                                            | 1 1 1 0                                                     | 0 0 0 1                                                     | 1 | 1                                  | CF ← 0                                                                                                                                                                                                                                                                                                                                                             | The CF contents are cleared.                                                                                                                                                                                                                                                                                                       | CF                |                                                                                                                      |                      |                |   |                      |                |   |                      |                |   |       |       |
|                                              | STC                                         | Set CF                                                              | 1 1 1 1                                                     | 0 0 0 1                                                     | 1 | 1                                  | CF ← 1                                                                                                                                                                                                                                                                                                                                                             | The CF is set.                                                                                                                                                                                                                                                                                                                     | CF                |                                                                                                                      |                      |                |   |                      |                |   |                      |                |   |       |       |
|                                              | CMA                                         | Complement AC                                                       | 1 1 1 0                                                     | 1 0 1 1                                                     | 1 | 1                                  | AC ← (AC)                                                                                                                                                                                                                                                                                                                                                          | The AC contents are complemented.                                                                                                                                                                                                                                                                                                  | ZF                |                                                                                                                      |                      |                |   |                      |                |   |                      |                |   |       |       |
|                                              | INC                                         | Increment AC                                                        | 0 0 0 0                                                     | 1 1 1 0                                                     | 1 | 1                                  | AC ← (AC) + 1                                                                                                                                                                                                                                                                                                                                                      | The AC contents are incremented +1.                                                                                                                                                                                                                                                                                                | ZF CF             |                                                                                                                      |                      |                |   |                      |                |   |                      |                |   |       |       |
|                                              | DEC                                         | Decrement AC                                                        | 0 0 0 0                                                     | 1 1 1 1                                                     | 1 | 1                                  | AC ← (AC) - 1                                                                                                                                                                                                                                                                                                                                                      | The AC contents are decremented -1.                                                                                                                                                                                                                                                                                                | ZF CF             |                                                                                                                      |                      |                |   |                      |                |   |                      |                |   |       |       |
|                                              | RAL                                         | Rotate AC left through CF                                           | 0 0 0 0                                                     | 0 0 0 1                                                     | 1 | 1                                  | AC <sub>0</sub> ← (CF), AC <sub>n+1</sub> ← (AC) <sub>n</sub> , CF ← (AC) <sub>3</sub>                                                                                                                                                                                                                                                                             | The AC contents are shifted left through the CF.                                                                                                                                                                                                                                                                                   | ZF CF             |                                                                                                                      |                      |                |   |                      |                |   |                      |                |   |       |       |
|                                              | TAE                                         | Transfer AC to E                                                    | 0 0 0 0                                                     | 0 0 1 1                                                     | 1 | 1                                  | E ← (AC)                                                                                                                                                                                                                                                                                                                                                           | The AC contents are transferred to the E.                                                                                                                                                                                                                                                                                          |                   |                                                                                                                      |                      |                |   |                      |                |   |                      |                |   |       |       |
|                                              | XAE                                         | Exchange AC with E                                                  | 0 0 0 0                                                     | 1 1 0 1                                                     | 1 | 1                                  | (AC) ↔ (E)                                                                                                                                                                                                                                                                                                                                                         | The AC contents and the E contents are exchanged.                                                                                                                                                                                                                                                                                  |                   |                                                                                                                      |                      |                |   |                      |                |   |                      |                |   |       |       |
| Memory manipulation instructions             | INM                                         | Increment M                                                         | 0 0 1 0                                                     | 1 1 1 0                                                     | 1 | 1                                  | M(DP) ← (M(DP)) + 1                                                                                                                                                                                                                                                                                                                                                | The M(DP) contents are incremented +1.                                                                                                                                                                                                                                                                                             | ZF CF             |                                                                                                                      |                      |                |   |                      |                |   |                      |                |   |       |       |
|                                              | DEM                                         | Decrement M                                                         | 0 0 1 0                                                     | 1 1 1 1                                                     | 1 | 1                                  | M(DP) ← (M(DP)) - 1                                                                                                                                                                                                                                                                                                                                                | The M(DP) contents are decremented -1.                                                                                                                                                                                                                                                                                             | ZF CF             |                                                                                                                      |                      |                |   |                      |                |   |                      |                |   |       |       |
|                                              | SMB bit                                     | Set M data bit                                                      | 0 0 0 0                                                     | 1 0 B <sub>1</sub> B <sub>0</sub>                           | 1 | 1                                  | M(DP, B <sub>1</sub> B <sub>0</sub> ) ← 1                                                                                                                                                                                                                                                                                                                          | A single bit of the M(DP) specified with B <sub>1</sub> B <sub>0</sub> is set.                                                                                                                                                                                                                                                     |                   |                                                                                                                      |                      |                |   |                      |                |   |                      |                |   |       |       |
|                                              | RMB bit                                     | Reset M data bit                                                    | 0 0 1 0                                                     | 1 0 B <sub>1</sub> B <sub>0</sub>                           | 1 | 1                                  | M(DP, B <sub>1</sub> B <sub>0</sub> ) ← 0                                                                                                                                                                                                                                                                                                                          | A single bit of the M(DP) specified with B <sub>1</sub> B <sub>0</sub> is reset.                                                                                                                                                                                                                                                   | ZF                |                                                                                                                      |                      |                |   |                      |                |   |                      |                |   |       |       |
| Arithmetic operation/comparison instructions | AD                                          | Add M to AC                                                         | 0 1 1 0                                                     | 0 0 0 0                                                     | 1 | 1                                  | AC ← (AC) + (M(DP))                                                                                                                                                                                                                                                                                                                                                | Binary addition of the AC contents and the M(DP) contents is performed and the result is stored in the AC.                                                                                                                                                                                                                         | ZF CF             |                                                                                                                      |                      |                |   |                      |                |   |                      |                |   |       |       |
|                                              | ADC                                         | Add M to AC with CF                                                 | 0 0 1 0                                                     | 0 0 0 0                                                     | 1 | 1                                  | AC ← (AC) + (M(DP)) + (CF)                                                                                                                                                                                                                                                                                                                                         | Binary addition of the AC, CF contents and the M(DP) contents is performed and the result is stored in the AC.                                                                                                                                                                                                                     | ZF CF             |                                                                                                                      |                      |                |   |                      |                |   |                      |                |   |       |       |
|                                              | DAA                                         | Decimal adjust AC in addition                                       | 1 1 1 0                                                     | 0 1 1 0                                                     | 1 | 1                                  | AC ← (AC) + 6                                                                                                                                                                                                                                                                                                                                                      | 6 is added to the AC contents.                                                                                                                                                                                                                                                                                                     | ZF                |                                                                                                                      |                      |                |   |                      |                |   |                      |                |   |       |       |
|                                              | DAS                                         | Decimal adjust AC in subtraction                                    | 1 1 1 0                                                     | 1 0 1 0                                                     | 1 | 1                                  | AC ← (AC) + 10                                                                                                                                                                                                                                                                                                                                                     | 10 is added to the AC contents.                                                                                                                                                                                                                                                                                                    | ZF                |                                                                                                                      |                      |                |   |                      |                |   |                      |                |   |       |       |
|                                              | EXL                                         | Exclusive or M to AC                                                | 1 1 1 1                                                     | 0 1 0 1                                                     | 1 | 1                                  | AC ← (AC) ∨ (M(DP))                                                                                                                                                                                                                                                                                                                                                | The AC contents and the M(DP) contents are exclusive-ORed and the result is stored in the AC.                                                                                                                                                                                                                                      | ZF                |                                                                                                                      |                      |                |   |                      |                |   |                      |                |   |       |       |
|                                              | AND                                         | And M to AC                                                         | 1 1 1 0                                                     | 0 1 1 1                                                     | 1 | 1                                  | AC ← (AC) ∧ (M(DP))                                                                                                                                                                                                                                                                                                                                                | The AC contents and the M(DP) contents are ANDed and the result is stored in the AC.                                                                                                                                                                                                                                               | ZF                |                                                                                                                      |                      |                |   |                      |                |   |                      |                |   |       |       |
|                                              | OR                                          | Or M to AC                                                          | 1 1 1 0                                                     | 0 1 0 1                                                     | 1 | 1                                  | AC ← (AC) ∨ (M(DP))                                                                                                                                                                                                                                                                                                                                                | The AC contents and the M(DP) contents are ORed and the result is stored in the AC.                                                                                                                                                                                                                                                | ZF                |                                                                                                                      |                      |                |   |                      |                |   |                      |                |   |       |       |
|                                              | CM                                          | Compare AC with M                                                   | 1 1 1 1                                                     | 1 0 1 1                                                     | 1 | 1                                  | (M(DP)) + (AC) + 1                                                                                                                                                                                                                                                                                                                                                 | The AC contents and the M(DP) contents are compared and the CF and ZF are set/reset.<br><table><tr><td>Comparison result</td><td>CF</td><td>ZF</td></tr><tr><td>(M(DP)) &gt; (AC)</td><td>0</td><td>0</td></tr><tr><td>(M(DP)) = (AC)</td><td>1</td><td>1</td></tr><tr><td>(M(DP)) &lt; (AC)</td><td>1</td><td>0</td></tr></table> | Comparison result | CF                                                                                                                   | ZF                   | (M(DP)) > (AC) | 0 | 0                    | (M(DP)) = (AC) | 1 | 1                    | (M(DP)) < (AC) | 1 | 0     | ZF CF |
| Comparison result                            | CF                                          | ZF                                                                  |                                                             |                                                             |   |                                    |                                                                                                                                                                                                                                                                                                                                                                    |                                                                                                                                                                                                                                                                                                                                    |                   |                                                                                                                      |                      |                |   |                      |                |   |                      |                |   |       |       |
| (M(DP)) > (AC)                               | 0                                           | 0                                                                   |                                                             |                                                             |   |                                    |                                                                                                                                                                                                                                                                                                                                                                    |                                                                                                                                                                                                                                                                                                                                    |                   |                                                                                                                      |                      |                |   |                      |                |   |                      |                |   |       |       |
| (M(DP)) = (AC)                               | 1                                           | 1                                                                   |                                                             |                                                             |   |                                    |                                                                                                                                                                                                                                                                                                                                                                    |                                                                                                                                                                                                                                                                                                                                    |                   |                                                                                                                      |                      |                |   |                      |                |   |                      |                |   |       |       |
| (M(DP)) < (AC)                               | 1                                           | 0                                                                   |                                                             |                                                             |   |                                    |                                                                                                                                                                                                                                                                                                                                                                    |                                                                                                                                                                                                                                                                                                                                    |                   |                                                                                                                      |                      |                |   |                      |                |   |                      |                |   |       |       |
| CI data                                      | Compare AC with immediate data              | 0 0 1 0<br>0 1 0 0                                                  | 1 1 0 0<br>1 3 1 2 1 1 0                                    | 2                                                           | 2 | 1 3 1 2 1 1 0 + (AC) + 1           | The AC contents and the immediate data 1 3 1 2 1 1 0 are compared and the ZF and CF are set/reset.<br><table><tr><td>Comparison result</td><td>CF</td><td>ZF</td></tr><tr><td>1 3 1 2 1 1 0 &gt; (AC)</td><td>0</td><td>0</td></tr><tr><td>1 3 1 2 1 1 0 = (AC)</td><td>1</td><td>1</td></tr><tr><td>1 3 1 2 1 1 0 &lt; (AC)</td><td>1</td><td>0</td></tr></table> | Comparison result                                                                                                                                                                                                                                                                                                                  | CF                | ZF                                                                                                                   | 1 3 1 2 1 1 0 > (AC) | 0              | 0 | 1 3 1 2 1 1 0 = (AC) | 1              | 1 | 1 3 1 2 1 1 0 < (AC) | 1              | 0 | ZF CF |       |
| Comparison result                            | CF                                          | ZF                                                                  |                                                             |                                                             |   |                                    |                                                                                                                                                                                                                                                                                                                                                                    |                                                                                                                                                                                                                                                                                                                                    |                   |                                                                                                                      |                      |                |   |                      |                |   |                      |                |   |       |       |
| 1 3 1 2 1 1 0 > (AC)                         | 0                                           | 0                                                                   |                                                             |                                                             |   |                                    |                                                                                                                                                                                                                                                                                                                                                                    |                                                                                                                                                                                                                                                                                                                                    |                   |                                                                                                                      |                      |                |   |                      |                |   |                      |                |   |       |       |
| 1 3 1 2 1 1 0 = (AC)                         | 1                                           | 1                                                                   |                                                             |                                                             |   |                                    |                                                                                                                                                                                                                                                                                                                                                                    |                                                                                                                                                                                                                                                                                                                                    |                   |                                                                                                                      |                      |                |   |                      |                |   |                      |                |   |       |       |
| 1 3 1 2 1 1 0 < (AC)                         | 1                                           | 0                                                                   |                                                             |                                                             |   |                                    |                                                                                                                                                                                                                                                                                                                                                                    |                                                                                                                                                                                                                                                                                                                                    |                   |                                                                                                                      |                      |                |   |                      |                |   |                      |                |   |       |       |
| CLI data                                     | Compare DP <sub>L</sub> with immediate data | 0 0 1 0<br>0 1 0 1                                                  | 1 1 0 0<br>1 3 1 2 1 1 0                                    | 2                                                           | 2 | (DP <sub>L</sub> ) ∨ 1 3 1 2 1 1 0 | The DP <sub>L</sub> contents and the immediate data 1 3 1 2 1 1 0 are compared.                                                                                                                                                                                                                                                                                    | ZF                                                                                                                                                                                                                                                                                                                                 |                   |                                                                                                                      |                      |                |   |                      |                |   |                      |                |   |       |       |
| Load/store instructions                      | LI data                                     | Load AC with immediate data                                         | 1 1 0 0                                                     | 1 3 1 2 1 1 0                                               | 1 | 1                                  | AC ← 1 3 1 2 1 1 0                                                                                                                                                                                                                                                                                                                                                 | The immediate data 1 3 1 2 1 1 0 is loaded in the AC.                                                                                                                                                                                                                                                                              | ZF                | * 1                                                                                                                  |                      |                |   |                      |                |   |                      |                |   |       |       |
|                                              | S                                           | Store AC to M                                                       | 0 0 0 0                                                     | 0 0 1 0                                                     | 1 | 1                                  | M(DP) ← (AC)                                                                                                                                                                                                                                                                                                                                                       | The AC contents are stored in the M(DP).                                                                                                                                                                                                                                                                                           |                   |                                                                                                                      |                      |                |   |                      |                |   |                      |                |   |       |       |
|                                              | L                                           | Load AC from M                                                      | 0 0 1 0                                                     | 0 0 0 1                                                     | 1 | 1                                  | AC ← (M(DP))                                                                                                                                                                                                                                                                                                                                                       | The M(DP) contents are loaded in the AC.                                                                                                                                                                                                                                                                                           | ZF                |                                                                                                                      |                      |                |   |                      |                |   |                      |                |   |       |       |
|                                              | XM data                                     | Exchange AC with M, then modify DP <sub>n</sub> with immediate data | 1 0 1 0                                                     | 0 M <sub>2</sub> M <sub>1</sub> M <sub>0</sub>              | 1 | 2                                  | (AC) ↔ (M(DP))<br>DP <sub>n</sub> ← (DP <sub>n</sub> ) ∨ 0 M <sub>2</sub> M <sub>1</sub> M <sub>0</sub>                                                                                                                                                                                                                                                            | The AC contents and the M(DP) contents are exchanged and then the DP <sub>n</sub> contents are modified with the contents of (DP <sub>n</sub> ) ∨ 0 M <sub>2</sub> M <sub>1</sub> M <sub>0</sub> .                                                                                                                                 | ZF                | The ZF is set/reset according to the result of (DP <sub>n</sub> ) ∨ 0 M <sub>2</sub> M <sub>1</sub> M <sub>0</sub> . |                      |                |   |                      |                |   |                      |                |   |       |       |
|                                              | X                                           | Exchange AC with M                                                  | 1 0 1 0                                                     | 0 0 0 0                                                     | 1 | 2                                  | (AC) ↔ (M(DP))                                                                                                                                                                                                                                                                                                                                                     | The AC contents and the M(DP) contents are exchanged.                                                                                                                                                                                                                                                                              | ZF                | The ZF is set/reset according to the DP <sub>n</sub> contents at the time of instruction execution.                  |                      |                |   |                      |                |   |                      |                |   |       |       |
|                                              | XI                                          | Exchange AC with M, then increment DP <sub>L</sub>                  | 1 1 1 1                                                     | 1 1 1 0                                                     | 1 | 2                                  | (AC) ↔ (M(DP))<br>DP <sub>L</sub> ← (DP <sub>L</sub> ) + 1                                                                                                                                                                                                                                                                                                         | The AC contents and the M(DP) contents are exchanged and then the DP <sub>L</sub> contents are incremented +1.                                                                                                                                                                                                                     | ZF                | The ZF is set/reset according to the result of (DP <sub>L</sub> ) + 1.                                               |                      |                |   |                      |                |   |                      |                |   |       |       |
|                                              | XD                                          | Exchange AC with M, then decrement DP <sub>L</sub>                  | 1 1 1 1                                                     | 1 1 1 1                                                     | 1 | 2                                  | (AC) ↔ (M(DP))<br>DP <sub>L</sub> ← (DP <sub>L</sub> ) - 1                                                                                                                                                                                                                                                                                                         | The AC contents and the M(DP) contents are exchanged and then the DP <sub>L</sub> contents are decremented -1.                                                                                                                                                                                                                     | ZF                | The ZF is set/reset according to the result of (DP <sub>L</sub> ) - 1.                                               |                      |                |   |                      |                |   |                      |                |   |       |       |
|                                              | RTBL                                        | Read table data from program ROM                                    | 0 1 1 0                                                     | 0 0 1 1                                                     | 1 | 2                                  | AC ← ROM (PCh, E, AC)                                                                                                                                                                                                                                                                                                                                              | The contents of ROM addressed by the PC whose low-order 8 bits are replaced with the E and AC contents are loaded in the AC and E.                                                                                                                                                                                                 |                   |                                                                                                                      |                      |                |   |                      |                |   |                      |                |   |       |       |

| Instruction                                | Mnemonic  |                                                             | Instruction code                                                       |                                                                                                                | Bytes | Cycles | Function                                                                                                                                                                                                                  | Description                                                                                                                                                                                                                                                                                                         | Status flag affected | Remarks                                                                                                                                                                                                                                                                                                                                                     |
|--------------------------------------------|-----------|-------------------------------------------------------------|------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------|-------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                            |           |                                                             | D <sub>7</sub> D <sub>6</sub> D <sub>5</sub> D <sub>4</sub>            | D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub>                                                    |       |        |                                                                                                                                                                                                                           |                                                                                                                                                                                                                                                                                                                     |                      |                                                                                                                                                                                                                                                                                                                                                             |
| Data pointer manipulation instructions     | L0Z data  | Load DPH with Zero and DPL with immediate data respectively | 1 0 0 0                                                                | 13 12 11 10                                                                                                    | 1     | 1      | DPH ← 0<br>DPL ← 13 12 11 10                                                                                                                                                                                              | The DPH and DPL are loaded with 0 and the immediate data 13 12 11 10 respectively.                                                                                                                                                                                                                                  |                      |                                                                                                                                                                                                                                                                                                                                                             |
|                                            | LHI data  | Load DPH with immediate data                                | 0 1 0 0                                                                | 13 12 11 10                                                                                                    | 1     | 1      | DPH ← 13 12 11 10                                                                                                                                                                                                         | The DPH is loaded with the immediate data 13 12 11 10.                                                                                                                                                                                                                                                              |                      |                                                                                                                                                                                                                                                                                                                                                             |
|                                            | IND       | Increment DPL                                               | 1 1 1 0                                                                | 1 1 1 0                                                                                                        | 1     | 1      | DPL ← (DPL) + 1                                                                                                                                                                                                           | The DPL contents are incremented +1.                                                                                                                                                                                                                                                                                | ZF                   |                                                                                                                                                                                                                                                                                                                                                             |
|                                            | DED       | Decrement DPL                                               | 1 1 1 0                                                                | 1 1 1 1                                                                                                        | 1     | 1      | DPL ← (DPL) - 1                                                                                                                                                                                                           | The DPL contents are decremented -1.                                                                                                                                                                                                                                                                                | ZF                   |                                                                                                                                                                                                                                                                                                                                                             |
|                                            | TAL       | Transfer AC to DPL                                          | 1 1 1 1                                                                | 0 1 1 1                                                                                                        | 1     | 1      | DPL ← (AC)                                                                                                                                                                                                                | The AC contents are transferred to the DPL.                                                                                                                                                                                                                                                                         |                      |                                                                                                                                                                                                                                                                                                                                                             |
|                                            | TLA       | Transfer DPL to AC                                          | 1 1 1 0                                                                | 1 0 0 1                                                                                                        | 1     | 1      | AC ← (DPL)                                                                                                                                                                                                                | The DPL contents are transferred to the AC.                                                                                                                                                                                                                                                                         | ZF                   |                                                                                                                                                                                                                                                                                                                                                             |
|                                            | XA H      | Exchange AC with DPH                                        | 0 0 1 0                                                                | 0 0 1 1                                                                                                        | 1     | 1      | (AC) ↔ (DPH)                                                                                                                                                                                                              | The AC contents and the DPH contents are exchanged.                                                                                                                                                                                                                                                                 |                      |                                                                                                                                                                                                                                                                                                                                                             |
| Working register manipulation instructions | XAt       | Exchange AC with working register At                        | 1 1 1 0                                                                | 11 10                                                                                                          | 1     | 1      | (AC) ↔ (A0)<br>(AC) ↔ (A1)<br>(AC) ↔ (A2)<br>(AC) ↔ (A3)                                                                                                                                                                  | The AC contents and the contents of working register At are exchanged. At is assigned one of A0, A1, A2, A3 according to t <sub>1</sub> t <sub>0</sub> .                                                                                                                                                            |                      |                                                                                                                                                                                                                                                                                                                                                             |
|                                            | XHa       | Exchange DPH with working register Ha                       | 1 1 1 1                                                                | 10 00                                                                                                          | 1     | 1      | (DPH) ↔ (H0)<br>(DPH) ↔ (H1)                                                                                                                                                                                              | The DPH contents and the contents of working register Ha are exchanged. Ha is assigned either of H0 or H1 according to a.                                                                                                                                                                                           |                      |                                                                                                                                                                                                                                                                                                                                                             |
|                                            | XLa       | Exchange DPL with working register La                       | 1 1 1 1                                                                | 01 00                                                                                                          | 1     | 1      | (DPL) ↔ (L0)<br>(DPL) ↔ (L1)                                                                                                                                                                                              | The DPL contents and the contents of working register La are exchanged. La is assigned either of L0 or L1 according to a.                                                                                                                                                                                           |                      |                                                                                                                                                                                                                                                                                                                                                             |
|                                            | XA0       |                                                             | 1 1 1 0                                                                | 0 0 0 0                                                                                                        | 1     | 1      |                                                                                                                                                                                                                           |                                                                                                                                                                                                                                                                                                                     |                      |                                                                                                                                                                                                                                                                                                                                                             |
|                                            | XA1       |                                                             | 1 1 1 0                                                                | 0 1 0 0                                                                                                        | 1     | 1      |                                                                                                                                                                                                                           |                                                                                                                                                                                                                                                                                                                     |                      |                                                                                                                                                                                                                                                                                                                                                             |
|                                            | XA2       |                                                             | 1 1 1 0                                                                | 1 0 0 0                                                                                                        | 1     | 1      |                                                                                                                                                                                                                           |                                                                                                                                                                                                                                                                                                                     |                      |                                                                                                                                                                                                                                                                                                                                                             |
| Flag manipulation instructions             | SFB flag  | Set flag bit                                                | 0 1 0 1                                                                | B3 B2 B1 B0                                                                                                    | 1     | 1      | F <sub>n</sub> ← 1                                                                                                                                                                                                        | The flag specified with B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub> is set.                                                                                                                                                                                                                         |                      |                                                                                                                                                                                                                                                                                                                                                             |
|                                            | RFB flag  | Reset flag bit                                              | 0 0 0 1                                                                | B3 B2 B1 B0                                                                                                    | 1     | 1      | F <sub>n</sub> ← 0                                                                                                                                                                                                        | The flag specified with B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub> is reset.                                                                                                                                                                                                                       | ZF                   | The flags are divided into 4 groups of F <sub>0</sub> to F <sub>3</sub> , F <sub>4</sub> to F <sub>7</sub> , F <sub>8</sub> to F <sub>11</sub> , F <sub>12</sub> to F <sub>15</sub> .<br>The ZF is set/reset according to the 4 bits including a single bit specified with the immediate data B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub> . |
| Jump/subroutine instructions               | JMP addr  | Jump in the current bank                                    | 0 1 1 0<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | 1 P <sub>10</sub> P <sub>9</sub> P <sub>8</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> | 2     | 2      | PC ← PC <sub>11</sub> (又は PC <sub>11</sub> ).<br>P <sub>10</sub> P <sub>9</sub> P <sub>8</sub> P <sub>7</sub> P <sub>6</sub> P <sub>5</sub><br>P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> | A jump to the address specified with the PC <sub>11</sub> (or PC <sub>11</sub> ) and immediate data P <sub>10</sub> P <sub>9</sub> P <sub>8</sub> P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> occurs.                                   |                      | If the BANK and JMP instructions are executed consecutively, PC <sub>11</sub> → PC <sub>11</sub> .                                                                                                                                                                                                                                                          |
|                                            | JPEA      | Jump in the current page modified by E and AC               | 1 1 1 1                                                                | 1 0 1 0                                                                                                        | 1     | 1      | PC <sub>7~0</sub> ← (E, AC)                                                                                                                                                                                               | A jump to the address specified with the contents of the PC whose low-order 8 bits are replaced by the E and AC contents occurs.                                                                                                                                                                                    |                      |                                                                                                                                                                                                                                                                                                                                                             |
|                                            | CZP addr  | Call subroutine in the zero page                            | 1 0 1 1                                                                | P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>                                                    | 1     | 1      | STACK ← (PC) + 1<br>PC <sub>11~6</sub> , PC <sub>1~0</sub> ← 0<br>PC <sub>5~2</sub> ← P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>                                                                         | A subroutine in page 0 of bank 0 is called.                                                                                                                                                                                                                                                                         |                      |                                                                                                                                                                                                                                                                                                                                                             |
|                                            | CAL addr  | Call subroutine in the zero bank                            | 1 0 1 0<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | 1 P <sub>10</sub> P <sub>9</sub> P <sub>8</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> | 2     | 2      | STACK ← (PC) + 2<br>PC <sub>11~0</sub> ← OP <sub>10</sub> P <sub>9</sub> P <sub>8</sub> P <sub>7</sub><br>P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>        | A subroutine in bank 0 is called.                                                                                                                                                                                                                                                                                   |                      |                                                                                                                                                                                                                                                                                                                                                             |
|                                            | RT        | Return from subroutine                                      | 0 1 1 0                                                                | 0 0 1 0                                                                                                        | 1     | 1      | PC ← (STACK)                                                                                                                                                                                                              | A return from a subroutine occurs.                                                                                                                                                                                                                                                                                  |                      |                                                                                                                                                                                                                                                                                                                                                             |
|                                            | RTI       | Return from interrupt routine                               | 0 0 1 0                                                                | 0 0 1 0                                                                                                        | 1     | 1      | PC ← (STACK)<br>CF ZF ← CSF, ZSF                                                                                                                                                                                          | A return from an interrupt service routine occurs.                                                                                                                                                                                                                                                                  | ZF CF                |                                                                                                                                                                                                                                                                                                                                                             |
|                                            | BANK      | Change bank                                                 | 1 1 1 1                                                                | 1 1 0 1                                                                                                        | 1     | 1      | PC <sub>11</sub> ← (PC <sub>11</sub> )                                                                                                                                                                                    | The bank is changed.                                                                                                                                                                                                                                                                                                |                      | Effective only when used immediately before the JMP instruction.                                                                                                                                                                                                                                                                                            |
| Branch instructions                        | BAt addr  | Branch on AC bit                                            | 0 1 1 1<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | 0 0 1 1 t <sub>0</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>                          | 2     | 2      | PC <sub>7~0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub><br>if AC <sub>1</sub> = 1                                                  | If a single bit of the AC specified with the immediate data t <sub>1</sub> t <sub>0</sub> is 1, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.      |                      | Mnemonic is BAO to BA3 according to the value of t.                                                                                                                                                                                                                                                                                                         |
|                                            | BNAt addr | Branch on no AC bit                                         | 0 0 1 1<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | 0 0 1 1 t <sub>0</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>                          | 2     | 2      | PC <sub>7~0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub><br>if AC <sub>1</sub> = 0                                                  | If a single bit of the AC specified with the immediate data t <sub>1</sub> t <sub>0</sub> is 0, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.      |                      | Mnemonic is BNA0 to BNA3 according to the value of t.                                                                                                                                                                                                                                                                                                       |
|                                            | BMt addr  | Branch on M bit                                             | 0 1 1 1<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | 0 1 1 1 t <sub>0</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>                          | 2     | 2      | PC <sub>7~0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub><br>if (M(DP), t <sub>1</sub> t <sub>0</sub> ) = 1                          | If a single bit of the M(DP) specified with the immediate data t <sub>1</sub> t <sub>0</sub> is 1, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.   |                      | Mnemonic is BMO to BM3 according to the value of t.                                                                                                                                                                                                                                                                                                         |
|                                            | BNMt addr | Branch on no M bit                                          | 0 0 1 1<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | 0 1 1 1 t <sub>0</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>                          | 2     | 2      | PC <sub>7~0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub><br>if (M(DP), t <sub>1</sub> t <sub>0</sub> ) = 0                          | If a single bit of the M(DP) specified with the immediate data t <sub>1</sub> t <sub>0</sub> is 0, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.   |                      | Mnemonic is BNMO to BNM3 according to the value of t.                                                                                                                                                                                                                                                                                                       |
|                                            | BPt addr  | Branch on Port bit                                          | 0 1 1 1<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | 1 0 1 1 t <sub>0</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>                          | 2     | 2      | PC <sub>7~0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub><br>if (P(DPL), t <sub>1</sub> t <sub>0</sub> ) = 1                         | If a single bit of port P(DPL) specified with the immediate data t <sub>1</sub> t <sub>0</sub> is 1, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs. |                      | Mnemonic is BPO to BP3 according to the value of t.                                                                                                                                                                                                                                                                                                         |
|                                            | BNPt addr | Branch on no Port bit                                       | 0 0 1 1<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | 1 0 1 1 t <sub>0</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>                          | 2     | 2      | PC <sub>7~0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub><br>if (P(DPL), t <sub>1</sub> t <sub>0</sub> ) = 0                         | If a single bit of port P(DPL) specified with the immediate data t <sub>1</sub> t <sub>0</sub> is 0, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs. |                      | Mnemonic is BNPO to BNP3 according to the value of t.                                                                                                                                                                                                                                                                                                       |
|                                            | BTM addr  | Branch on timer                                             | 0 1 1 1<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | 1 1 0 0<br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>                                         | 2     | 2      | PC <sub>7~0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub><br>if TMF = 1<br>then TMF ← 0                                              | If the TMF is 1, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs. The TMF is reset.                                                                   | TMF                  |                                                                                                                                                                                                                                                                                                                                                             |

| Instruction               | Mnemonic              | Instruction code                                            |                                                                        | Bytes                                                                                                                      | Cycles | Function | Description                                                                                                                                                                    | Status flag affected                                                                                                                                                                                                                                                                                                                               | Remarks |                                                                  |
|---------------------------|-----------------------|-------------------------------------------------------------|------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------|--------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|------------------------------------------------------------------|
|                           |                       | D <sub>7</sub> D <sub>6</sub> D <sub>5</sub> D <sub>4</sub> | D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub>            |                                                                                                                            |        |          |                                                                                                                                                                                |                                                                                                                                                                                                                                                                                                                                                    |         |                                                                  |
| Branch instructions       | BN <sub>TM</sub> addr | Branch on no timer                                          | 0 0 1 1<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | 1 1 0 0<br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>                                                     | 2      | 2        | PC <sub>7~0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub><br>if TMF = 0<br>then TMF ← 0   | If the TMF is 0, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs. The TMF is reset.                                                                                                  | TMF     |                                                                  |
|                           | BI addr               | Branch on interrupt                                         | 0 1 1 1<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | 1 1 0 1<br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>                                                     | 2      | 2        | PC <sub>7~0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub><br>if EXTF = 1<br>then EXTF ← 0 | If the EXTF is 1, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs. The EXTF is reset.                                                                                                | EXTF    |                                                                  |
|                           | BNI addr              | Branch on no interrupt                                      | 0 0 1 1<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | 1 1 0 1<br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>                                                     | 2      | 2        | PC <sub>7~0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub><br>if EXTF = 0<br>then EXTF ← 0 | If the EXTF is 0, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs. The EXTF is reset.                                                                                                | EXTF    |                                                                  |
|                           | BC addr               | Branch on CF                                                | 0 1 1 1<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | 1 1 1 1<br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>                                                     | 2      | 2        | PC <sub>7~0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub><br>if CF = 1                    | If the CF is 1, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.                                                                                                                     |         |                                                                  |
|                           | BNC addr              | Branch on no CF                                             | 0 0 1 1<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | 1 1 1 1<br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>                                                     | 2      | 2        | PC <sub>7~0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub><br>if CF = 0                    | If the CF is 0, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.                                                                                                                     |         |                                                                  |
|                           | BZ addr               | Branch on ZF                                                | 0 1 1 1<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | 1 1 1 0<br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>                                                     | 2      | 2        | PC <sub>7~0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub><br>if ZF = 1                    | If the ZF is 1, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.                                                                                                                     |         |                                                                  |
|                           | BNZ addr              | Branch on no ZF                                             | 0 0 1 1<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | 1 1 1 0<br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>                                                     | 2      | 2        | PC <sub>7~0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub><br>if ZF = 0                    | If the ZF is 0, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs.                                                                                                                     |         |                                                                  |
|                           | BF <sub>n</sub> addr  | Branch on flag bit                                          | 1 1 0 1<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | n <sub>3</sub> n <sub>2</sub> n <sub>1</sub> n <sub>0</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> | 2      | 2        | PC <sub>7~0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub><br>if F <sub>n</sub> = 1        | If the flag bit of the 16 flags specified with the immediate data n <sub>3</sub> n <sub>2</sub> n <sub>1</sub> n <sub>0</sub> is 1, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs. |         | Mnemonic is BFD to BF15 according to the value of n.             |
|                           | BNF <sub>n</sub> addr | Branch on no flag bit                                       | 1 0 0 1<br>P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> | n <sub>3</sub> n <sub>2</sub> n <sub>1</sub> n <sub>0</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> | 2      | 2        | PC <sub>7~0</sub> ← P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub><br>P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub><br>if F <sub>n</sub> = 0        | If the flag bit of the 16 flags specified with the immediate data n <sub>3</sub> n <sub>2</sub> n <sub>1</sub> n <sub>0</sub> is 0, a branch to the address specified with the immediate data P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> within the same page occurs. |         | Mnemonic is BNF0 to BNF15 according to the value of n.           |
| Input/Output instructions | IP                    | Input port to AC                                            | 0 0 0 0                                                                | 1 1 0 0                                                                                                                    | 1      | 1        | AC ← {P(DP <sub>L</sub> )}                                                                                                                                                     | Port P(DP <sub>L</sub> ) contents are loaded in the AC.                                                                                                                                                                                                                                                                                            | ZF      |                                                                  |
|                           | OP                    | Output AC to port                                           | 0 1 1 0                                                                | 0 0 0 1                                                                                                                    | 1      | 1        | P(DP <sub>L</sub> ) ← {AC}                                                                                                                                                     | The AC contents are outputted to port P(DP <sub>L</sub> ).                                                                                                                                                                                                                                                                                         |         |                                                                  |
|                           | SPB bit               | Set port bit                                                | 0 0 0 0                                                                | 0 1 B <sub>1</sub> B <sub>0</sub>                                                                                          | 1      | 2        | P(DP <sub>L</sub> , B <sub>1</sub> B <sub>0</sub> ) ← 1                                                                                                                        | A single bit in port P(DP <sub>L</sub> ) specified with the immediate data B <sub>1</sub> B <sub>0</sub> is set.                                                                                                                                                                                                                                   |         | When this instruction is executed, the E contents are destroyed. |
|                           | RPB bit               | Reset port bit                                              | 0 0 1 0                                                                | 0 1 B <sub>1</sub> B <sub>0</sub>                                                                                          | 1      | 2        | P(DP <sub>L</sub> , B <sub>1</sub> B <sub>0</sub> ) ← 0                                                                                                                        | A single bit in port P(DP <sub>L</sub> ) specified with the immediate data B <sub>1</sub> B <sub>0</sub> is reset.                                                                                                                                                                                                                                 | ZF      | When this instruction is executed, the E contents are destroyed. |
| Other instructions        | SCTL bit              | Set control register bit(S)                                 | 0 0 1 0<br>1 0 0 0                                                     | 1 1 0 0<br>B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub>                                                     | 2      | 2        | CTL ← (CTL) V<br>B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub>                                                                                                   | The bits of the control register specified with the immediate data B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub> are set.                                                                                                                                                                                                            |         |                                                                  |
|                           | RCTL bit              | Reset control register bit(S)                               | 0 0 1 0<br>1 0 0 1                                                     | 1 1 0 0<br>B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub>                                                     | 2      | 2        | CTL ← (CTL) A<br>B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub>                                                                                                   | The bits of the control register specified with the immediate data B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub> are reset.                                                                                                                                                                                                          | ZF      |                                                                  |
|                           | WTIM                  | Write timer                                                 | 1 1 1 1                                                                | 1 0 0 1                                                                                                                    | 1      | 1        | TM ← {E}, {AC}<br>TMF ← 0                                                                                                                                                      | The E and AC contents are loaded in the timer. The TMF is reset.                                                                                                                                                                                                                                                                                   | TMF     |                                                                  |
|                           | HALT                  | Halt                                                        | 1 1 1 1                                                                | 0 1 1 0                                                                                                                    | 1      | 1        | Halt                                                                                                                                                                           | All operations stop.                                                                                                                                                                                                                                                                                                                               |         | Only when all pins of port PA are set at L stop.                 |
|                           | NOP                   | No operation                                                | 0 0 0 0                                                                | 0 0 0 0                                                                                                                    | 1      | 1        | No operation                                                                                                                                                                   | No operation is performed, but 1 machine cycle is consumed.                                                                                                                                                                                                                                                                                        |         |                                                                  |

\*1 If the CLA instruction is used continuously in such a manner as CLA, CLA, ———, the first CLA instruction only is effective and the following CLA instructions are changed to the NOP instructions. This is also true of the LI instruction.