Quad Channel 155 Mbit/s SONET/SDH Framer and Aligner

FEATURES

- Monolithic four channel SONET/SDH Payload Extractor/Aligner for use in STS-3 (STM-1/AU-3) or STS-3c (STM-1/AU-4) interface applications, operating at serial interface speeds of 155.52 Mbit/s.

- Provides integrated clock recovery and clock synthesis to allow direct interface to optical modules.

- Each channel provides termination for SONET Section and Line, SDH Regenerator Section and Multiplexer Section transport overhead, and path overhead of three STS-1 (STM-0/AU-3) paths or a single STS-3c (STM-1/AU-4) path.

- Each channel maps three STS-1 (STM-0/AU-3) payloads or a single STS-3c (STM-1/AU-4) payload to system timing reference, accommodating plesiosynchronous timing offsets between the references through pointer processing.

- The entire SONET/SDH transport and path overheads are extracted to and inserted from dedicated pins.

- Frames to the SONET/SDH receive stream and inserts framing bytes and STS identification into the transmit stream and processes or inserts the transport overhead.

- Interprets or generates the STS (AU) pointer bytes (H1, H2, H3), extracts or inserts the synchronous payload envelope(s) and processes or inserts the path overhead.

- Supports Automatic Protection Switching (APS):
  - Ring control port communication of path REI and path RDI alarms;
  - Filters the APS channel (K1,K2) bytes into internal registers; inserts the APS channel into the transmit stream.

- Provides Time Slot Interchange (TSI) function at the ADD and DROP TelecomBus Interfaces for grooming twelve STS-1 (STM-0/AU-3) paths.

- Supports line loopback from the line side receive stream to the transmit stream and diagnostic loopback from an ADD TelecomBus interface to a DROP TelecomBus interface.

- Provides a standard five signal P1149.1 JTAG test port for boundary scan board test purposes.

- Provides a generic 8-bit microprocessor bus interface for configuration, control, and status monitoring.

- Low power 3.3 V CMOS with TTL compatible digital inputs and CMOS/TTL digital outputs.

- Industrial temperature range (-40°C to +85°C).

- 520 pin Super BGA package.

- Supports clock recovery bypass for use in applications where external clock recovery is desired.

- Complies with Bellcore GR-253-CORE jitter tolerance, jitter transfer, and intrinsic jitter criteria.

BLOCK DIAGRAM
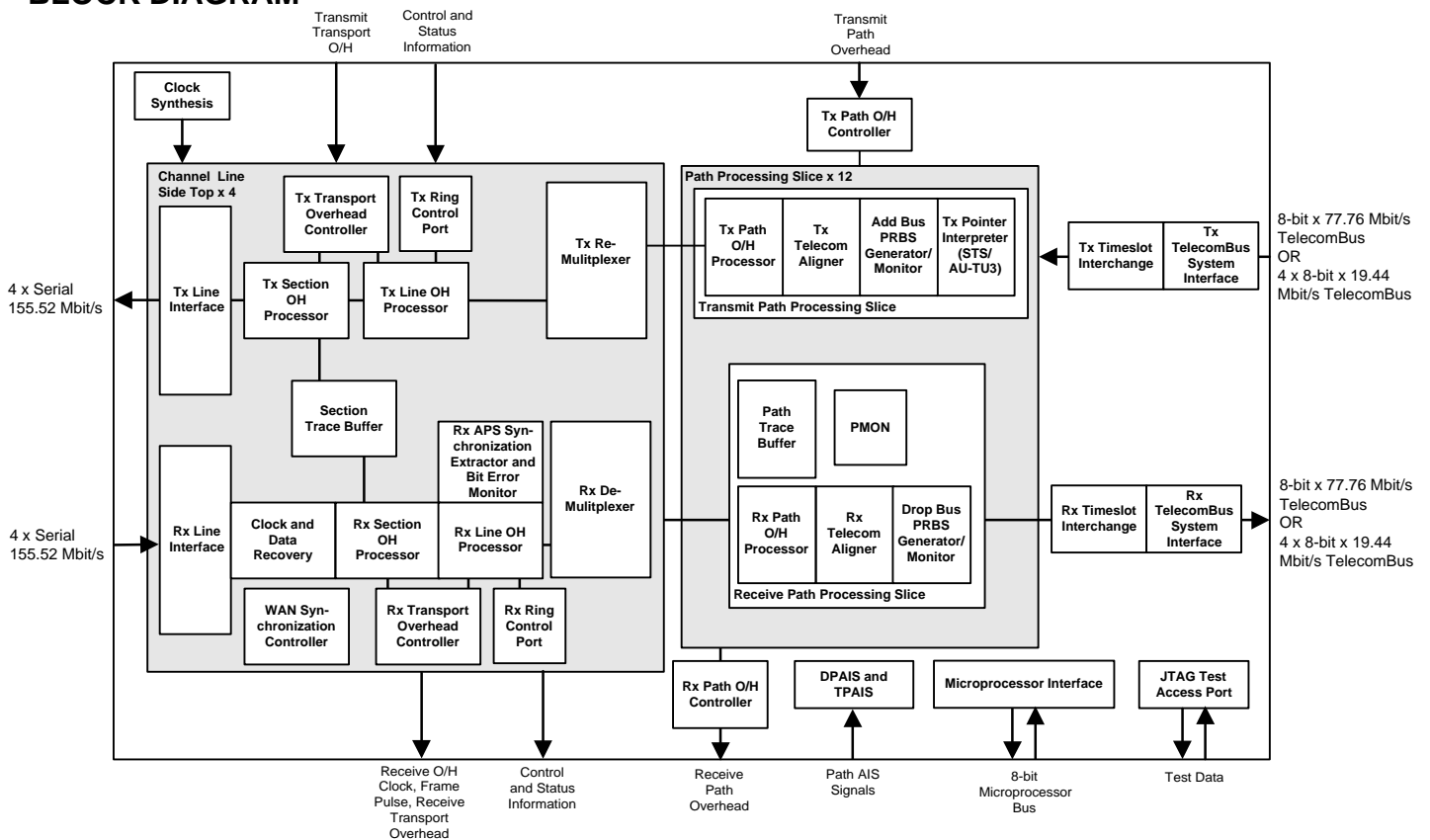
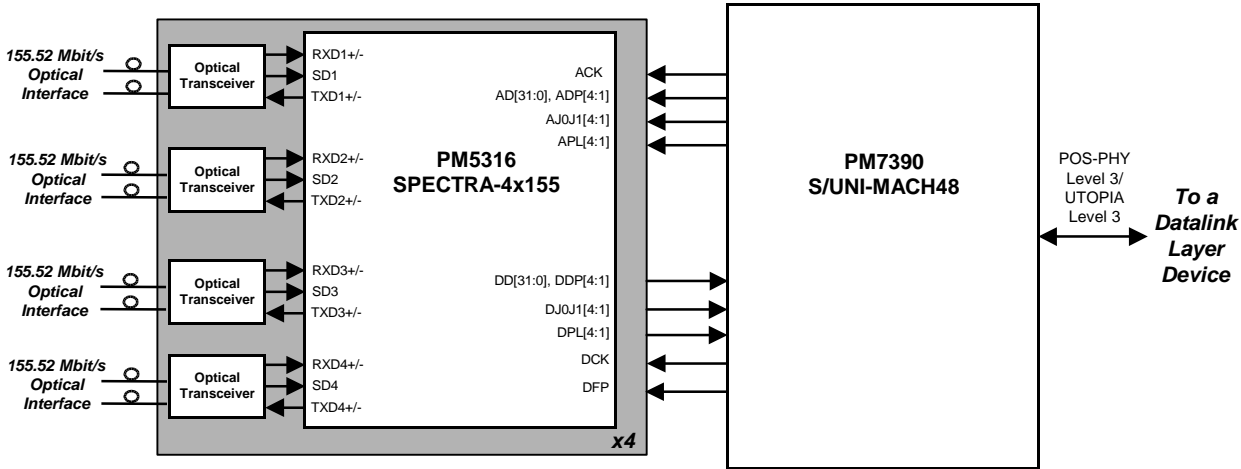## Quad Channel 155 Mbit/s SONET/SDH Framer and Aligner

APPLICATIONS

• Channelized STS-3/STM-1 Interfaces for:

  • Optical Cross Connects;
  • Digital Cross Connects;
  • Router and Switch Line Cards;
  • ADM Aggregate Cards for TDM and Multi-service applications;
  • Terminal Multiplexers.

TYPICAL APPLICATIONS

STS-3/STM-0 APPLICATION WITH VT/TU POINTER PROCESSING/ALIGNMENT
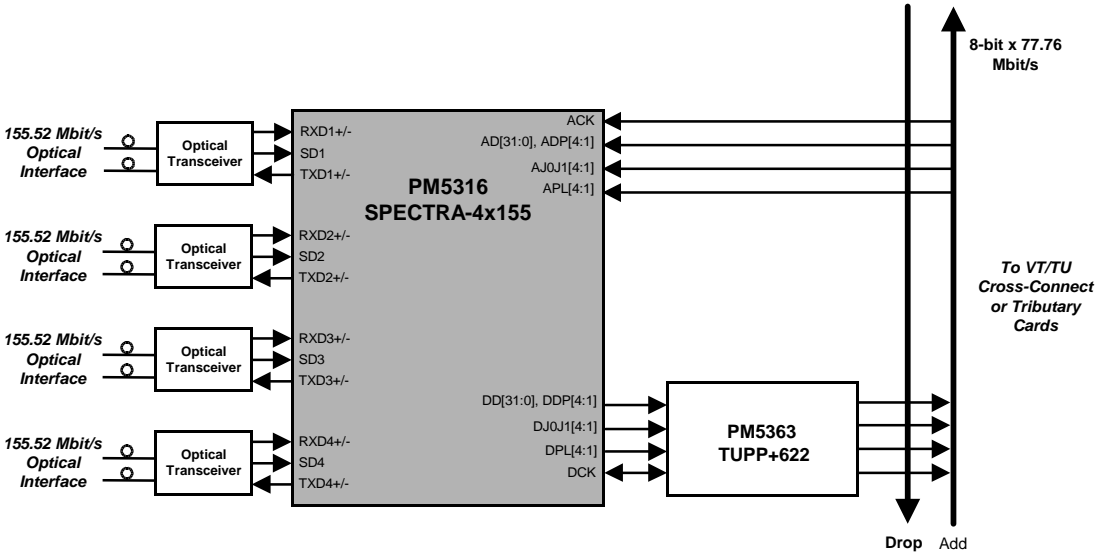
16 X STS-3/STM-0 APPLICATION WITH POS/ATM PROCESSING