2

Description of Instructions

2.1 ADCAM

Operation: Acc ← Acc + RAM[HL] + CF

Description: Add the contents of the data memory specified by the HL registers and the carry flag to the accumulator, and place the result in the accumulator.

Code Bytes	Instruction Cycles	Object Code
1	1	0111 0000

Flags

C	Set the carry flag if the accumulator has a carry from the highest bit after the add operation; clear otherwise.
Z	Set the zero flag if the value of the accumulator is 0; clear otherwise.
S	Transfer the inverse value of the carry flag to the status flag.

2.2 ADD #k, y

Operation: RAM[y] ← RAM[y] + k

Description: Add the immediate data K to the contents of the data memory specified by the zero page address y (y = 0 ~ $0F_H$), and place the result in the data memory.

Code Bytes	Instruction Cycles	Object Code
2	2	0100 1001 kkkk yyyy

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the data memory is 0; clear otherwise.
S	Transfer the inverse value of the carry flag to the status flag.

2.3 ADDA #k

Operation: Acc ← Acc + k

Description: Add the immediate data K to the contents of the accumulator, and place the result in the accumulator.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1110 0101 kkkk

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the accumulator is 0; clear otherwise.
S	Transfer the inverse value of the carry flag to the status flag.

2.4 ADDAM

Operation: Acc ← Acc + RAM[HL]

Description: Add the immediate data K to the contents of the accumulator, and place the result in the accumulator.

Code Bytes	Instruction Cycles	Object Code
1	1	0111 0001

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the accumulator is 0; clear otherwise.
S	Transfer the inverse value of the carry flag to the status flag.

2.5 ADDAH #k

Operation: HR ← HR + k

Description: Add the immediate data K to the contents of the H register, and place the result in the H register.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1110 1001 kkkk

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the H register is 0; clear otherwise.
S	Transfer the inverse value of the carry flag to the status flag.

2.6 ADDL #k

Operation: LR ← LR + k

Description: Add the immediate data K to the contents of the L register, and place the result in the L register.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1110 0001 kkkk

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the L register is 0; clear otherwise.
S	Transfer the inverse value of the carry flag to the status flag.

2.7 ADDM #k

Operation: RAM[HL] ← RAM[HL] + k

Description: Add the immediate data K to the contents of the data memory specified by the H and L registers, and place the result in the data memory.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1110 1101 kkkk

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the data memory is 0; clear otherwise.
S	Transfer the inverse value of the carry flag to the status flag.

2.8 ANDA #k

Operation: Acc ← Acc & k

Description: Logic AND the contents of the accumulator and the immediate data k, and place the result in the accumulator.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1110 0110 kkkk

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the accumulator is 0; clear otherwise.
S	Transfer the inverse value of the zero flag to the status flag.

2.9 ANDAM

Operation: Acc ← Acc & RAM[HL]

Description: Logic AND the contents of the accumulator and the immediate data k, and place the result in the accumulator.

Code Bytes	Instruction Cycles	Object Code
1	1	0111 1011

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the accumulator is 0; clear otherwise.
S	Transfer the inverse value of the zero flag to the status flag.

2.10 ANDM #k

Operation: RAM[HL] ← RAM[HL[& k

Description: Logic AND the contents of the accumulator and the immediate data k, and place the result in the accumulator.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1110 1110 kkkk

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the data memory is 0; clear otherwise.
S	Transfer the inverse value of the zero flag to the status flag.

2.11 CGF

Operation: GF ← 0

Description: Clear the general flag to zero. Note that this instruction does not apply to the 8K ROM chip.

Code Bytes	Instruction Cycles	Object Code
1	1	0101 0111

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is always 1.

2.12 CIL r

Operation: IL ← IL & r

Description: Clear the interrupt latch IL_i with $r_i = 0$ (i = 0 ~ 5).

Code Bytes	Instruction Cycles	Object Code
1	1	0110 0011 10rr rrrr

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is always 1.

2.13 CLM b

Operation: RAM[HL] b ← 0

Description: Clear the bit b of the data memory specified by the H and L registers to 0.

Code Bytes	Instruction Cycles	Object Code
1	1	1111 00bb

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is always 1.

2.14 CLP p, b

Operation: PORT[p] b ← 0

Description: Clear the bit b of the port p (p = 0 ~ 15) to 0.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1101 11bb pppp

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is always 1.

2.15 CLPL

Operation: PORT[$LR_{3\sim2}$ + 4] $LR_{1\sim0} \leftarrow 0$

Description: Clear the bit of the port specified by the L register to 0. The bit number is specified by bit1 ~ bit0 of the L register and the port number (P4 ~ P7) is equal to 4 plus the bit3 ~ bit2 of the L register.

Code Bytes	Instruction Cycles	Object Code
1	2	0110 0000

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is always 1.

2.16 CLR y, b

Operation: RAM[y] b ← 0

Description: Clear the bit b of the data memory specified by the zero-page address y (y = 0 ~ $0F_H$) to 0.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1100 11bb yyyy

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is always 1.

2.17 CMP #k, y

Operation: K - RAM[y]

Description: Compare the immediate data k with the contents of the data memory specified by the zero-page address y (y = 0 ~ $0F_H$).

Code Bytes	Instruction Cycles	Object Code
2	2	0100 1011 kkkk yyyy

Flags

C	Set the carry flag if k ≥ RAM[y]; clear otherwise.
Z	Set the zero flag if k = RAM[y]; clear otherwise.
S	Transfer the inverse value of the zero flag to the status flag.

2.18 CMPA x

Operation: RAM[x] - Acc

Description: Compare the contents of the data memory specified by the address x with the contents of the accumulator.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1011 xxxx xxxx

Flags

C	Set the carry flag if RAM[x] ≥ Acc; clear otherwise.
Z	Set the zero flag if RAM[x] = Acc; clear otherwise.
S	Transfer the inverse value of the zero flag to the status flag.

2.19 CMPM

Operation: RAM[HL] - Acc

Description: Compare the contents of the data memory specified by the contents of the H and L registers with the contents of the accumulator.

Code Bytes	Instruction Cycles	Object Code
1	1	0111 0011

Flags

C	Set the carry flag if RAM[HL] ≥ Acc; clear otherwise.
Z	Set the zero flag if RAM[HL] = Acc; clear otherwise.
S	Transfer the inverse value of the zero flag to the status flag.

2.20 CMPH #k

Operation: k - HR

Description: Compare the immediate data k with the contents of the H register.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1110 1011 kkkk

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if k = HR; clear otherwise.
S	Set the status flag if k ≥ HR; clear otherwise.

2.21 CMPIA #k

Operation: k - Acc

Description: Compare the immediate data k with the contents of the accumulator.

Code Bytes	Instruction Cycles	Object Code
1	1	1011 kkkk

Flags

C	Set the carry flag if k ≥ Acc; clear otherwise.
Z	Set the zero flag if k = HR; clear otherwise.
S	Transfer the inverse value of the zero flag to the status flag.

2.22 CMPL #k

Operation: k - LR

Description: Compare the immediate data k with the contents of the L register.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1110 0011 kkkk

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if k = LR; clear otherwise.
S	Set the status flag if k ≥ LR; clear otherwise.

2.23 DECA

Operation: Acc ← Acc - 1

Description: Decrease the contents of the accumulator by 1.

Code Bytes	Instruction Cycles	Object Code
1	1	0101 1100

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the accumulator is 0; clear otherwise.
S	Transfer the value of the carry flag to the status flag.

2.24 DECL

Operation: LR ← LR - 1

Description: Decrease the contents of the L register by 1.

Code Bytes	Instruction Cycles	Object Code
1	1	0111 1100

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the L register is 0; clear otherwise.
S	Transfer the value of the carry flag to the status flag.

2.25 DECM

Operation: RAM[HL] ← RAM[HL] - 1

Description: Decrease the contents of the data memory specified by the H and L registers by 1.

Code Bytes	Instruction Cycles	Object Code
1	1	0101 1101

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the data memory is 0; clear otherwise.
S	Transfer the value of the carry flag to the status flag.

2.26 DICIL r

Operation: EIF ← 0, IL ← IL & r

Description: Disable interrupt Flip-Flop and clear the interrupt latch IL_i with $r_i = 0$ (i = 0 ~ 5).

Code Bytes	Instruction Cycles	Object Code
2	2	0110 0011 00rr rrrr

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is always 1.

2.27 EICIL r

Operation: EI ← 1, IL ← IL & r

Description: Enable interrupt Flip-Flop and clear the interrupt latch IL_i with $r_i = 0$ (i = 0 ~ 5).

Code Bytes	Instruction Cycles	Object Code
2	2	0110 0011 11rr rrrr

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is always 1.

2.28 EXA x

Operation: Acc ↔ RAM[x]

Description: Exchange the contents the accumulator and the data memory specified by the address x.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1000 xxxx xxxx

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the accumulator is 0; clear otherwise.
S	The value of the status flag is always 1.

2.29 EXAE

Operation: EIR ↔ Acc

Description: Exchange the contents the interrupt enable registers and the accumulator.

Code Bytes	Instruction Cycles	Object Code
1	1	0110 1000 xxxx xxxx

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is always 1.

2.30 EXAH

Operation: Acc ↔ HR

Description: Exchange the contents the accumulator and the H register.

Code Bytes	Instruction Cycles	Object Code
1	2	0110 0110

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the accumulator is 0; clear otherwise.
S	The value of the status flag is always 1.

2.31 EXAL

Operation: Acc ↔ LR

Description: Exchange the contents the accumulator and the L register.

Code Bytes	Instruction Cycles	Object Code
1	2	0110 0100

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the accumulator is 0; clear otherwise.
S	The value of the status flag is always 1.

2.32 EXAM

Operation: Acc ↔ RAM[HL]

Description: Exchange the contents the accumulator and the data memory specified by the H and L registers.

Code Bytes	Instruction Cycles	Object Code
1	1	0101 1000

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the accumulator is 0; clear otherwise.
S	The value of the status flag is always 1.

2.33 EXHL x

Operation: LR ↔ RAM[x], HR ↔ RAM[x+1]

Description: Exchange the contents the H and L registers with the data memory specified by the address x, which lower two bits must be zero.

Code Bytes	Instruction Cycles	Object Code
2	2	0100 1100 xxxx xx00

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed..
S	The value of the status flag is always 1.

2.34 INA p

Operation: Acc ← PORT[p]

Description: Place the input data from port p (p = 0 ~ 15) in the accumulator.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1111 0100 pppp

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the accumulator is 0; clear otherwise.
S	Transfer the inverse value of the zero flag to the status flag.

2.35 INCA

Operation: Acc ← Acc + 1

Description: Increase the contents of the accumulator by one.

Code Bytes	Instruction Cycles	Object Code
1	1	0101 1110

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the accumulator is 0; clear otherwise.
S	Transfer the inverse value of the carry flag to the status flag.

2.36 INCL

Operation: LR ← LR + 1

Description: Increase the contents of the L register by one.

Code Bytes	Instruction Cycles	Object Code
1	1	0111 1110

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the L register is 0; clear otherwise.
S	Transfer the inverse value of the carry flag to the status flag.

2.37 INCM

Operation: RAM[HL] ← RAM[HL] + 1

Description: Increase the contents of the L register by one.

Code Bytes	Instruction Cycles	Object Code
1	1	0101 1111

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the data memory is 0; clear otherwise.
S	Transfer the inverse value of the carry flag to the status flag.

2.38 INM p

Operation: RAM[HL] ← PORT[p]

Description: Place the input data from port p (p = 0 ~ 15) in the data memory specified by the H and L registers.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1111 1100 pppp

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	Transfer the inverse value of the zero flag to the status flag.

2.39 LBR a

Operation: If SF = 1, then PC ← $a_{11\sim0}$ else null

Description: If the status flag is equal to one, the program branches to the destination address a (PC ← $a_{11\sim0}$) within one bank (one bank = 4K bytes). If the status flag equals zero, set the status flag to one and increment the program counter to the next address (PC ← PC +2).

Code Bytes	Instruction Cycles	Object Code
2	2	1100 aaaa aaaa aaaa

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is always one.

2.40 LCALL a

Operation: STACK[SP] ← PC, SP ← SP - 1, PC ← a, a = 0 ~ $07FF_H$

Description: For the subroutine call, save the contents of the program counter in the stack (location SP), decease the stack pointer, and place the address a (a = 0 ~ $07FF_H$) in the program counter.

Code Bytes	Instruction Cycles	Object Code
2	2	0100 0aaa aaaa aaaa

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is not changed.

2.41 LDA x

Operation: Acc ← RAM[x]

Description: Load the contents of the data memory specified by the address x into the accumulator.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1010 xxxx xxxx

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the data memory is 0; clear otherwise.
S	The value of the status flag is always 1.

2.42 LDADPL

Operation: Acc ← $[DP]_L$

Description: Load the contents of the low nibble data pointer register into the accumulator.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1010 1111 1100

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the register is 0; clear otherwise.
S	The value of the status flag is always 1.

2.43 LDADPM

Operation: Acc ← $[DP]_M$

Description: Load the contents of the middle nibble data pointer register into the accumulator.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1010 1111 1101

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the register is 0; clear otherwise.
S	The value of the status flag is always 1.

2.44 LDADPH

Operation: Acc ← $[DP]_H$

Description: Load the contents of the high nibble data pointer register into the accumulator.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1010 1111 1110

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the register is 0; clear otherwise.
S	The value of the status flag is always 1.

2.45 LDAM

Operation: Acc ← RAM[HL]

Description: Load the contents of the data memory specified by the H and L registers into the accumulator.

Code Bytes	Instruction Cycles	Object Code
1	1	0101 1010

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the data memory is 0; clear otherwise.
S	The value of the status flag is always 1.

2.46 LDASP

Operation: Acc ← SP

Description: Load the contents of the stack pointer into the accumulator.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1010 1111 1111

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the stack pointer is 0; clear otherwise.
S	The value of the status flag is always 1.

2.47 LDATAL

Operation: Acc ← $[TA]_L$

Description: Load the contents of the low nibble timer/counter A register into the accumulator.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1010 1111 0100

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the register is 0; clear otherwise.
S	The value of the status flag is always 1.

2.48 LDATAM

Operation: Acc ← $[TA]_M$

Description: Load the contents of the middle nibble timer/counter A register into the accumulator.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1010 1111 0101

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the register is 0; clear otherwise.
S	The value of the status flag is always 1.

2.49 LDATAH

Operation: Acc ← $[TA]_H$

Description: Load the contents of the high nibble timer/counter A register into the accumulator.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1010 1111 0110

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the register is 0; clear otherwise.
S	The value of the status flag is always 1.

2.50 LDATBL

Operation: Acc ← $[TB]_L$

Description: Load the contents of the low nibble timer/counter B register into the accumulator.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1010 1111 1000

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the register is 0; clear otherwise.
S	The value of the status flag is always 1.

2.51 LDATBM

Operation: Acc ← $[TB]_M$

Description: Load the contents of the middle nibble timer/counter B register into the accumulator.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1010 1111 1001

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the register is 0; clear otherwise.
S	The value of the status flag is always 1.

2.52 LDATBH

Operation: Acc ← $[TB]_H$

Description: Load the contents of the high nibble timer/counter B register into the accumulator.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1010 1111 1010

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the register is 0; clear otherwise.
S	The value of the status flag is always 1.

2.53 LDAX

Operation: Acc ← $ROM[DP]_L$

Description: Load the lower nibble data that reads from the data table of the program memory specified by the data pointer to the accumulator. The range of the data table is address 0000 ~ $07FF_H$ in the 2K ROM chip, 0000 ~ $0FFF_H$ in the 4K ROM chip, and 1000 ~ $1FFF_H$ in the 8K ROM chip.

Code Bytes	Instruction Cycles	Object Code
1	2	0110 0101

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the program memory is 0; clear otherwise.
S	The value of the status flag is always 1.

2.54 LDAXI

Operation: Acc ← ROM[DP]$_H$, DP + 1

Description: Load the higher nibble data that reads from the data table of the program memory specified by the data pointer to the accumulator, and increase the data pointer by one. The range of the data table is address 0000 ~ 07FF$_H$ in the 2K ROM chip, 0000 ~ 0FFF$_H$ in the 4K ROM chip, and 1000 ~ 1FFF$_H$ in the 8K ROM chip.

Code Bytes	Instruction Cycles	Object Code
1	2	0110 0111

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the program memory is 0; clear otherwise.
S	The value of the status flag is always 1.

2.55 LDH #k

Operation: HR ← k

Description: Load the immediate data k into the H register.

Code Bytes	Instruction Cycles	Object Code
1	1	1001 kkkk

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is always 1.

2.56 LDHL x

Operation: LR ← RAM[x], HR ← RAM[x + 1]

Description: Load the contents of the data memory specified by the address x, of which the lower two bits must be zero, into the H and L registers.

Code Bytes	Instruction Cycles	Object Code
2	2	0100 1110 xxxx xx00

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is always 1.

2.57 LDIA #k

Operation: Acc ← k

Description: Load the immediate data k into the accumulator.

Code Bytes	Instruction Cycles	Object Code
1	1	1101 kkkk

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the immediate data is 0; clear otherwise.
S	The value of the status flag is always 1.

2.58 LDL #k

Operation: LR ← k

Description: Load the immediate data k into the L register.

Code Bytes	Instruction Cycles	Object Code
1	1	1000 kkkk

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is always 1.

2.59 NOP

Operation: No operation

Description: No operation.

Code Bytes	Instruction Cycles	Object Code
1	1	0101 0110

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is not changed.

2.60 ORA #k

Operation: Acc ← Acc | k

Description: Logic OR the contents of the accumulator with the immediate data k and place the result in the accumulator.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1110 0100 kkkk

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the accumulator is 0; clear otherwise.
S	Transfer the inverse value of the zero flag to the status flag

2.61 ORAM

Operation: Acc ← Acc | RAM[HL]

Description: Logic OR the contents of the accumulator with the contents of the data memory specified by the H and L registers, and place the result in the accumulator.

Code Bytes	Instruction Cycles	Object Code
1	1	0111 1000

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the accumulator is 0; clear otherwise.
S	Transfer the inverse value of the zero flag to the status flag

2.62 ORM #k

Operation: RAM[HL] ← RAM[HL] | k

Description: Logic OR the contents of the data memory specified by the H and L registers with the immediate data k, and place the result in the data memory.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1110 1100 kkkk

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the data memory is 0; clear otherwise.
S	Transfer the inverse value of the zero flag to the status flag

2.63 OUT #k, p

Operation: PORT[p] ← k

Description: Output the immediate data k to the port p (p = 0 ~ 15).

Code Bytes	Instruction Cycles	Object Code
2	2	0100 1010 kkkk pppp

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is always 1.

2.64 OUTA p

Operation: PORT[p] ← Acc

Description: Output the contents of the accumulator to the port p (p = 0 ~ 31).

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1111 000p pppp

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is always 1.

2.65 OUT12

Operation: PORT[2].PORT[1] ← ROM[$FE0_H$ + CF.RAM[HL]]

Description: Output the 8-bit data in the data conversion table of the program memory to port 2 and port 1 synchronously. The 5-bit data is composed by the contents of the carry flag and the data memory specified by the H and L registers.

CF = 0, P1 = ROM[$07E0_H$ + RAM[HL]]$_L$, P2 = ROM[$07E0_H$ + RAM[HL]]$_H$ in 2K ROM chip.
P1 = ROM[$0FE0_H$ + RAM[HL]]$_L$, P2 = ROM[$0FE0_H$ + RAM[HL]]$_H$ in 4K ROM chip.
P1 = ROM[$1FE0_H$ + RAM[HL]]$_L$, P2 = ROM[$1FE0_H$ + RAM[HL]]$_H$ in 8K ROM chip.

CF = 1, P1 = ROM[$07F0_H$ + RAM[HL]]$_L$, P2 = ROM[$07F0_H$ + RAM[HL]]$_H$ in 2K ROM chip.
P1 = ROM[$0FF0_H$ + RAM[HL]]$_L$, P2 = ROM[$0FF0_H$ + RAM[HL]]$_H$ in 4K ROM chip.
P1 = ROM[$1FF0_H$ + RAM[HL]]$_L$, P2 = ROM[$1FF0_H$ + RAM[HL]]$_H$ in 8K ROM chip.

Code Bytes	Instruction Cycles	Object Code
1	2	0111 0111

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is always 1.

2.66 RET

Operation: SP ← SP + 1, PC ← STACK[SP]

Description: Return from subroutine to the previous program. Increase the stack pointer and restore the data of the return address from the stack (location SP) to the program counter.

Code Bytes	Instruction Cycles	Object Code
1	2	0100 1111

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is not changed.

2.67 RLCA

Operation: ← CF ← Acc ←

Description: Rotate the contents of the carry flag and the accumulator left by one bit.

Code Bytes	Instruction Cycles	Object Code
1	1	0101 0000

Flags

C	Set the carry flag if the highest bit of the accumulator is 1; clear otherwise.
Z	Set the zero flag if the value of the accumulator is 0; clear otherwise.
S	Transfer the inverse value of the carry flag to the status flag.

2.68 RRCA

Operation: → CF → Acc →

Description: Rotate the contents of the carry flag and the accumulator right by one bit.

Code Bytes	Instruction Cycles	Object Code
1	1	0101 0001

Flags

C	Set the carry flag if the lowest bit of the accumulator is 1; clear otherwise.
Z	Set the zero flag if the value of the accumulator is 0; clear otherwise.
S	Transfer the inverse value of the carry flag to the status flag.

2.69 RTI

Operation: SP ← SP + 1, EIF ← 1, FLAG.PC ← STACK[SP]

Description: Return from the interrupt subroutine to the previous program. Increase the stack pointer and restore the data of the return address and flags from the stack (location SP) to the program counter and flags. Set the interrupt enable Flip-Flop to 1.

Code Bytes	Instruction Cycles	Object Code
1	2	0100 1101

Flags

C	The value of the carry flag is specified by this operation.
Z	The value of the zero flag is specified by this operation.
S	The value of the status flag is specified by this operation.

2.70 SBCAM

Operation: Acc ← RAM[HL] - Acc - CF'

Description: Subtract the inverse contents of the carry flag and the contents of the accumulator from the data memory specified by the H and L registers, and place the result in the accumulator.

Code Bytes	Instruction Cycles	Object Code
1	1	0111 0010

Flags

C	Set the carry flag if the accumulator has no borrow for subtraction; clear otherwise.
Z	Set the zero flag if the value of the accumulator is 0; clear otherwise.
S	Transfer the value of the carry flag to the status flag.

2.71 SBR a

Operation: If SF = 1, then PC ← $PC_{12\sim6}.a_{5\sim0}$, else null

Description: If SF equals 1, the program counter branches to the destination address within one page (one page = 64 bytes). The destination address (PC ← $PC_{12\sim6}.a_{5\sim0}$) is specified by the highest seven bits of the program counter concatenated with the lower six bits of the address a. If this instruction specifies the last address of this page ($PC_{5\sim0}$. = 111111_B), the program counter will branch to the next page (PC ← ($PC_{12\sim6}$ + 1).$a_{5\sim0}$). And, if SF = 0 it only sets the SF to 1 and the program counter moves to the next address (PC ← PC + 1).

Code Bytes	Instruction Cycles	Object Code
1	1	00aa aaaa

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is always 1.

2.72 SCALL a

Operation: STACK[SP] ← PC, SP SP - 1, PC a, a = 8n + 6 (n=1~15), a = 0086_H (n=0)

Description: For the short form subroutine call, save the contents of the program counter in the stack (location SP), decrease the stack pointer and place the address a in the program counter. (I.e., a = $00E_H$, 016_H, $01E_H$, 026_H, $02E_H$, 036_H, $03E_H$, 046_H, $04E_H$, 056_H, $05E_H$, 066_H, $06E_H$, 076_H, $07E_H$, 086_H.)

Code Bytes	Instruction Cycles	Object Code
1	2	1110 nnnn

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is not changed.

2.73 SEM b

Operation: RAM[HL] b ← 1

Description: Set the bit b of the data memory specified by the H and L registers to 1.

Code Bytes	Instruction Cycles	Object Code
1	1	1111 01bb

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is always 1.

2.74 SEP p, b

Operation: PORT[p] b ← 1

Description: Set the bit b of the port p (p = 1 ~ 15) to 1.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1101 01bb pppp

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is always 1.

2.75 SEPL

Operation: PORT[$LR_{3\sim2}$ + 4] $LR_{1\sim0} \leftarrow 1$

Description: Set the bit of the port specified by the L register to 1. The bit number is specified by bit 1 ~ bit 0 of the L register, and the port number (P4 ~ P7) is equal to 4 plus bit 3 ~ bit 2 of the L register.

Code Bytes	Instruction Cycles	Object Code
1	2	0110 0010

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is always 1.

2.76 SET y, b

Operation: RAM[y] b ← 1

Description: Set the bit of the data memory specified by the zero page address y (y = 0 ~ $0F_H$) to 1.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1100 01bb yyyy

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is always 1.

2.77 SGF

Operation: GF ← 1

Description: Set the general flag to 1. This instruction cannot apply to the 8K ROM chip.

Code Bytes	Instruction Cycles	Object Code
1	1	0101 0101

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is always 1.

2.78 SLBR a

Operation: If SF = 1, then PC ← $a_{12\sim0}$ else null

Description: If SF equals 1, the program counter branches to the destination address a (PC ← $a_{12\sim0}$) between two banks (one bank = 4K bytes). If SF equals 0, it only sets the status flag to 1 and the program counter moves to the next address (PC ← PC + 3). This instruction only applies to the 8K ROM chip.

Code Bytes	Instruction Cycles	Object Code
3	3	1100 aaaa aaaa aaaa

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is always 1.

2.79 STA x

Operation: RAM[x] ← Acc

Description: Store the contents of the accumulator into the data memory specified by the address x.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1001 xxxx xxxx

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is always 1.

2.80 STADPL

Operation: $[DP]_L$ ← Acc

Description: Store the contents of the accumulator into the low nibble of the data pointer register.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1001 1111 1100

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is always 1.

2.81 STADPM

Operation: $[DP]_M \leftarrow Acc$

Description: Store the contents of the accumulator into the middle nibble of the data pointer register.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1001 1111 1101

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is always 1.

2.82 STADPH

Operation: $[DP]_H \leftarrow Acc$

Description: Store the contents of the accumulator into the high nibble of the data pointer register.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1001 1111 1110

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is always 1.

2.83 STAM

Operation: RAM[HL] ← Acc

Description: Store the contents of the accumulator into the data memory specified by the H and L registers.

Code Bytes	Instruction Cycles	Object Code
1	1	0101 1001

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is always 1.

2.84 STAMD

Operation: RAM[HL] ← Acc, LR - 1

Description: Store the contents of the accumulator into the data memory specified by the H and L registers, and decrease the contents of the L register by 1.

Code Bytes	Instruction Cycles	Object Code
1	1	0111 1101

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the accumulator is 0; clear otherwise.
S	Transfer the value of the carry flag to the status flag.

2.85 STAMI

Operation: RAM[HL] ← Acc, LR + 1

Description: Store the contents of the accumulator into the data memory specified by the H and L registers, and increase the contents of the L register by 1.

Code Bytes	Instruction Cycles	Object Code
1	1	0111 1111

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the accumulator is 0; clear otherwise.
S	Transfer the inverse value of the carry flag to the status flag.

2.86 STASP

Operation: SP ← Acc

Description: Store the contents of the accumulator into the stack pointer.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1001 1111 1111

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is always 1.

2.87 STATAL

Operation: $[TA]_L \leftarrow Acc$

Description: Store the contents of the accumulator into the low nibble of the timer/counter A register.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1001 1111 0100

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is always 1.

2.88 STATAM

Operation: $[TA]_M \leftarrow Acc$

Description: Store the contents of the accumulator into the middle nibble of the timer/counter A register.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1001 1111 0101

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is always 1.

2.89 STATAH

Operation: $[TA]_H \leftarrow Acc$

Description: Store the contents of the accumulator into the high nibble of the timer/counter A register.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1001 1111 0110

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is always 1.

2.90 STATBL

Operation: $[TB]_L \leftarrow Acc$

Description: Store the contents of the accumulator into the low nibble of the timer/counter B register.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1001 1111 1000

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is always 1.

2.91 STATBM

Operation: $[TB]_M \leftarrow Acc$

Description: Store the contents of the accumulator into the middle nibble of the timer/counter B register.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1001 1111 1001

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is always 1.

2.92 STATBH

Operation: $[TB]_H \leftarrow Acc$

Description: Store the contents of the accumulator into the high nibble of the timer/counter B register.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1001 1111 1010

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is always 1.

2.93 STD #k, y

Operation: RAM[y] ← k

Description: Store the immediate data k into the data memory specified by the zero page address y (y = 0 ~ $0F_H$).

Code Bytes	Instruction Cycles	Object Code
2	2	0100 1000 kkkk yyyy

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is always 1.

2.94 STDMI #k

Operation: RAM[HL] ← k, LR + 1

Description: Store the immediate data k into the data memory specified by the H and L registers, and increase the contents of the L register by 1.

Code Bytes	Instruction Cycles	Object Code
1	1	1010 kkkk

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the immediate data k is 0; clear otherwise.
S	Transfer the inverse value of the carry flag to the status flag.

2.95 SUBA #k

Operation: Acc ← k - Acc

Description: Subtract the contents of the accumulator from the immediate data k and place the result in the accumulator.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1110 0111 kkkk

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the accumulator is 0; clear otherwise.
S	Transfer the value of the carry flag to the status flag.

2.96 SUBM #k

Operation: RAM[HL] ← k - RAM[HL]

Description: Subtract the contents of the data memory specified by the H and L registers from the immediate data k, and place the result in the data memory.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1110 1111 kkkk

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the data memory is 0; clear otherwise.
S	Transfer the value of the carry flag to the status flag.

2.97 TFA b

Operation: SF ← Acc b'

Description: Place the inverse contents of the bit b of the accumulator into the status flag.

Code Bytes	Instruction Cycles	Object Code
1	1	1111 10bb

Flags

C	The value of the carry flag is not changed
Z	The value of the zero flag is not changed.
S	The value of the status flag is specified by this operation.

2.98 TFCFC

Operation: SF ← CF', CF ← 0

Description: Place the inverse contents of the carry flag into the status flag, then clear the carry flag to 0.

Code Bytes	Instruction Cycles	Object Code
1	1	0101 0011

Flags

C	The value of the carry flag is always 0.
Z	The value of the zero flag is not changed.
S	The value of the status flag is specified by this operation.

2.99 TFM b

Operation: SF ← RAM[HL] b'

Description: Place the inverse contents of the bit b of the data memory specified by the H and L registers into the status flag.

Code Bytes	Instruction Cycles	Object Code
1	1	1111 11bb

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is specified by this operation.

2.100 TFP p, b

Operation: SF ← PORT[p] b'

Description: Place the inverse contents of the bit b of the port p (p = 0 ~ 15) into the status flag.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1101 00bb pppp

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is specified by this operation.

2.101 TFPL

Operation: SF ← PORT[$LR_{3\sim2}$ + 4] $LR_{1\sim0}$'

Description: Place the inverse contents of the bit b of the port p specified by the L register into the status flag. The bit number is specified by bit 1 ~ bit 0 of the L register, and the port number (P4 ~ P7) is equal to 4 plus bit 3 ~ bit 2 of the L register.

Code Bytes	Instruction Cycles	Object Code
1	2	0110 0001

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is specified by this operation.

2.102 TGS

Operation: SF ← GF

Description: Place the contents of the general flag into the status flag. This instruction cannot apply to the 8K ROM chip.

Code Bytes	Instruction Cycles	Object Code
1	1	0101 0100

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is specified by this operation.

2.103 THA

Operation: Acc ← HR

Description: Place the contents of the H register into the accumulator.

Code Bytes	Instruction Cycles	Object Code
1	1	0111 0110

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the H register is 0; clear otherwise
S	The value of the status flag is always 1.

2.104 TLA

Operation: Acc ← LR

Description: Place the contents of the L register into the accumulator.

Code Bytes	Instruction Cycles	Object Code
1	1	0111 0100

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the L register is 0; clear otherwise
S	The value of the status flag is always 1.

2.105 TT y, b

Operation: SF ← RAM[y] b

Description: Place the contents of the bit b of the data memory specified by the zero page address y (y = 0 ~ $0F_H$) into the status flag.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1100 10bb yyyy

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is specified by this operation.

2.106 TTCFS

Operation: SF ← CF, CF ← 1

Description: Place the contents of the carry flag into the status flag, then set the carry flag to 1.

Code Bytes	Instruction Cycles	Object Code
1	1	0101 0010

Flags

C	The value of the carry flag is always 1.
Z	The value of the zero flag is not changed.
S	The value of the status flag is specified by this operation.

2.107 TTP p, b

Operation: SF ← PORT[p] b

Description: Place the contents of the bit b of the port p (p = 0 ~ 15) into the status flag.

Code Bytes	Instruction Cycles	Object Code
2	2	0110 1101 10bb pppp

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is specified by this operation.

2.108 TZS

Operation: SF ← ZF

Description: Place the contents of the zero flag into the status flag.

Code Bytes	Instruction Cycles	Object Code
1	1	0101 1011

Flags

C	The value of the carry flag is not changed.
Z	The value of the zero flag is not changed.
S	The value of the status flag is specified by this operation.

2.109 XORAM

Operation: Acc ← Acc ^ RAM[HL]

Description: Logic XOR the contents of the accumulator with the contents of the data memory specified by the H and L registers and place the result in the accumulator.

Code Bytes	Instruction Cycles	Object Code
1	1	0111 1001

Flags

C	The value of the carry flag is not changed.
Z	Set the zero flag if the value of the accumulator is 0; clear otherwise
S	Transfer the inverse value of the zero flag to the status flag.