CH9203 Dual Programmable Clock Generator

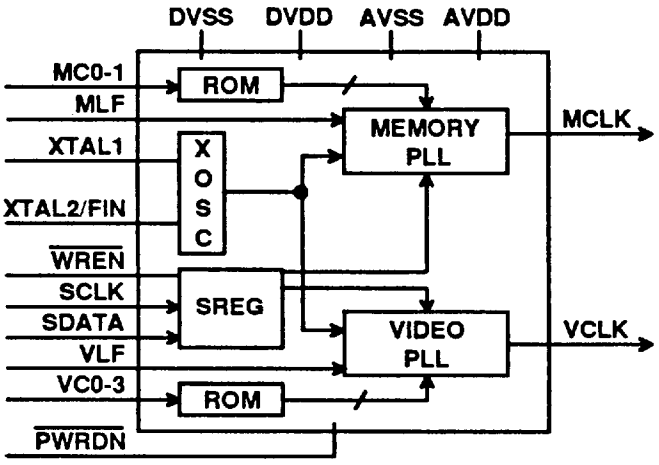
Features

- 16 Video Clock frequencies and 4 Memory Clock frequencies
- Supports output frequencies up to 130 MHz
- Draws less than 1 µA in Power Down mode
- Only four external components needed - one 14.318 MHz crystal and three capacitors
- Backward pin compatible with CH920X series and ICS1394 (same basic pinout)
- Supports graphics standards such as EGA, VGA, SuperVGA, XGA, and 8514A
- High performance, low power CMOS technology
- Available in 20 pin plastic DIP or SOIC
- User customized frequency options available
- Proprietary VCO design for low phase jitter
- 5V and 3.3V supply

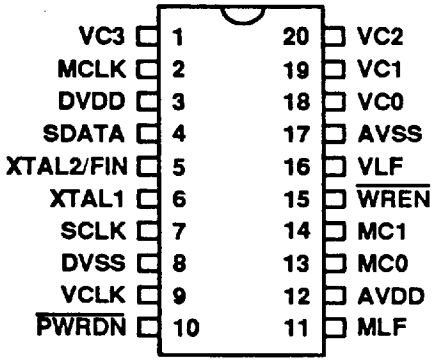
Description

The Chrontel CH9203 is a dual phase-locked loop frequency synthesizer designed for low power and high performance applications, such as graphics systems based on the VGA, SuperVGA, XGA and 8514A formats. The CH9203 has a Power Down mode in which it typically draws less than 1 µA of supply current, making it ideal for notebook, palmtop, and other portable applications. It is also well-suited for use in other applications that require multiple clocks, such as disk drives, CD-ROM systems, FAX-modems, etc.

When used in the latest generation of high performance graphics controllers, the CH9203 provides separate memory (MCLK) and video (VCLK) clocks. The minimum and maximum frequencies of both clock outputs can be as low as 8 MHz, and as high as 130 MHz, respectively. The reference frequency is 14.318 MHz, which can be derived from either a crystal or an external reference frequency. Other input frequencies can be used to obtain non-standard output frequencies.



BLOCK DIAGRAM



PINOUT DIAGRAM

Power Down Mode

When power down is active (logic low), the CH9203 is placed in a standby mode. All outputs are tristated and both internal PLLs are disabled to minimize power consumption. In this mode, CH9203 uses less than 1 μA of current. After power up, CH9203 typically requires 40 milliseconds for the PLLs to stabilize.

Variable Output Drive Current

For output frequencies less than 50 MHz, the output source current is typically 4.0 mA and the sink current is 6.0 mA. When the output frequency is higher than 50 MHz, the output source and sink currents automatically increase to 6.0 mA and 8.0 mA respectively. This feature adjusts the output rise and fall times for different applications. In some cases, fast rise and fall times may cause excessive electro-magnetic interference.

CH9203's Advantages and Compatibility to the CH9201/ICS1394

The pinout diagrams of Chrontel's CH920X-series frequency synthesizers are based on those of the CH9201/ICS1394. If a board was originally designed for CH9201 or ICS1394, only minor changes are required in the board layout to upgrade to CH9203. The changes are the following:

1. Instead of using a separate oscillator for the memory clock (MCLK) of the VGA controller, CH9203 provides the MCLK output at pin 2.
2. AVDD of CH9203 can be connected directly to the 5V supply, eliminating the Zener diode used in the CH9201/ICS1394 design. This further reduces power consumption.
3. Optional MC0-MC1 jumpers may be required for proper MCLK frequency selection. The MCLK frequency defaults to 60 MHz if MC0-MC1 are left open (internal pull-up).
4. 0.1 μF capacitors are needed between pin 11 and pin 12 for the memory loop filter, and between pin 16 and 12 for the video loop filter.
5. WREN*, SDATA and SCLK can be used to serially program CH9203

CH9203 Frequency Tables (Version L shown below)

Video Clock

VC3	VC2	VC1	VC0	VCLK (MHz)
0	0	0	0	25.175
0	0	0	1	28.322
0	0	1	0	40.0
0	0	1	1	Serial Prog.
0	1	0	0	50.0
0	1	0	1	77.0
0	1	1	0	36.0
0	1	1	1	44.9
1	0	0	0	130.0
1	0	0	1	120.0
1	0	1	0	80.0
1	0	1	1	31.5
1	1	0	0	110.0
1	1	0	1	65.0
1	1	1	0	75.0
1	1	1	1	94.5

Please contact Chrontel for exact output frequencies and custom frequency tables.

Memory Clock

MC1	MC0	MCLK (MHz)
0	0	50.0
0	1	55.0
1	0	Serial Prog.
1	1	60.0

Pin Description

Pin	Type	Symbol	Description
1, 18-20	In	VC3, VC0-VC2	Video clock select (internal pull-up)
2	Out	MCLK	Memory clock output
3	Power	DVDD	Digital 5V supply
4	In	SDATA	Serial data input (internal pull-up)
5	Out/In	XTAL2 / FIN	Crystal output/external FREF input
6	In	XTAL1	Crystal input
7	In	SCLK	Serial clock input (positive edge triggered, internal pull-down)
8	Power	DVSS	Digital ground
9	Out	VCLK	Video clock output
10	In	PD*	Power down input (active low)
11	In	MLF	Memory PLL filter
12	Power	AVDD	Analog 5V supply
13, 14	In	MC0, MC1	Memory clock select (internal pull-up)
15	In	WREN*	Serial data write enable (active low, internal pull-up)
16	In	VLF	Video PLL filter
17	Power	AVSS	Analog ground

DC Specifications (T_A = 0°C – 70°C, V_{DD} = 5V ±5%)

Symbol	Description	Test Condition @T_A=25°C	Min	Typ	Max	Unit
V_{OH}	Output high voltage	V_{DD}=4.75V, I_{OH}=4mA	2.4			V
V_{OL}	Output low voltage	V_{DD}=4.75V, I_{OL}=8mA			0.4	V
V_{IH}	Input high voltage		2.0			V
V_{IL}	Input low voltage				0.8	V
I_{PU}	Input pull-up current			5	20	µA
I_L	Input leakage current		–10		10	µA
I_{STBY}	Standby current	PD* = low			1	µA
I_{DD}	Operating current	V_{CLK}=50MHz, M_{CLK}=55MHz, V_{DD}=5.0V		45		mA

AC Specifications (T_A = 0°C – 70°C, V_{DD} = 5V ±5%)

Symbol	Description	Test Condition @T_A=25°C	Min	Typ	Max	Unit
F_{IN}	Crystal/F_{REF} input			14.318		MHz
V_{CLK}	Video clock frequency		8		130	MHz*
M_{CLK}	Memory clock frequency		8		130	MHz*
T_R, T_F	Output clock rise/fall time	C_L=25pF, V_{OL} – V_{OH}		2		ns
T_{DC}	Output clock duty cycle	@V_{DD}/2, V_{DD}=5.0V	40	50	60	%

Note: * Output levels are guaranteed up to 90 MHz. Please consult Chrontel for suggested circuit implementations for frequencies higher than 90 MHz.

Absolute Maximum Ratings

Symbol	Description	Value	Unit
V_{DD}	Power supply voltage with respect to Vss	–0.5 to +7.0	V
V_{IN}	Input voltage on any pins with respect to Vss	–0.5 to V_{DD}+0.5	V
TSTOR	Storage temperature	–55 to +150	°C

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions above those indicated under parametric values of the DC or AC Specifications below is not recommended or guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Serial Interface Specifications

The serial interface requires a 19-bit data stream containing coefficients for the three programmable counters in each PLL synthesizer and three control signals:

1. A 1-bit control signal (S) to select either the VCLK or the MCLK register
2. A 1-bit control signal (T) for factory use only, should be set to zero for normal operations
3. An 8-bit binary value (N) for the feedback frequency divider
4. A 1-bit control signal (D) to select output driving capability
5. A 2-bit value (O) for the output divider
6. A 6-bit binary value (M) for the reference frequency divider
7. $F_{OUT} = [(N + 8) / (M + 2) \times F_{REF}] / O$
   Note: Some combinations of N and M are not valid; please consult Chrontel for more information

Bit Definitions

Bit 18-13 A 6-bit reference frequency divider (M) where b18 = MSB, b13 = LSB

Bit 21-11 A 2-bit output divider (O)

b12	b11	Definition
0	0	No divide (divide by 1)
0	1	Divide by 2
1	0	Divide by 4
1	1	Divide by 8

Bit 10 Output current drive (D)
0 : high sink and source current capabilities
1 : low sink and source current capabilities

Bits 9-2 An 8-bit feedback counter (N) b9 = MSB and b2 = LSB

Bit 1 (T) should be always set to zero

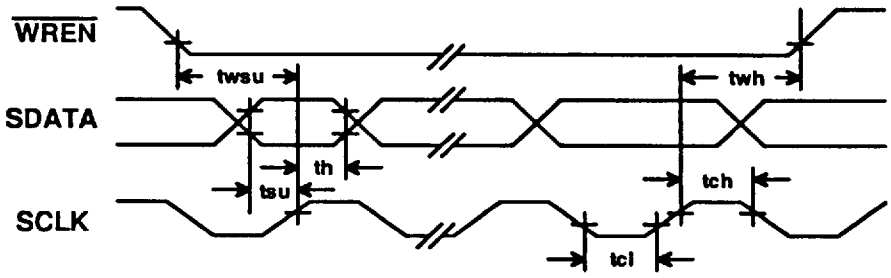
Bit 0 Programming register select (S)
0 : Video clock programming register
1 : Memory clock programming register

18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
M	M	M	M	M	M	O	O	D	N	N	N	N	N	N	N	N	T	S	→

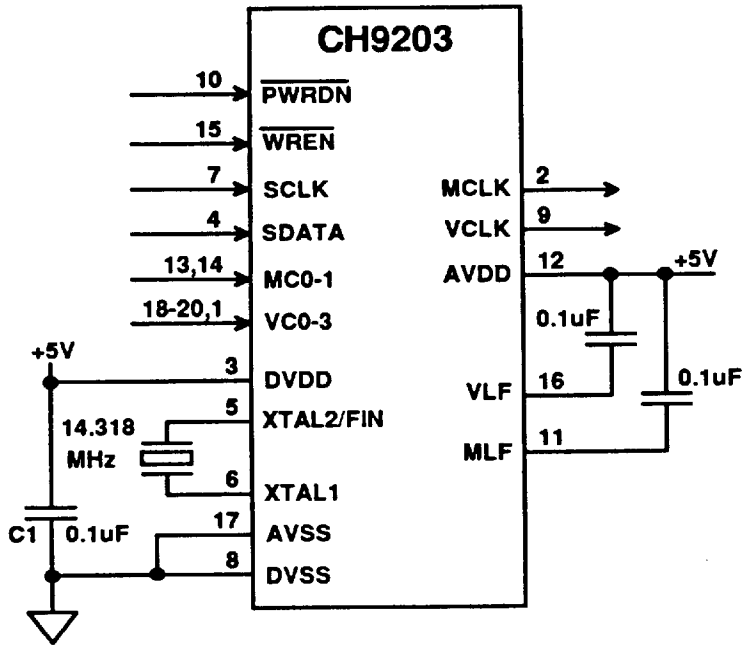
→ Bit 00 is the first bit to be shifted in.

Serial Interface Timing

Symbol	Description	Min	Type	Max	Unit
tsu	Serial data setup time	20			ns
th	Serial data hold time	20			ns
twsu	Write enable setup time	30			ns
twh	Write enable hold time	30			ns
tcl	SCLK low pulse width	20			ns
tch	SCLK high pulse width	20			ns



SERIAL INTERFACE TIMING DIAGRAM



CH9203 APPLICATION SCHEMATIC

Note:
C1 should be placed in close proximity to the power pins

ORDERING INFORMATION	
Part Number	Package Type
CH9203Cx-NC	300 mil PDIP
CH9203Cx-SC	300 mil SOIC
Note: x = Frequency table version	

For the location of the sales office nearest you, contact:

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