T-75-33-05

MATRA-HARRIS SEMICONDUCTOR

data sheet

HC-5570

300 BAUDS MODEM

PRELIMINARY

JANUARY 1987

Features

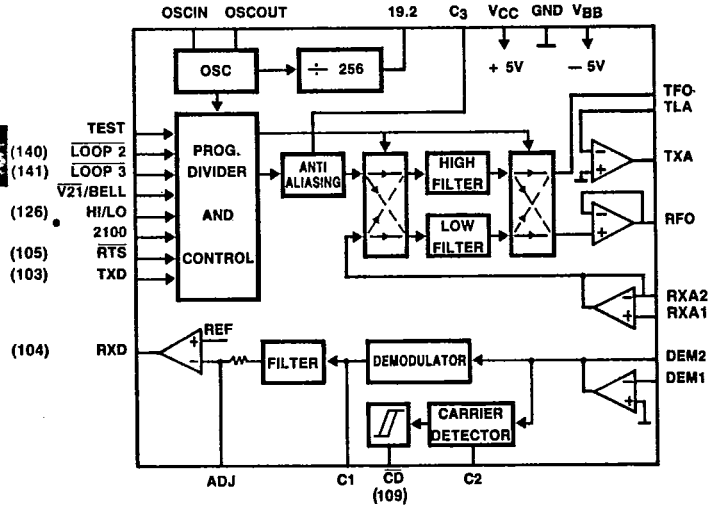
- CCITT V21 AND BELL 103 COMPATIBLE
- +/— 5V SUPPLIES
- FULL DUPLEX ANSWER OR ORIGINATE OPERATION
- QUARTZ REFERENCE: 4.9152 MHz
- HIGH PERFORMANCE CORRELATION DEMODULATOR
- HIGH INPUT RANGE: 0 TO —48 dBm
- ADJUSTABLE OUTPUT RANGE: —1 TO —15 dBm
- CARRIER FREQUENCY PRECISION: +/— 3 Hz
- CARRIER DETECT OUTPUT
- 2 LOOPBACK TEST MODES
- 2100 Hz TONE GENERATION
- UART CLOCK GENERATION (19.2 KHz).

Description

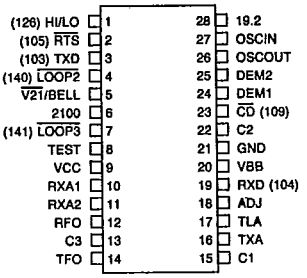
The HC-5570 is a full duplex 300 bauds modem. It can receive and transmit according to CCITT V21 or BELL 103 standards through a single pin programming. The transmit and receive channels (high or low) can also be programmed.

The modulator produces a phase coherent frequency shift keyed (FSK) output. The receive section consists of an anti-aliasing RC filter followed by a 12th order filter to reject the transmit channel components. The demodulator performs an auto-correlation of the received signal to guarantee an excellent behaviour in noisy environments.

Functional Diagram



Pin Configuration



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HC-5570

Pin Description

PIN N°	NAME	FUNCTION
1	HI/LO (126)	This input makes the high or low channel selection for the transmit and receive sections. HI/LO | Tx | Rx 0 | HIGH | LOW 1 | LOW | HIGH
2	$\overline{\text{RTS}}$ (105)	Request to send : this input is active low and enables data transmission.
3	TXD (103)	Transmitted data : this is the data input.
4	$\overline{\text{LOOP 2}}$ (140)	Digital loopback : when this input is low, the received data are sent back on the line. The transmission is enabled by the carrier detector output instead of $\overline{\text{RTS}}$.
5	$\overline{\text{V21}}$/BELL	If this input is tied to ground, V21 standard is selected. BELL 103 is selected when tied to a logic 1.
6	2100	Generation of a 2100 Hz tone signal when this input is connected to a high level.
7	$\overline{\text{LOOP 3}}$ (141)	Analog loopback : when this input is low, the analog transmit signal is looped back on the receive section and demodulated.
8	TEST	Should be left open in normal use.
9	Vcc	Positive supply pin . 5V +/— 5 %
10	RXA1	Receive Analog 1 : input of the unity-gain receive amplifier.
11	RXA2	Receive Analog 2 : output of the unity-gain receive amplifier.
12	RFO	Receive Filter Output.
13	C3	An external capacitor C3 should be connected to this pin for anti-aliasing.
14	TFO	Transmit Filter Output.
15	C1	Capacitor C1 is used to integrate the demodulated signal.
16	TXA	Transmit Analog : output of the line driver.
17	TLA	Transmit Level Adjust : inverting input of the analog transmit amplifier. The gain of this amplifier is set via 2 external resistors connected to pins TFO, TLA and TXA.
18	ADJ	Adjustment of the DC component of the demodulated signal. Can be used to optimize the detector performance.
19	RXD	Receive Data : This is the data output pin.
20	VBB	Negative supply pin : — 5V +/ — 5 %
21	GND	Ground : all signals are referenced to this pin.
22	C2	Capacitor C2 sets the time constant of the carrier detect circuit.
23	$\overline{\text{CD}}$	Carrier Detect output. This output becomes low when a carrier is detected on the receive channel.
24	DEM1	Inverting input of the demodulator amplifier.
25	DEM2	Output of the demodulator amplifier.
26	OSCOUT	Output of the inverter used for clock generation. A 4.9152 MHz quartz reference should be connected between OSCIN and OSCOUT.
27	OSCIN	Input of the oscillator inverter (see pin 26). An external clock can drive this pin directly.
28	19.2	This output provides a 19.2 KHz square wave that can be used for a UART.

HC-5570

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Functional description

INTRODUCTION

The HC 5570 is able to transmit and receive data simultaneously at a rate comprised between 0 and 300 bps. The modulation used for transmission is frequency shift keying (FSK) of an audio frequency tone according to the logic state of the input TXD (transmit data).

At the same time, the modem is able to demodulate the FSK signal present on the receive channel. Sharp filters are used to separate transmit from receive frequency bands, and a complex signal processing is performed to discriminate the receive frequencies.

This modem can work either with V21 or BELL 103 standards. The frequency allocations for both standards are indicated in table 1 :

DATA	V21		BELL 103	
	LOW	HIGH	LOW	HIGH
0	1180	1850	1070	2025
1	980	1650	1270	2225

Table 1 : Frequency Allocations

RTS	2100	V21/BELL	HI/LO	TXD	STANDARD frequency (Hz)	DEVIATION from standard (Hz)
0	0	0 (V21)	1 (LOW)	1	980	— 1.3
				0	1180	+ 2.1
			0 (HIGH)	1	1650	+ 1.6
				0	1850	+ 0.6
		1 (BELL 103)	1 (LOW)	1	1270	— 1.9
				0	1070	— 1.0
			0 (HIGH)	1	2225	+ 1.1
				0	2025	+ 2.7
	1	X	X	X	2100	+ 0.5
1	NO OUTPUT SIGNAL					

Table 2 : Modulator Truth table

MODULATOR

The basic element used for the modulation is a programmable divider. The oscillator frequency (4.9152 MHz) is divided by an integer number depending from the standard (V21 or BELL 103), from the channel selection (high or low), and from the logic state of the TXD input.

The frequencies are all within 3Hz of the theoretical value. The table 2 gives the truth table of the modulator .

A 2100 Hz signal can be generated with both standards by activating the 2100 input, independently of the HI/LO and TXD status. However $\overline{RTS}$ must be low to enable the 2100 Hz generation. This frequency is used to inhibit the echo suppressors for full duplex communication.

The square wave is followed by a 12th order switched capacitor filter. The high filter or low filter is selected depending of the HI/LO choice. Each filter bandwidth is adjusted according to the selected standard (V21 or BELL 103). This translation is achieved by shifting internally the clocking frequency of the switched capacitor array.

The output amplifier is used to set the transmit level and as an active filter to reject the sampling frequency (about 40KHz).

RECEIVE SECTION

The received signal goes first through a unity gain amplifier. A second order Sallen-key filter can be easily built around this amplifier to achieve an efficient anti-aliasing.

The output of this amplifier is connected to the 12th order high or low filter, (see modulator description), to eliminate all the components which are outside the receive band.

The receive filter is followed by a unity gain buffer and the resulting analog signal is available at the RFO output.

DEMODULATOR

An additional amplifier (inverting input = DEM1 ; output = DEM2) allows adjustable amplification and adequate smoothing of the receive filter output signal.

The demodulator performs an auto-correlation of the received signal. The squared waveform is connected to an exclusive OR whose second input receives the same signal delayed through a shift register. The length of this register depends from the selected channel and from the transmission standard. The consequence of this fixed delay is that the mean value of the signal at the output of the exclusive OR is different for the 2 frequencies to be decoded, for example 980 Hz and 1180 Hz. This waveform is integrated first through a simple RC (antialiasing) and then through a 4th order switched capacitor filter. A comparator finally restores the serial data flow on the RXD pin.

The average value of the signal at the input of the comparator can be altered externally through an adjustable resistor connected to pin ADJ. This arrangement allows for greater sensitivity and optimum performance.

CARRIER DETECTION

A peak detector is used, followed by a Trigger circuit to avoid unstable detection at low level. The hysteresis of the detector is typically 3dB. An external capacitor C2 is required to set the carrier detect circuit timing. The $\overline{CD}$ pin is active low.

UART CLOCK

This clock is directly obtained by dividing by 256 the oscillator frequency and gives a 19.2 KHz signal to synchronize a UART.

LOOPBACK

2 loopback modes are possible for testing and evaluation purposes :

- Digital Loopback.
  When pin $\overline{LOOP2}$ is connected to ground, the data received on pin RXD are sent back to the modulator. The transmission is enabled by the carrier detect ($\overline{CD}$) output instead of $\overline{RTS}$. The quality of the telephone line can thus be tested.

- Analog loopback.
  When pin $\overline{LOOP3}$ is connected to ground, the modulator works on the high channel. After going through the high filter, the signal passes through the low filter, which has been translated on the high channel. It is then demodulated and the data are reproduced on the RXD output. In that mode, the inputs RXA1 and RXA2 are disabled and no signal is sent on TXA. This test mode is used to check the correct operation of the modulator, demodulator and filters.

Electrical specifications

ABSOLUTE MAXIMUM RATINGS

Vcc to GND ..... — 0.3V to 7V
VBB to GND ..... + 0.3V to — 7V

Voltage at any digital input or output	Vcc + 0.3V to GND — 0.3V
Voltage at any analog input or output	Vcc + 0.3V to VBB — 0.3V
Operating temperature range	— 25°C to 80°C
Storage temperature range	— 65°C to 150°C
Lead temperature (soldering 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS

Unless otherwise noted : Vcc = 5.0V +/— 5 %, VBB = — 5V +/— 5 %, GND = OV, TA = 0°C to 70°C, typical characteristics specified at Vcc = 5.0V, VBB = — 5.0V, TA = 25°C ; all signals are referenced to GND
Fo = 4.9152 MHz +/— 10^{-4}

DIGITAL INPUTS (TXD, $\overline{RTS}$, 2100, HI/LO, V21/BELL, $\overline{LOOP2}$, $\overline{LOOP3}$)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage		2			V
I_{IL}	Input current pull-up	Vin = 0V	— 200			μA

DIGITAL OUTPUT (RXD, 19.2, $\overline{CD}$)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OL}	Output low voltage	IL = 500 μA			0.4	V
V_{OH}	Output high voltage	IL = —500 μA	3			V

POWER DISSIPATION

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Icc	Positive supply current	no load on outputs		16		mA
I_{BB}	Negative supply current	no load on outputs		12		mA

TRANSMIT OUTPUT AMPLIFIER

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OTXA}	Maximum output level	R_L = 10 KΩ	5	5.5	6	dBm

CARRIER DETECTOR

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
T_H—T_L	Hysteresis	Input amplifier gain = 0dB	2	3	5	dB
T_L	Threshold (low) of the detector	Input amplifier gain = 0db	— 5			dBm

Transmission characteristics - High channel

Unless otherwise specified : TA = 25°C, VCC = 5.0V +/— 5 %, VBB = — 5V +/— 5 %, VIN = OdBm applied to pin RXA1, pins LOOP2 and LOOP3 connected to VCC.

HIGH CHANNEL TRANSFER CHARACTERISTICS (CCITT V21)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
G HVR	Gain relative to gain at 1750Hz	f = 0—1280Hz f = 1550—1950Hz f = 3200—4000Hz	— 2		— 65 — 40	dB dB dB

HIGH CHANNEL TRANSFER CHARACTERISTICS (BELL 103)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
G HBR	Gain relative to gain at 2125Hz	f = 0—1370Hz f = 1925—2325Hz f = 3200—4000Hz	— 2		— 65 — 40	dB dB dB

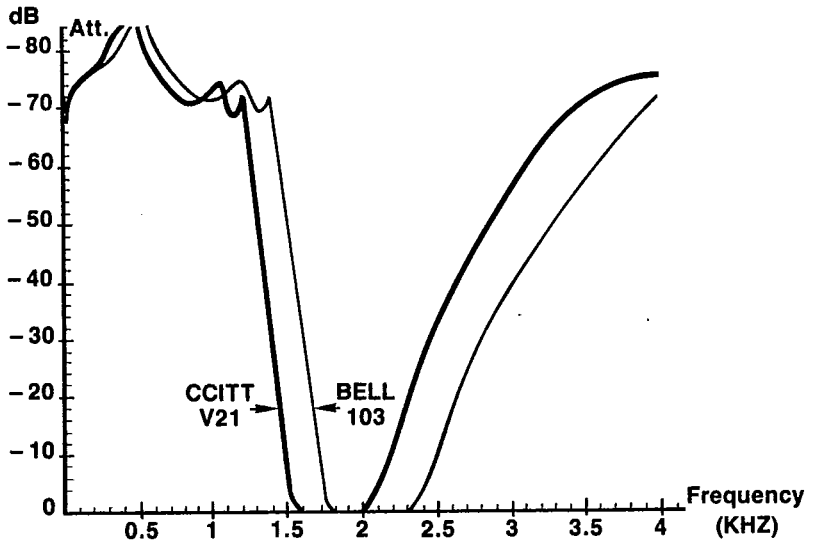

FIG. 1 : HIGH CHANNEL FILTER

Transmission characteristics - Low channel

Unless otherwise specified : TA = 25°C, VCC = 5.0V +/— 5 %, VBB = — 5V +/— 5 %, VIN = OdBm applied to pin RXA1, pins $\overline{LOOP2}$ and $\overline{LOOP3}$ connected to VCC.

LOW CHANNEL TRANSFER CHARACTERISTICS (CCITT V21)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
G_{LVR}	Gain relative to gain at 1080Hz	f = 0— 440Hz f = 880—1280Hz f = 1550—1950Hz f = 1950—4000Hz	— 2		— 40 — 65 — 60	dB dB dB dB

LOW CHANNEL TRANSFER CHARACTERISTICS (BELL 103)

SYMBOL	PARAMETER	CONDITIONS	MIN	TY	MAX	UNITS
G_{LBR}	Gain relative to gain at 1170Hz	f = 0— 440Hz f = 970—1370Hz f = 1925—2325Hz f = 2325—4000Hz	— 2		— 40 — 65 — 60	dB dB dB dB

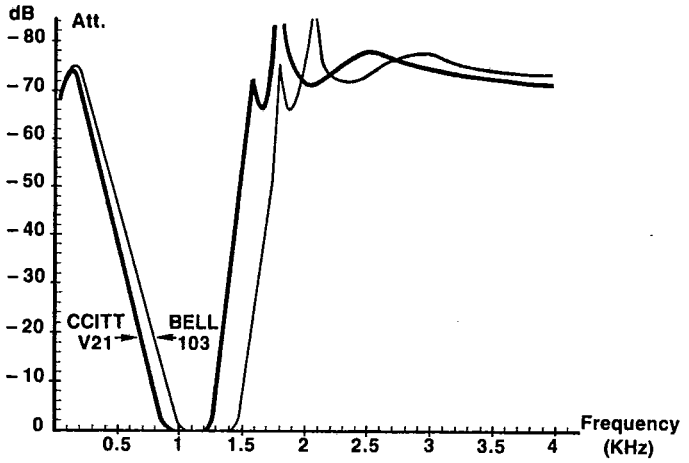

FIG. 2 : LOW CHANNEL FILTER

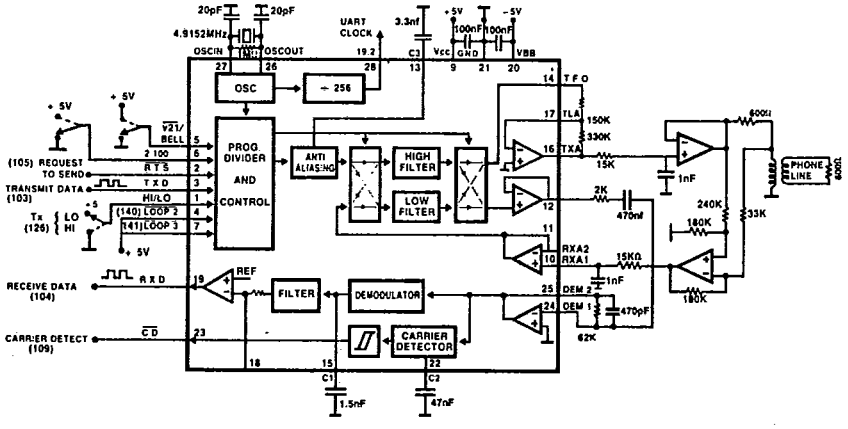

FIG. 3 : TYPICAL APPLICATION