SIEMENS

FM-Transmitter

PMB 2230

Preliminary Data

Bipolar IC

Features

- Reduced external components
- High decoupling of RF VCO from entire chip
- Balanced RF VCO and transmit VCO for high common mode rejection
- High decoupling of RF VCO and transmit VCO and transmit mixer
- High decoupling of PLL-output frequency from RF VCO
- Very small residual and SSB-phase noise of transmit VCO and RF VCO
- Low-noise, internal reference voltage
- Reduced shielding demands
- High common mode rejection against interfering signals due to balanced design

P-DSO-24-S

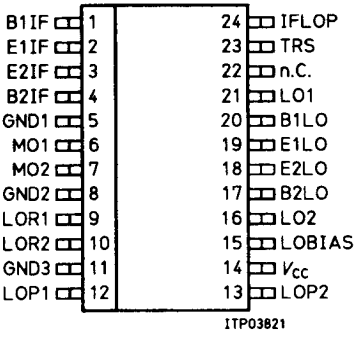
Type	Ordering Code	Package
PMB 2230-S	Q67006 -A6047	P-DSO-24-4 (S) (SMD) (Tape & Reel)

The PMB 2230 is a FM-transmitter with main VCO, transmit VCO and isolation amplifiers.

The chip is a monolithic integrated circuit for use in analog FM-mobile radio systems e.g. AMPS, NMT and cordless FM telephones.

The device contains a colpitts configuration based RF VCO and transmit VCO.
In the transmit mode the transmit mixer is driven by the two VCO-signals. At the output of the mixer the upper and lower sideband have the same level.
During receive mode the transmit VCO and – mixer are switched off with a voltage < 2.5 V at TRS pin.

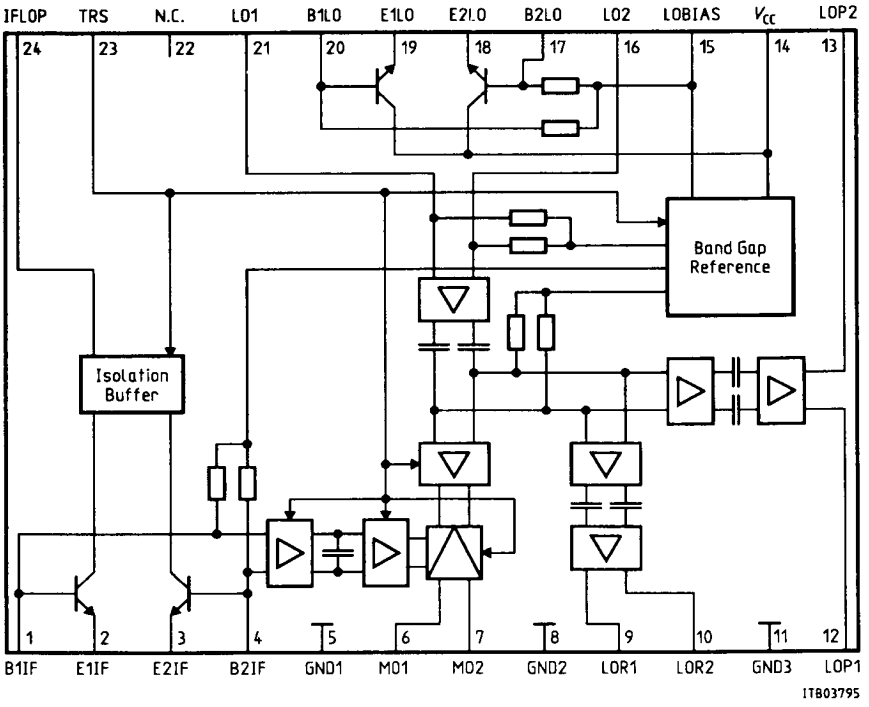
Two integrated isolation buffer fed the RF VCO signal to the receiver chip and a PLL.
The transmit VCO signal is also available at pin IFLOP to drive a PLL.



Pin Configuration
(top view)

Pin Definitions and Functions

Pin No.	Symbol	Function
1	B1IF	Base input 1 of transmit VCO
2	E1IF	Emitter output 1 of transmit VCO
3	E2IF	Emitter output 2 of transmit VCO
4	B2IF	Base input 2 of transmit VCO
5	GND1	Ground for chip
6	MO1	Collector output 1 of transmit mixer
7	MO2	Collector output 2 of transmit mixer
8	GND2	Ground for chip
9	LOR1	LO-output 1 to receiver
10	LOR2	LO-output 2 to receiver
11	GND3	Ground for chip
12	LOP1	LO-output 1 to prescaler
13	LOP2	LO-output 2 to prescaler
14	V_{CC}	Power supply for chip
15	LOBIAS	Bias voltage for RF VCO
16	LO2	LO-input 2 of mixer and isolation buffer
17	B2LO	Base input 2 of RF VCO
18	E2LO	Emitter output 2 of RF VCO
19	E1LO	Emitter output 1 of RF VCO
20	B1LO	Base input 1 of RF VCO
21	LO1	LO-input 1 of mixer and isolation buffer
22	n.C.	
23	TRS	Input for transmit and receive mode switching
24	IFLOP	Transmit VCO-output to PLL



Block Diagram

Circuit Description

Transmit VCO

This oscillator is based on a symmetrical colpitts configuration. The oscillator current is determined by resistors to ground at pins E1IF and E2IF. A tank circuit has to be connected between the bases B1IF and B2IF to determine the oscillator frequency. Frequency tuning can be done with a external varactor diode BB 814 in parallel to the tank circuit.
The VCO-signal is available at pin IFLOP to drive the prescaler of a PLL-circuit.

RF VCO

The RF VCO is also a symmetrical colpitts oscillator type. The oscillator current is determined by resistors to ground at pins E1LO and E2LO. The oscillator frequency is determined by ceramic resonators which are coupled to the transistor bases at pin B1LO and B2LO. A varactor diode in parallel to the resonators provides frequency tuning.
The VCO-signal is fed to the chip through parasitic coupling of pin LO1 with pin B1LO and pin LO2 with pin B2IO. Two isolation buffers are driven with the oscillator signal at pin LO1 and LO2. The one provides the LO signal for the receiver chip at pin LOR1 and LOR2, the other drives the prescaler of a PLL at pin LOP1 and LOP2.
The RF VCO is active in transmit mode as well as in receive mode.

Isolation Buffers

The two isolation buffers for the RF VCO-signal have a common input at pin LO1 and LO2. They have internal load resistors and are always active. The transmit VCO-signal is damped with two buffers in series which drive the transmit mixer. A low pass is inserted between the two buffers in order to suppress harmonics.

Additional Information

Symmetrical circuit topology is used throughout the chip for good common mode rejection.
A bandgap reference with temperature and supply voltage compensation is also integrated.
With the TRS-input the IC can be switched from transmit to receive mode.

In receive mode (TRS = low) the transmit VCO is OFF, the transmit mixer is OFF, the isolation buffer for IFLOP is OFF, the buffer for LOR1/2 is ON, the buffer for LOP1/2 is ON and the RF VCO is ON.

In transmit mode (TRS = high) the transmit VCO is ON, the transmit mixer is ON, the isolation buffer for IFLOP is ON, the buffer for LOR1/2 is ON, the buffer for LOP1/2 is ON and the RF VCO is ON.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_{14}	– 0.5	7	V	
Open collector output voltage	$V_{6,7}$	– 0.5	V_S + 2.5	V	$V_S \leq 5.5$ V
Differential input voltage	$V_{1,4}$	– 1	1	V	
Junction temperature	T_j		125	°C	
Storage temperature	T_S	– 65	150	°C	
Thermal resistance (junction to ambient)	$R_{th\,JA}$		90	°C/W	

Operational Range

Within the operational range the IC operates as described in the circuit description.

Ambient temperature	T_A	– 40	85	°C	
Supply voltage	V_{14}	4.5	5.5	V	
RF VCO frequency range	$f_{RF\,VCO}$	1	1500	MHz	
Mixer frequency range	f_{Mix}	1	1500	MHz	
TR VCO frequency range	$f_{TR\,VCO}$	80	140	MHz	
I_{TRS} current: high	I_{TRS}		200	µA	$V_{TRS} = V_S$
V_{TRS} voltage: high	V_{TRS}	3.0	V_S	V	
I_{TRS} current: low	I_{TRS}		– 50	µA	V_{TRS} = 0 V
V_{TRS} voltage: low	V_{TRS}	0	0.8	V	

AC/DC Characteristics
T_A = – 40 to 85 °C; V_{CC} = 4.75 to 5.25 V

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Supply current during transmit operation	I_{14}	8.0	10.6	13.2	mA	TRS = high E1(2)LO and E1(2)IF open	1
Supply current	$I_{6,7}$	5.4	7.2	9.0	mA	TRS = high	1
Supply current during receive operation	I_{14}	5.6	7.5	9.4	mA	TRS = low E1(2)LO and E1(2)IF open	1
Supply current	$I_{6,7}$			10	µA	TRS = low	1
Transmit Mixer Output MO1/2							
Output resistance	$R_{MO1/2}$	1.0	1.2	1.4	kΩ	differential output	3
Output capacitance	$C_{MO1/2}$		700		fF	in parallel to $R_{MO1/2}$	3
Output level	V_X	75	100	125	mVrms		1
Output level	$P_{MO1/2}$	– 4	– 2	0	dBm	design hint for application circuit **see diagram 1**	2
Residual AM 90-MHz harmonic spurious				2	%		
Transmit VCO, Fixed Tank Circuit, External Circuitry Temperature Compensated							
Warm up drift of oscillator frequency	Δf_{VCO}		150		kHz	t = 5 s to 15 min after switch on	1
Residual carrier FM	$\Delta f_{VCO, rms}$			5	Hz	over 0.3 – 3.4 kHz acc. CCITT	1
Output phase noise	$L(f_m)$			– 120	dBC/ Hz	at ± 25 kHz, target value	1
Spurious level fluctuation	a_{SP}			– 42	dBC	at ± 12.5 kHz offset	1

AC/DC Characteristics (cont'd)
T_A = – 40 to 85 °C; V_{CC} = 4.75 to 5.25 V

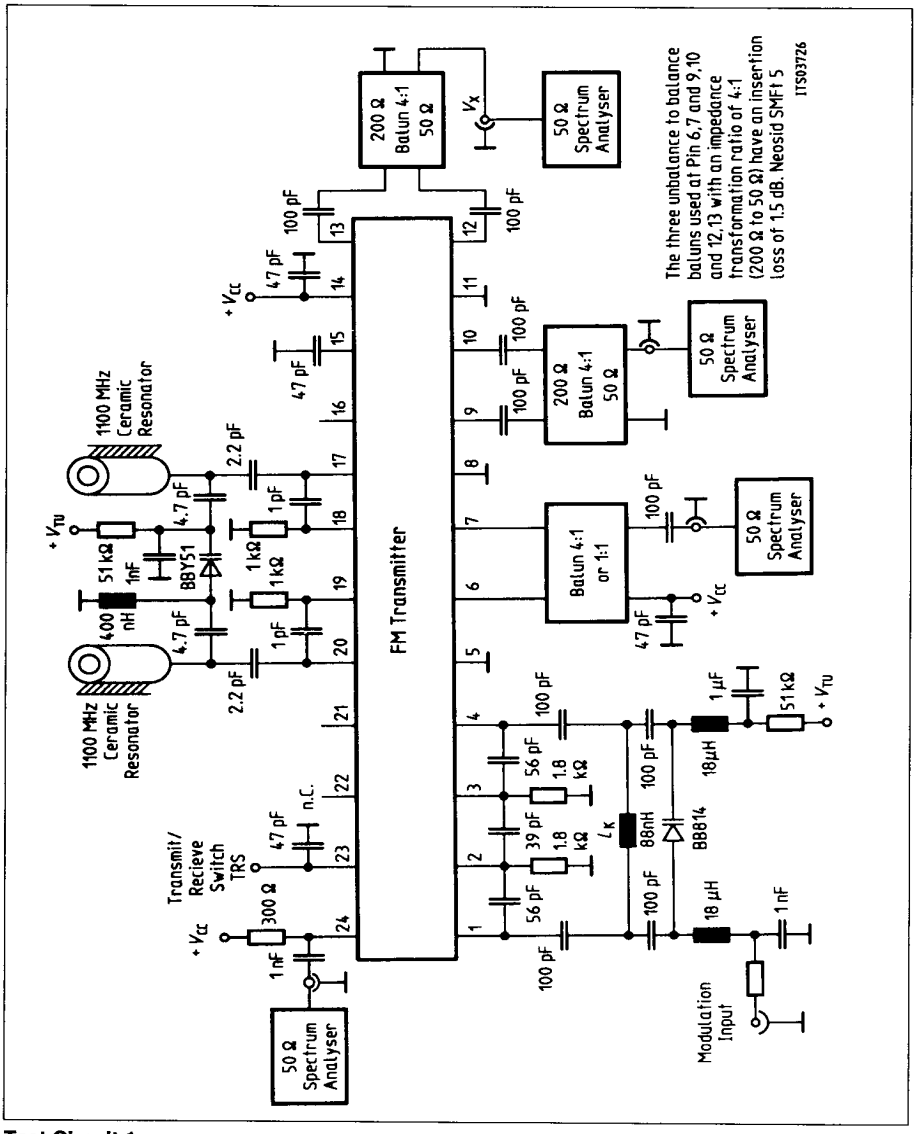
Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
RF VCO, Fixed Resonator, External Circuitry Temperature Compensated							
Oscillator frequency range	f_{VCO} f_{VCO}	945 900		980 1050	MHz MHz	V_T = 1 ... 4 V, with one fixed resonator using several types of resonators, according to desired frequency and matched test circuits	1
Warm up drift of oscillator frequency	Δf_{VCO}		150		kHz	TRS = low V_T = const t = 5 s to 15 min after switch ON	1
Warm up drift of oscillator frequency	Δf_{VCO}		350		kHz	TRS = high V_T = const t = 5 s to 15 min after switch ON	1
Residual carrier FM	$\Delta f_{VCO, rms}$			5	Hz	over 0.3 – 3.4 kHz acc. CCITT	1
Output phase noise	$L(f_m)$			– 114	dBC/Hz	at ± 25 kHz, target value according oscillator frequency range	1
Spurious outputs	a_{SP}			– 42	dBC	at ± 12 kHz offset, according oscillator frequency range	1
RF VCO-frequency pulling with transmit/receive switching				2	kHz	**see diagram 2**, target value	
Output to Receiver LOR1/2							
Output resistance	$R_{LOR1/2}$	1.6	2	2.4	kΩ	balanced value	3
Output capacitance	$C_{LOR1/2}$		500		fF	in parallel to $R_{LOR1/2}$	3
Output level	V_x	28	40	56	mVrms		1
Output level	$V_{LOR1/2}$	500		1000	mVpp	design hint for application circuit	2

$V_{LOR1/2}$ specified such that with the optimized coupling circuit between PMB 2430 and PMB 2230 the specified performance of the PMB 2430 can be achieved.

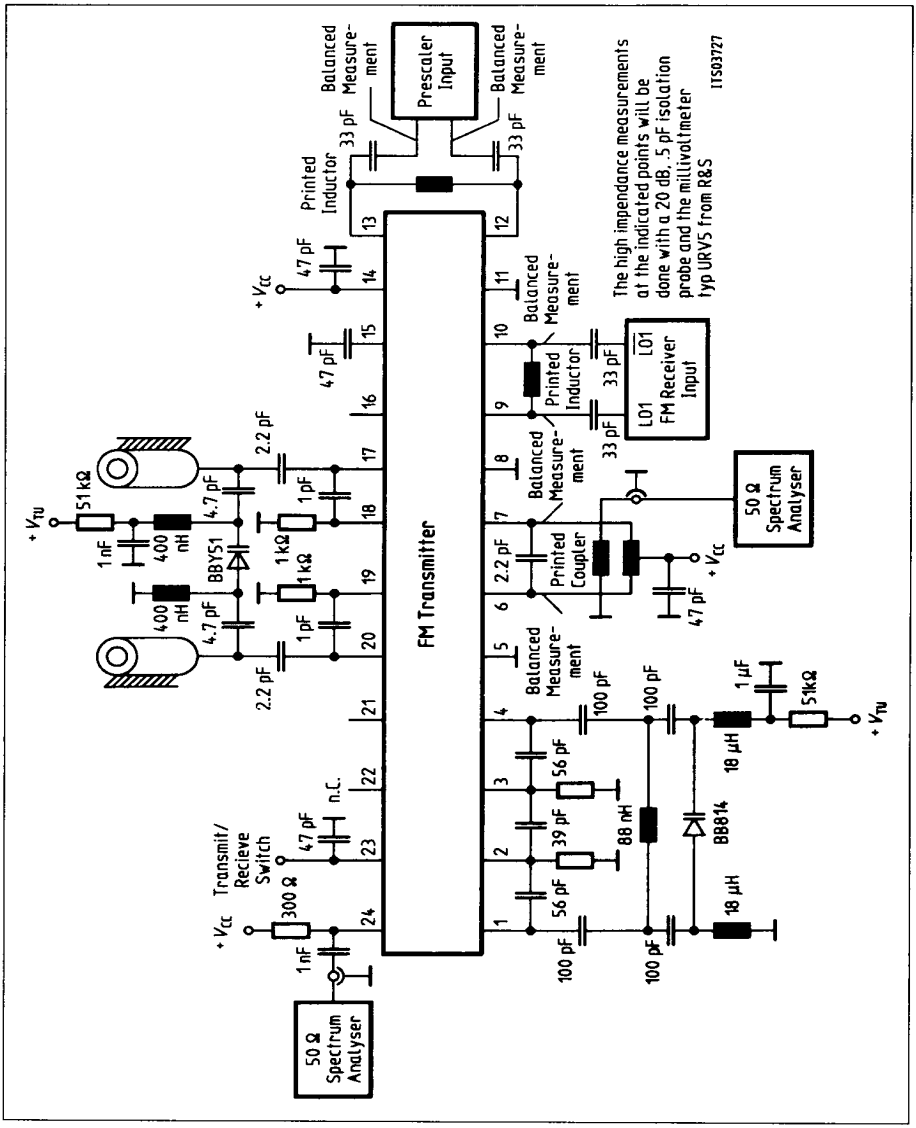
AC/DC Characteristics (cont'd)
T_A = – 40 to 85 °C; V_{CC} = 4.75 to 5.25 V

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Output to Prescaler / PLL LOP1/2							
Output resistance	$R_{LOP1/2}$	1.6	2	2.4	kΩ	balanced value	3
Output capacitance	$C_{LOP1/2}$		500		fF	in parallel to $R_{LOP1/2}$	3
Output level	V_X	28	40	56	mVrms		1
Output level	$V_{LOP1/2}$	70	175	210	mVrms	design hint for application circuit	2
Output to Transmit VCO PLL IFLOP							
Output resistance	R_{IFLOP}					external pull up resistor	
Output capacitance	C_{IFLOP}		500		fF	in parallel to R_{IFLOP}	3
Output level	V_{IFLOP}					depends on transmit VCO-current and IFLOP pull up resistor	1
Transmit / Receive Switch TRS							
L-input Voltage	V	0		0.8	V		1
L-input Current	I			– 50	µA		1
H-input Voltage	V	3		V_S	V		1
H-input Current	I			200	µA		1

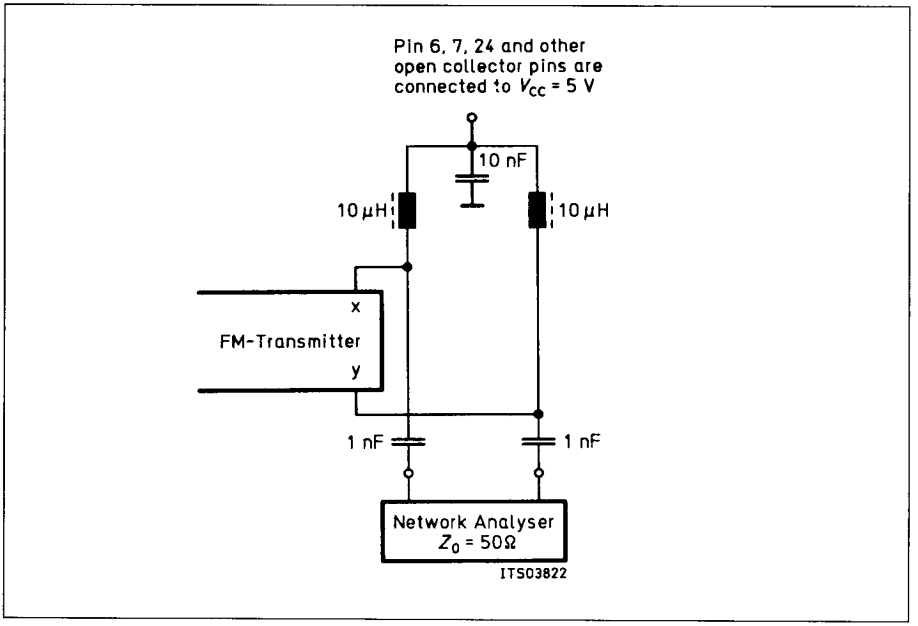
TRS	Transmit VCO	LOR1/2 Buffer	Transmit Mixer	LOP1/2 Buffer	Isolation Buffer	RF VCO ON
LOW	OFF	ON	OFF	ON	OFF	ON
HIGH	ON	ON	ON	ON	ON	ON



Test Circuit 1



Test Circuit 2



Test Circuit 3

Test Point	Test Frequency/MHz	Pin x	Pin y
LOP-output impedance	900	12	13
LOR-output impedance	900	9	10
MO-output impedance	900	6	7
IFLOP-output impedance	90	24	

The S-parameters are tested at the indicated frequency and the equivalent parallel or series circuit is calculated on this base.

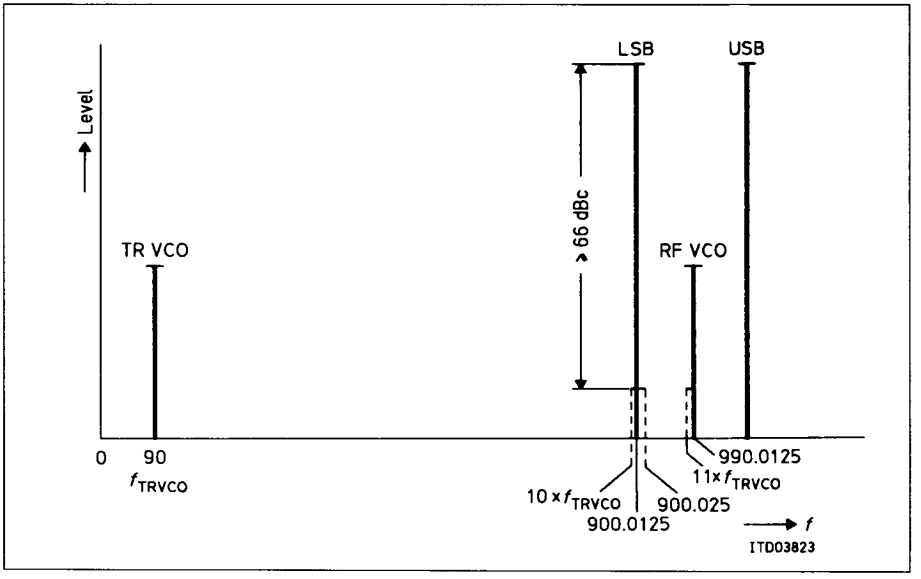


Diagram 1
Transmitter Mixer 90-MHz Harmonic Spurious

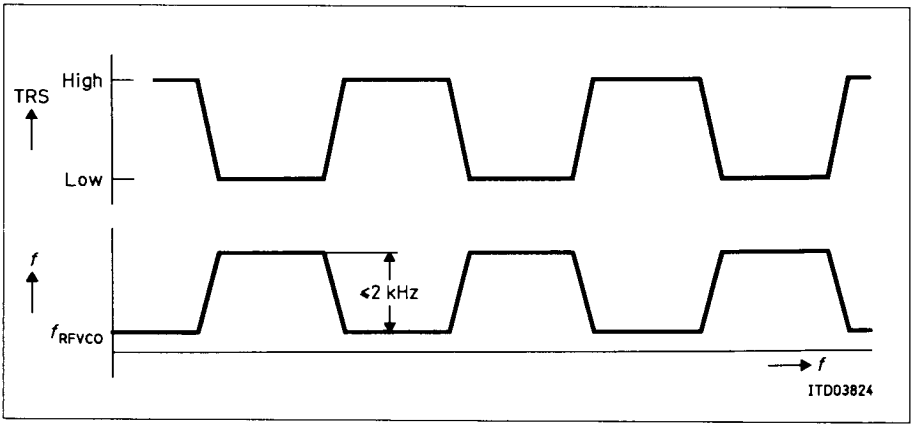
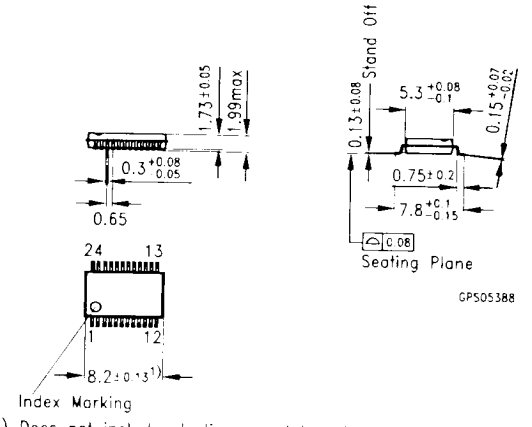


Diagram 2
RF VCO-Frequency Pulling with Transmit/Receive Switching

Package Outlines

Plastic-Package, P-DSO-24-4 (Shrink) (SMD)
(Dual-Small-Outlines)



1) Does not include plastic or metal protrusions of 0.15 per side

Sorts of Packing
Package outlines for tubes, trays ect. are contained in our Data Book "Package Information"

SMD = Surface Mounted Device

Dimensions in mm