SSI 78Q903
10Base-T Hub Transceiver

November 1991

DESCRIPTION

The SSI 78Q903 hub transceiver is designed for use in multi-port repeaters. It interfaces the hub (a multi-port transceiver) to the unshielded twisted-pair media. The SSI 78Q903 performs transmit, receive and receive squelch functions. Additional implementations include 10Base-T link integrity testing, automatic correction of receive polarity reversal, and a watchdog timer to jab continuous transmission.

The SSI 78Q903 software control mode provides a microprocessor interface with extensive command and status options. The hardware mode provides stand-alone operation.

The SSI 78Q903 is an advanced CMOS device and requires only a single 5-volt power supply.

APPLICATIONS

- Multi-port Repeaters

FEATURES

- **Meets or exceeds IEEE 802.3 standards for 10Base-T interface**
- **Provides predistorted signal to the transmit filter**
- **Internal programmable squelch circuits**
- **Detection and correction of reversed polarity**
- **Microprocessor interface and control**
- **Differential or single-ended transmit input**
- **LED driver for jabber, link and reversed polarity**
- **Single 5 V supply, low-power CMOS technology**
- **Available in 24-pin DIP and 28-pin PLCC packages**

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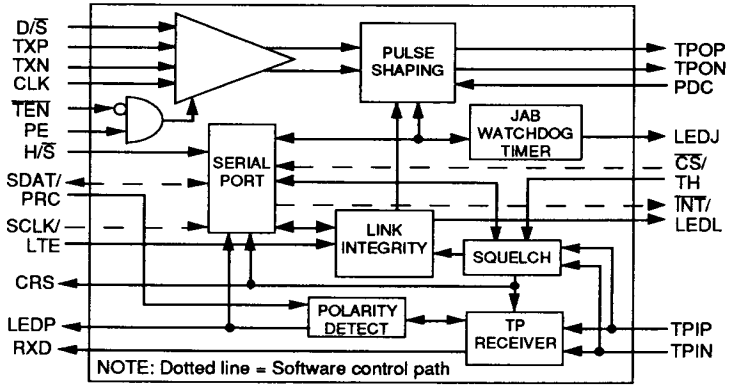
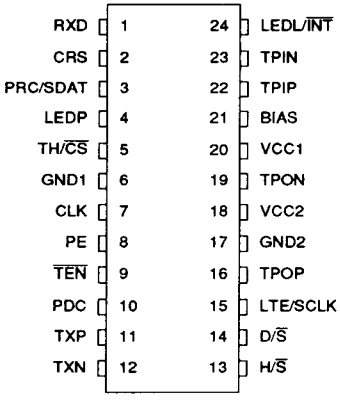
BLOCK DIAGRAM



PIN DIAGRAM



24-Pin DIP

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 78Q903 hub transceiver interfaces a hub controller to unshielded twisted-pair cables, transferring data in both directions. The hub side of the interface comprises three circuits: Transmit (the DO output from the hub controller), Receive (the DI input to the hub controller), and Status/Command. The twisted-pair network side of the interface comprises two circuits: Twisted Pair Input (TPI) and Twisted Pair Output (TPO). In addition to these basic circuits, the SSI 78Q903 contains logic controls and LED drivers for status indications.

Functions are defined from the hub side of the interface. The SSI 78Q903 "Transmit" function refers to data transmitted by the hub over the DO circuit to the twisted-pair network. The SSI 78Q903 Receive function refers to data received by the hub over the DI circuit from the twisted-pair network. In addition to basic transmit and receive functions, the SSI 78Q903 performs some of the Medium Attachment Unit (MAU) functions defined by the IEEE 802.3 10Base-T specification such as link integrity testing and jabber control. The SSI 78Q903 also offers extensive software control and status reporting capabilities available through the serial interface.

TRANSMIT FUNCTION

The SSI 78Q903 transfers Manchester-encoded, CMOS-level data from the hub controller to the twisted-pair network (the TPO circuit). The output signal on TPON and TPOP is pre-distorted to meet the 10 Base-T jitter template. The output waveform (after the transmit filter) is shown in Figure 1. During idle periods, the SSI 78Q903 transmits link integrity test pulses on the TPO circuit. Transmitter inputs can be differential or single-ended, as selected by the D/$\overline{S}$ pin. The differential input is TXP/TXN. Single-ended input is supplied by TXP.

SINGLE ENDED INPUT MODE

The single ended transmit interface consists of TXP, Port Enable (PE) and the 20 MHz clock input (CLK). In the single-ended mode, TXP is sampled before transmission at the 20 MHz clock rate and must meet the specified setup and hold times relative to the CLK input. Predistortion control is generated internally. PE must be high for transmission to occur. Transmission begins at the first low-going data on TXP. End of Frame is detected when TXP is held high for more than 150 ns (plus setup and hold times).

DIFFERENTIAL INPUT MODE

In the differential input mode, the transmit interface consists of TXP and TXN, PE, PDC, and the Transmit Enable input ($\overline{TEN}$). Transmission starts when PE is high and $\overline{TEN}$ is low, and ends when either PE or $\overline{TEN}$ goes inactive. Predistortion control is provided by the PDC input.

RECEIVE FUNCTION

The SSI 78Q903 receive function accepts serial data from the twisted-pair network (the TPI circuit), converts it to a CMOS level signal, and passes it to the hub controller. An internal squelch function discriminates noise from link test pulses and valid data streams. Only valid data streams activate the receive function. If the differential signal at the TPI circuit input falls below 75% of the threshold level (unsquelched) for 8 bit times (typical), the SSI 78Q903 receive function will enter the idle state. A reduced threshold is available which lowers the squelch level by 4.5 dB. Reducing the squelch level extends the network range when used with a low-noise media such as shielded twisted-pair. In the software control mode, the reduced threshold is selected through the serial interface. In the hardware mode, the reduced threshold is selected by tying the TH pin low.

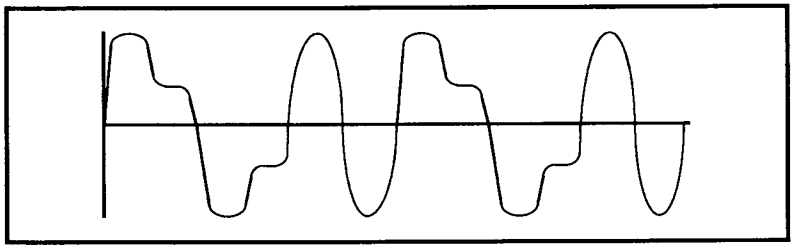


FIGURE 1: 78Q903 TPO Output Waveform

POLARITY REVERSE FUNCTION

The SSI 78Q903 polarity reverse function uses both link pulses and end-of-frame data to determine polarity of the received signal. A reversed polarity condition is declared when eight opposite link pulses are received without receipt of a link pulse with the expected polarity. Reversed polarity is also declared if four frames are received with a reversed start-of-idle. Whenever reversed polarity is declared, these two counters are reset to zero. If the SSI 78Q903 enters the link fail state and no receive data or link pulses are received within 96 to 128 ms, the polarity is reset to the default (non-flipped) condition. (If Link Integrity is disabled, polarity detection is based only on received data.)

JABBER CONTROL FUNCTION

Figure 2 is a state diagram of the SSI 78Q903 jabber control function. In the software mode, jabber control may be disabled through the serial port. In the hardware mode, jabber control is enabled at all times. The SSI 78Q903 on-chip watchdog timer prevents the device from locking into a continous transmit mode. When a transmission exceeds the time limit, the Watchdog timer disables the transmit function. Once the SSI 78Q903 is in the jabber state, the transmit circuit must remain idle for a period of 491 to 525 ms before it will exit the jabber state.

LINK INTEGRITY TEST

Figure 3 is a state diagram of the SSI 78Q903 Link Integrity Test Function. The Link Integrity Test is used to determine the status of the receive side twisted-pair cable. Link testing is enabled when the LTE pin is tied high. When enabled, the receiver recognizes link integrity pulses which are transmitted in the absence of receive traffic. If no serial data stream or link integrity pulse is detected within 50 - 150 ms, the chip enters a link fail state and disables the transmit function. The SSI 78Q903 ignores any link integrity pulse with interval less than 2 -7 ms. The SSI 78Q903 will remain in the link fail state until it detects either a serial data packet or two or more link integrity pulses. Link activity is indicated by a low on the LEDL pin.

HARDWARE CONTROL MODE

In hardware control mode the serial port is not used, and the transceiver is accessed and controlled through individual pins. Hardware control mode is selected when the H/$\overline{S}$ pin is set to a logic 1.

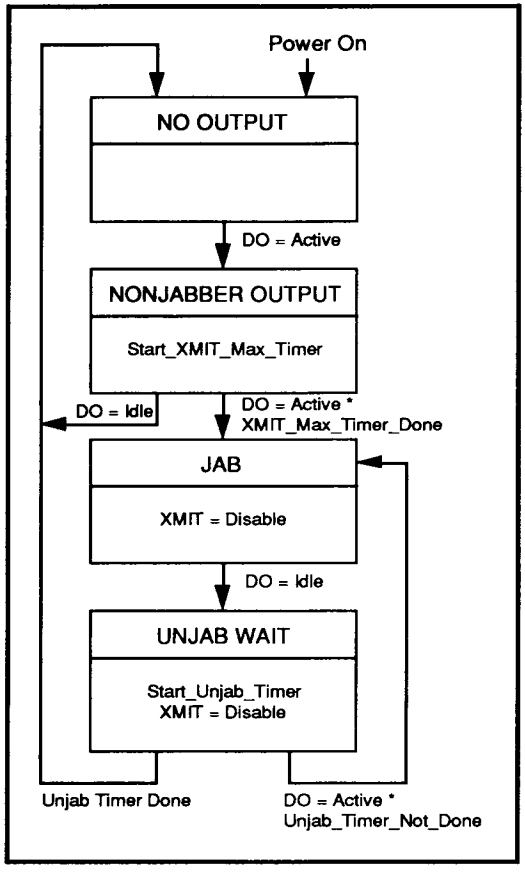


FIGURE 2: Jabber Control Function

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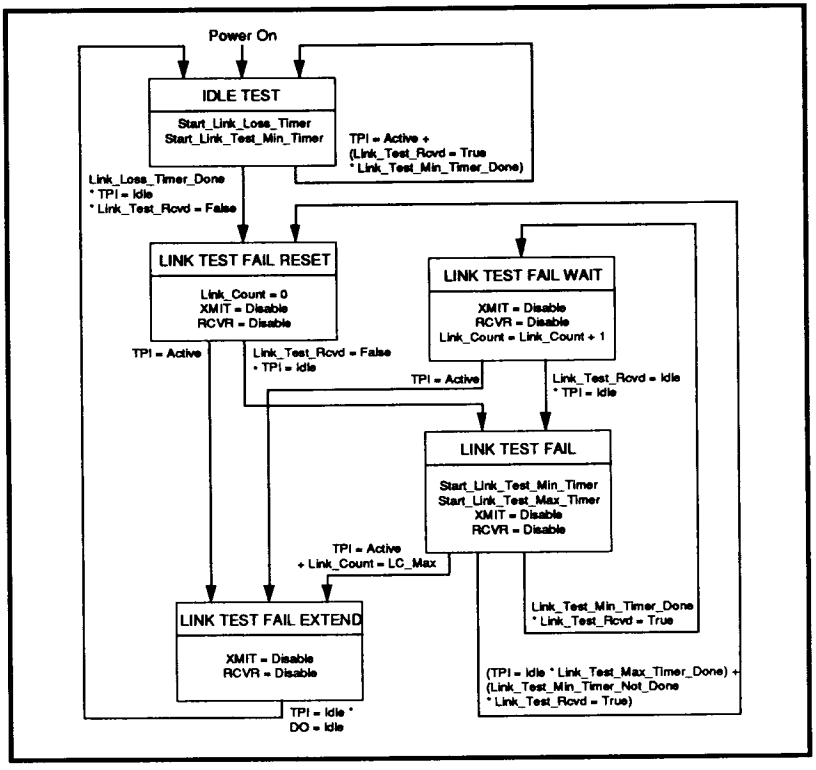

FIGURE 3: Link Integrity Test Function

SOFTWARE CONTROL MODE

To allow a microprocessor to access and control the SSI 78Q903 through the serial interface, the H/$\overline{S}$ pin is set to logic 0. The serial interface consists of three signals: the Chip Select input ($\overline{CS}$), the bidirectional Serial Data port (SDAT), and a Serial Clock (SCLK). The SSI 78Q903 incorporates a standard microcontroller interface which operates with any standard 8051 using TXD/RXD (port 3) for SCLK and SDAT, and any port for $\overline{CS}$. The SCLK frequency should be 5 MHz or less. In software control mode, the LEDL pin is reconfigured as an interrupt out ($\overline{INT}$). $\overline{INT}$ is an open drain, active low which is set by any of three conditions: Jab, Link Fail, or Non-Correctable Polarity. The $\overline{INT}$ signal stays active until $\overline{CS}$ goes active (low). The $\overline{INT}$ bit remains set until the first port read cycle. Once set and then cleared, $\overline{INT}$ will not set again until all failure interrupts return to a pass state. The $\overline{INT}$ signal can be masked by bit C4 of the Command word. The serial data (SDAT) is contained in a 16-bit word consisting of an 8-bit Address/Command byte and an 8-bit Command/Status byte. Figure 4 shows the serial interface data structure and timing. The SSI 78Q903 serial port is accessed by causing the Chip Select ($\overline{CS}$) input to transition from high to low. Bit 4 of the serial Address/Command byte provides Read/Write control when the chip is accessed. A logic 1 indicates a read operation, and a logic 0 indicates a write operation.

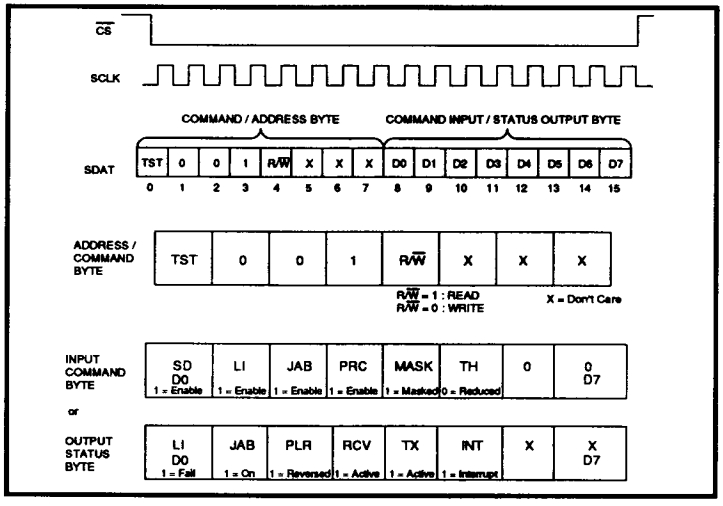

FIGURE 4: Serial Interface Data Structure

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TABLE 1: Address/Command Bits

AC0	Test Mode. Must be 0 (1 reserved for Factory)
AC1	Address Bit 0. Must be 0 (reserved)
AC2	Address Bit 1. Must be 0 (reserved)
AC3	Address Bit 2. Must be 1 (reserved)
AC4	Read/Write. 1 = Read, 0 = Write
AC5	Must be 0 (reserved)
AC6	Must be 0 (reserved)
AC7	Must be 0 (reserved)

TABLE 2: Command (Write) Bits

C0	Shut Down (TXP/TXN and TEN are ignored, RXD and CRS go to high impedance. Standard transmit functions are disabled, but Link Pulse reception/transmission continue.)
C1	Link Test Enable/Disable
C2	Jabber Enable/Disable
C3	Polarity Correction Enable
C4	Mask Interrupt (Prevents the open drain $\overline{INT}$ pin from going active.)
C5	Reduced Threshold (Receive threshold reduced by 4.5 dB.)
C6	Must be 0 (reserved)
C7	Must be 0 (reserved)

TABLE 3: Status (Read) Bits

S0	Link Test Fail/Pass
S1	Jabber On/Off
S2	Polarity Reversed/Normal
S3	Receiver Active (Cleared on Read)
S4	Transmitter Active (Cleared on Read)
S5	Interrupt (Cleared on Read)
S6	Don't Care
S7	Don't Care

PIN DESCRIPTION

INPUT PINS

NAME	TYPE	DESCRIPTION
RXD	O	Receive Data: Data received from the twisted-pair is output to the hub controller DI circuit on this pin as a CMOS level Manchester encoded data stream. High impedance when in software shut down mode.
CRS	O	Carrier Sense: Goes high to indicate valid receive data. High impedance when in software shut down mode.
PRC	I	Polarity Reverse Correction (Hardware Control): In the hardware control mode, tying this pin high enables the SSI 78Q903 to automatically correct for reversed polarity at the TPI circuit.
SDAT	I/O	Serial Data (Software Control): In software control mode, this pin is the serial data I/O port.
LEDP	O	Polarity Reverse. Open drain output: Active low indicates polarity reversed.
TH	I	Threshold Control (Hardware Control): In hardware mode, forcing this pin low reduces the TP receive squelch by 4.5 dB.
$\overline{CS}$	I	Chip Select (Software Control): Active low input accesses the serial port in the software mode. $\overline{CS}$ must transition high to low, and remain low for each port operation.
GND1	-	Ground #1.
CLK	I	Clock: 20 MHz CMOS level clock input.
PE	I	Port Enable: Active CMOS high enables the transmitter. In differential input mode, PE must be high when $\overline{TEN}$ is low to enable transmitter.
$\overline{TEN}$	O	Transmit Enable: Active CMOS low enables the transmitter when PE is high. Required for differential input mode only.
PDC	I	Pre-Distortion Control: A CMOS level, synchronous input signal at logic 1 will predistort the output voltage (differential input mode only).
TXP/TXN	I	Data Out Positive/Data Out Negative: Differential input pair connected to the hub controller DO circuit. When D/$\overline{S}$ pin is tied low, TXP becomes single-ended CMOS level input, synchronous to the 20 MHz CLK.
LEDJ	O	Jabber LED Driver: Open drain driver for the Jabber indicator LED. Goes active when watch dog timer begins jab and stays active until end of the unjab wait period (491 - 525 ms).
H/$\overline{S}$	I	Hardware/Software Control Select: When set to a logic 0, selects software control mode. When set to a logic 1, selects hardware control mode.
D/$\overline{S}$	I	Differential/Single-Ended Select: When set to a logic 0, selects single-ended TXP input. When set to a logic 1, selects differential TXP/TXN input.
LTE	I	Link Test Enable (Hardware Control):In hardware control mode, an active high on this pin enables the link test function.
SCLK	I	Serial Clock (Software Control):The serial clock required for software control operation is input on this pin. SCLK must be ≤ 2 MHz.

PIN DESCRIPTION (continued)

INPUT PINS (continued)

NAME	TYPE	DESCRIPTION
TPOP/TPON	O	Twisted Pair Transmit Outputs: Transmit drivers to the twisted-pair output filter. The output is pre-distorted to meet the 10Base-T template.
GND 2 GND 3 GND 4	- - -	Ground 2. Ground 3. Ground 3.
VCC2 VCC1 VCC3	- - -	Power Supply #2: + 5 V power supply input. Power Supply # 1: + 5 V power supply input. Power Supply # 3: + 5 V power supply input.
BIAS	O	Resistor Bias Control: Bias control for the operating circuit. Bias is set from an external 12.4 kΩ resistor to ground.
TPIP/TPIN	O	Twisted-Pair Receive Inputs: Differential receive inputs from the twisted-pair input filter.
LEDL[1]	O	Link Driver (Hardware Control): LED driver indicates link activity.
$\overline{INT}$	O	Interrupt (Software Control): The microprocessor interrupt required for software control is output on this pin. The interrupt is an open drain, active low which indicates Jab, Link Failure or Non-correctable Polarity.

[1]LED drivers pull low when active.

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ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATING	UNIT
Supply Voltage, Vcc	-0.3 to 6	V
Operating Temperature, T_{OP}	0 to +70	°C
Storage Temperature, T_{ST}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM[1]	MAX	UNIT
Supply Voltage[2], Vcc		4.75	5.0	5.25	V
Operating Temperature, T_{OP}		0	-	70	°C

[1]Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

[2] Maximum voltage differential between VCC1 and VCC2 (and VCC3 for PLCC parts) must not exceed 0.3V.

ELECTRICAL SPECIFICATIONS

I/O ELECTRICAL CHARACTERISTICS (Ta = 0 to 70 °C, Vcc = 5V ±5%)

PARAMETER		CONDITIONS	MIN	NOM[1]	MAX	UNIT
Input low voltage	V_{IL}		-	-	0.8	V
Input high voltage	V_{IH}		2.0	-	-	V
Output low voltage (Open drain LED Driver[2])	V_{OL}	IOUT = 10 mA	-	-	0.4	V
Supply current	I_{CC}	Line Idle	-	40	-	mA
		Line Active	-	75	-	mA
Input leakage current[3]	I_{LL}	Input between VCC and GND	-	±1	±10	µA
High Z state leakage current	I_{TS}	Output between VCC and GND	-	±1	±10	µA

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing

[2] LED Drivers can sink up to 10 mA of drive current

[3] Not including TPIN, TPIP, TXN, TXP, PDC, PE, CLK or $\overline{TEN}$.

CMOS I/O CHARACTERISTICS[4] (Ta = 0 to 70°C, Vcc = 5V ±5%)

Input low voltage	V_{CIL}		-	2.0	-	V
Input high voltage	V_{CIH}		-	3.0	-	V
Output low voltage	V_{COL}		-	0	-	V
Output high voltage	V_{COH}		-	5.0	-	V
Input leakage current	I_{CIL}		-	± 1.0	-	µA

[4]Pins TXP, TSN, $\overline{TEN}$, PE, PDC, CLK and RXD

TRANSMIT CHARACTERISTICS (Ta = 0 to 70°C, Vcc = 5V ±5%)

Transmit output impedance Z_{OUT}		-	5	-	Ω
Peak differential output voltage V_{OD}	Load = 200 Ω at TXP/TXN	± 4.5	-	± 5.2	V
Differential voltage imbalance V_{OB}	Load = 200 Ω at TXP/TXN	-	-	± 40	mV
Transmit timing jitter addition	After Tx filter, 0 line length	-	-	± 8	ns
Transmit timing jitter addition	After Tx filter, line model as shown in IEEE 802.3 standard for 10Base-T	-	-	± 3.5	ns

RECEIVE CHARACTERISTICS (Ta = 0 to 70°C, Vcc = 5V ±5%)

Receive input impedance, Z_{IN}	Between TPIP/TPIN	-	20	-	kΩ
Differential squelch threshold, V_{DS}		-	420	-	mV
Reduced squelch threshold, V_{DSR}		-	250	-	mV
Receive timing jitter		-	-	1.5	ns

SWITCHING CHARACTERISTICS (Ta = 0 to 70°C, Vcc = 5V ±5%)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Jabber Timing						
Maximum transmit time			88.5	-	144	ms
Unjab time			442	-	578	ms
Link Integrity Timing						
Time link loss			65	-	66	ms
Time between Link Integrity Pulses			9	-	11	ms
Valid interval for received Link Integrity Pulses			4.1	-	65	ms
Serial Interface Timing						
SCLK low time	t_{S1}		100	-	-	ns
SCLK high time	t_{S2}		100	-	-	ns
$\overline{CS}$ to SCLK setup time	t_{S3}		50	-	-	ns
SCLK to $\overline{CS}$ hold time	t_{S4}		0	-	-	ns
$\overline{CS}$ inactive time	t_{S5}		50	-	-	ns
SDAT to SCLK setup time	t_{S6}		50	-	-	ns
SCLK to SDAT hold time	t_{S7}		0	-	-	ns
SCLK to SDAT valid	t_{S8}		-	-	100	ns
SCLK falling edge or $\overline{CS}$ rising edge to SDAT high Z	t_{S9}		-	-	100	ns
SCLK rise/fall time			-	-	20	ns
Transmit Timing (Single Ended Mode)						
TXP setup time to CLK high	t_{ST1}		20	-	-	ns
TXP hold time from CLK high	t_{ST2}		0	-	-	ns
Transmit Timing (Differential Mode)						
TXP rising edge to PDC rising edge	t_{DT1}		-	50	-	ns
TXP low to PDC low	t_{DT2}		-	0	-	ns
TXP high to TXN low	t_{DT3}		0	-	± 5	ns
TXP low to TXN high	t_{DT4}		0	-	± 5	ns

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ELECTRICAL SPECIFICATIONS

SWITCHING CHARACTERISTICS (Ta = 0 to 70°C, Vcc = 5V ±5%) (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Receive Timing						
Valid receive data to CRS high	t_{R1}		-	-	500	ns
Receive steady state propagation delay	t_{R2}		-	-	100	ns
Receive turn-off to CRS low	t_{R3}		250	-	400	ns
Receiver jitter	t_{R4}		-	-	± 1.5	ns
CRS high to RXD low	t_{R5}		0	-	100	ms
General						
Receive start-up delay			0	-	500	ns
Transmit start-up delay			0	-	200	ns
TXP/TXN rise/fall time	t_{TRF}		-	5	-	ns

FIGURE 5: Serial Interface Timing

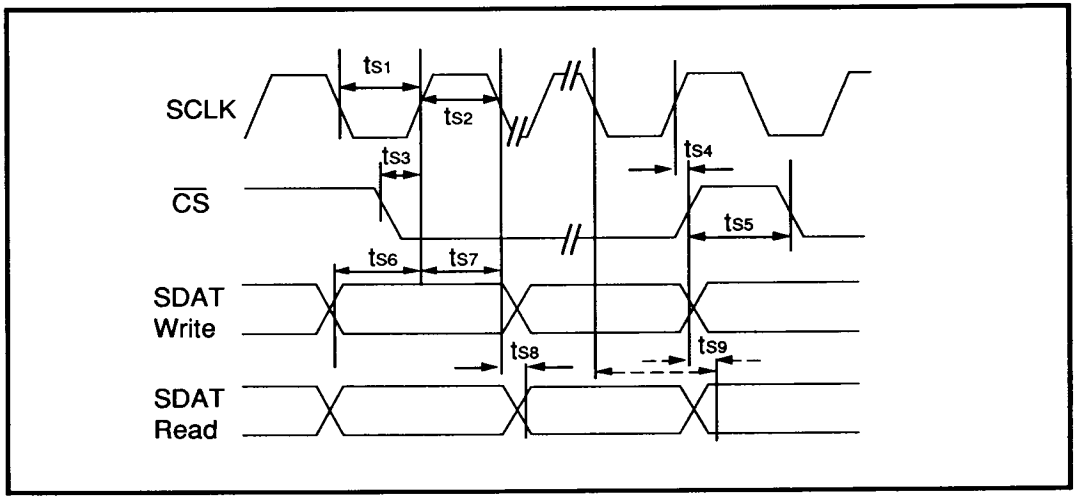

FIGURE 6: Transmit Timing - Single Ended Input Mode

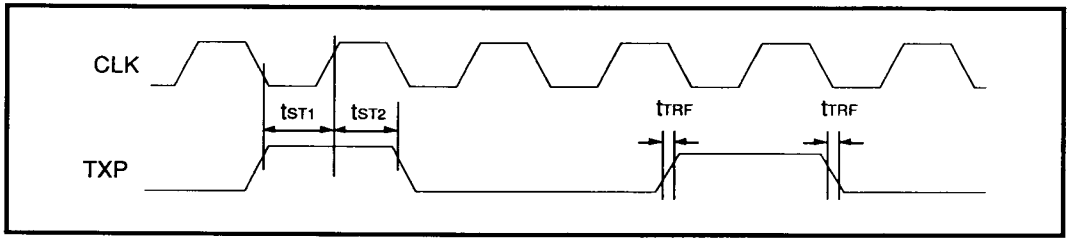

FIGURE 7: Transmit Timing - Differential Input Mode

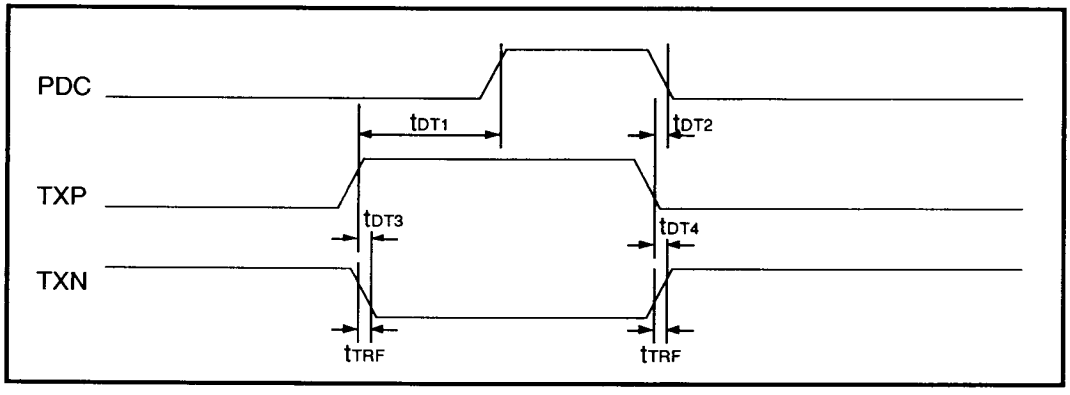

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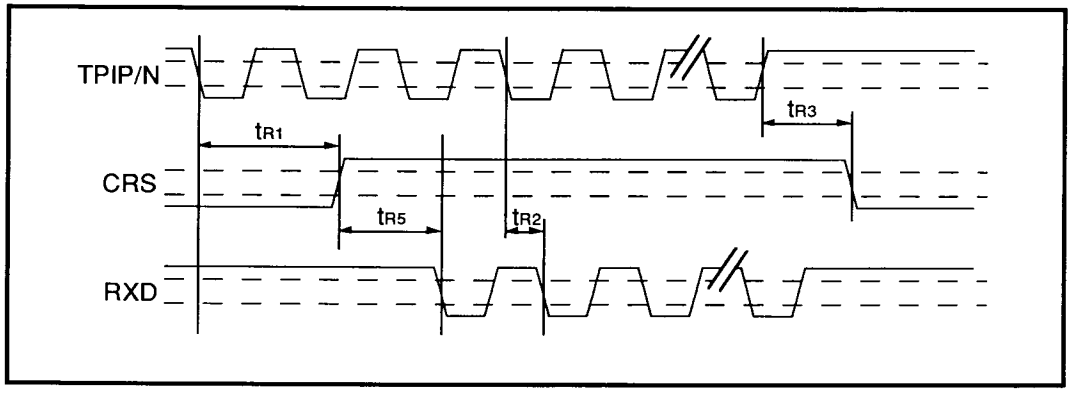
FIGURE 8: Receive Timing



APPLICATIONS

Figure 9 shows the SSI 78Q903 in a typical hardware control application. The SSI 78Q903 hub transceivers interface the Hub Controller to the RJ45 connectors of the twisted pair network. The D/$\overline{S}$ pin is grounded, effecting the single ended mode, so TXN, PDC and $\overline{TEN}$ are not connected. An external source provides the required 20 MHz clock signal. Transmit and receive filters are required in the TPO and TPI circuits. Details of the transmit and receive filters are shown in Figures 10 and 11, respectively. (Differential filters are also recommended.) Integrated filters such as the TDK Corporation HIM 3000, Valor PT3877, Fil-Mag 78Z1120B or Pulse Engineering PE65421 may be used. Figure 12 shows a typical software control application, operating in the differential input mode (D/$\overline{S}$ is tied high) with TXN, $\overline{TEN}$, and PDC connected.

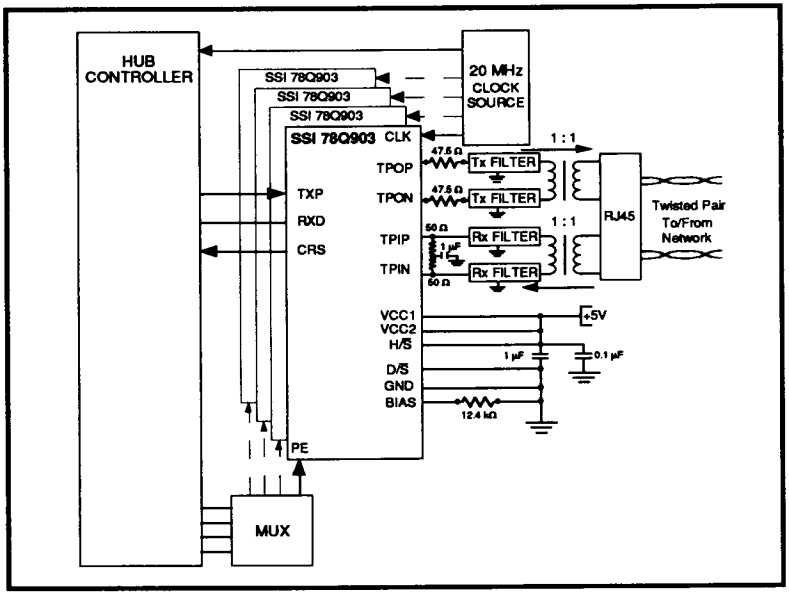


FIGURE 9: Typical SSI 78Q903 Hardware Control Application

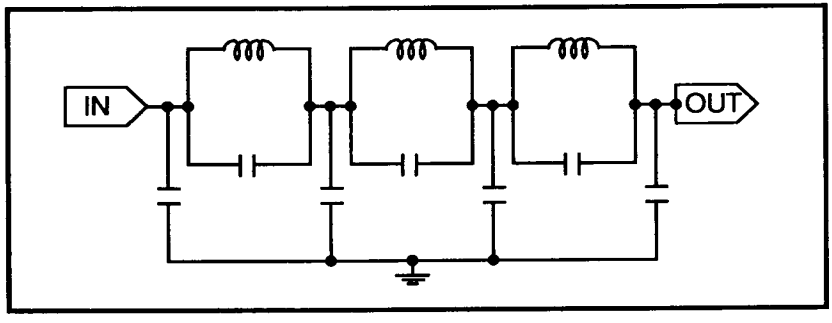


FIGURE 10: Transmit Filter Diagram

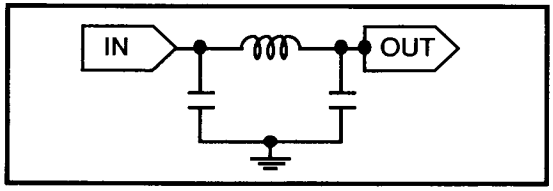


FIGURE 11: Receive Filter Diagram

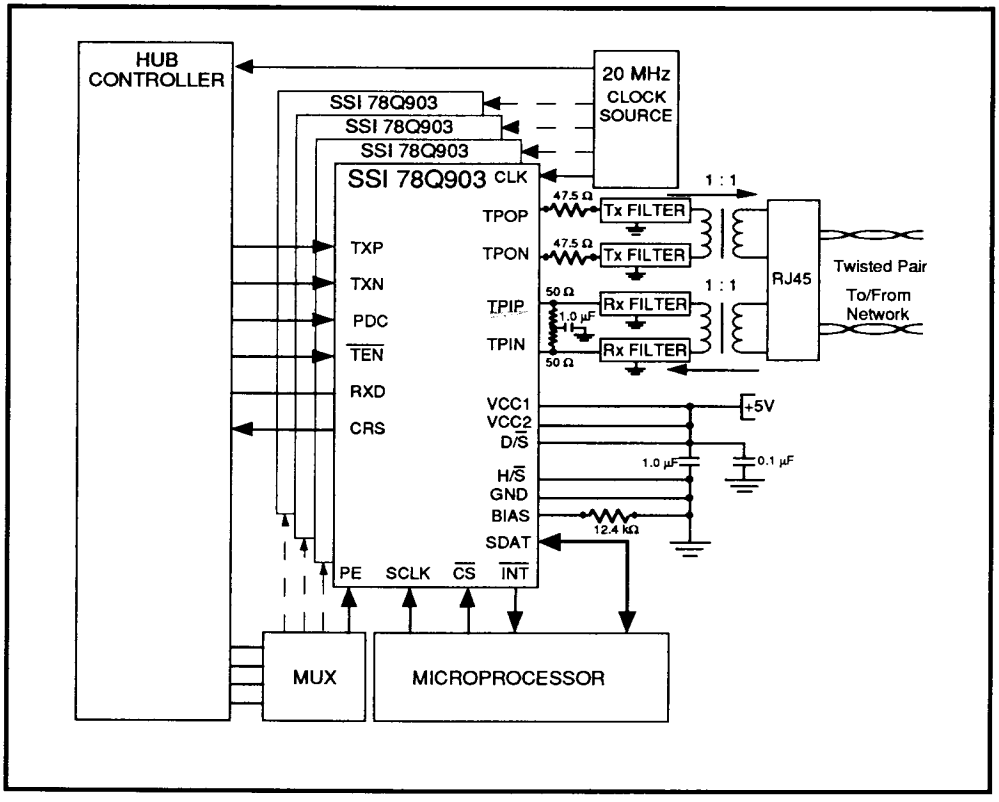


FIGURE 12: Typical SSI 78Q903 Software Control Application

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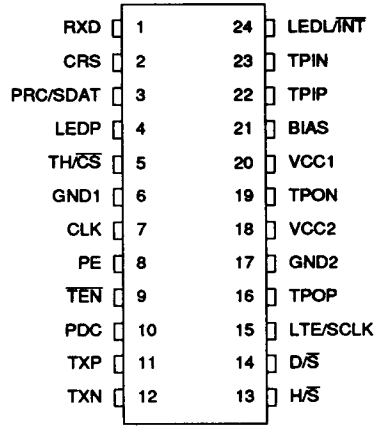
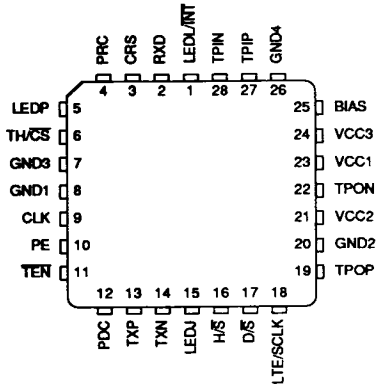
PACKAGE PIN DESIGNATIONS
(TOP VIEW)

CAUTION: Use handling procedures necessary for a static sensitive component.



24-Pin DIP



28-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 78Q903 24-Pin DIP	78Q903-CP	78Q903-CP
SSI 78Q903 28-Pin PLCC	78Q903-CH	78Q903-CH

Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX (714) 573-6914