

Absolute Maximum Ratings

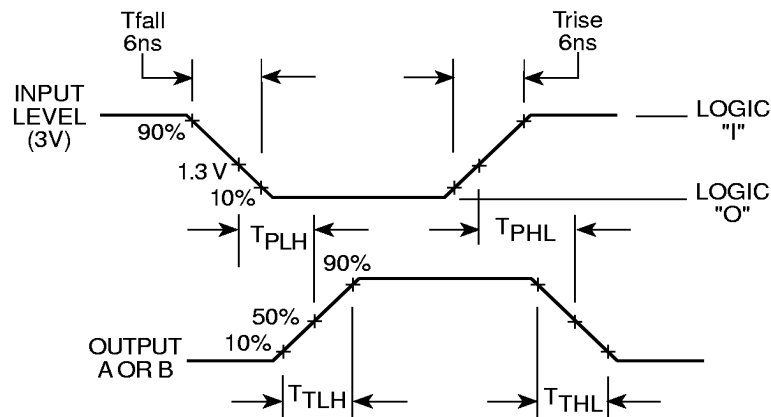
Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Positive DC Supply Voltage	-0.5	5.5	V
V_{EE}	Negative DC Supply Voltage	-9.0	0.5	V
V_{OPT}	Optional DC Output Supply Voltage	-0.5	2.0	V
$V_{OPT} - V_{EE}$	Output to Negative Supply Voltage Range	-0.5	9.0	V
$V_{CC} - V_{EE}$	Positive to Negative Supply Range	-0.5	14.5	V
V_I	DC Input Voltage	-0.5	$V_{CC} + 0.5$	V
I_I	DC Input Current	-25	25	mA
V_O	DC Output Voltage	$V_{EE} - 0.5$	$V_{OPT} + 0.5$	V
V_O	DC Output Current	-25	25	mA
T_{STG}	Storage Temperature	-65	150	°C

All voltage are referenced to GND. All inputs and outputs incorporate latch-up protection structures.

DC Characteristics Over Guaranteed Operating Range

Symbol	Parameter	Test Conditions		Units	Limits		
					Min.	Typ.	Max.
V_{IH}	Input HIGH Voltage	Guaranteed HIGH Input Voltage		V	2.0	1.5	
V_{IL}	Input LOW Voltage	Guaranteed LOW Input Voltage		V		1.5	0.8
V_{OH}	Output HIGH Voltage	$I_{OH} = -1\text{ mA}$	$V_{EE} = \text{Max}$	V	$V_{OPT} - 0.1$		
V_{OL}	Output LOW Voltage	$I_{OL} = 1\text{ mA}$	$V_{EE} = \text{Max}$	V			$V_{EE} + 0.1$
I_{IN}	Input Leakage Current	$V_{IN} = V_{CC}$ or GND	$V_{EE} = \text{Min}$	μA	-1.0	0	1.0
I_{CC}	Quiescent Supply Current	$V_{CC} = \text{Max}$ $V_{OPT} = \text{Min or Max}$	$V_{EE} = \text{Min}$ $V_{IN} = V_{CC}$ or GND	μA			100
ΔI_{CC}	Additional Supply Current, per TTL Input pin	$V_{CC} = \text{Max}$	$V_{IN} = V_{CC} - 2.1\text{ V}$	mA			1.0

Switching Waveforms



2. V_{OPT} is grounded for most applications. To improve the intermodulation performance and the 1dB compression point of GaAs control devices at low frequencies, V_{OPT} can be increased to between 1.0 and 2.0V. The nonlinear characteristics of the GaAs control devices will approximate performance at 500 MHz. It should be noted that the control currents on the GaAs MMICs will increase when positive controls are applied.

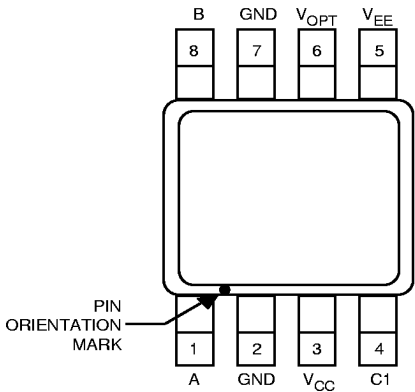
Truth Table for Single Driver (SWD-109)

Input	Outputs	
C1	A	B
Logic "0"	V_{EE}	V_{OPT}
Logic "1"	V_{OPT}	V_{EE}

Ordering Information

Part No.	Package
SWD-109 PIN	SOIC 8 Lead
SWD-109TR	Forward Tape and Reel
SWD-109RTR	Reverse Tape and Reel

Functional Schematic (SWD-109)



AC Characteristics Over Guaranteed Operating Range⁴ (SWD - 109)

Symbol	Parameter	$V_{OPT} - V_{EE}$	Max Limits			Unit
			-55 to +25°C	≤ +85°C	≤ +125°C	
T_{PLH}	Propagation Delay, I to either O	4.5 6.5 8.5	45 44 43	55 54 52	61 59 57	ns
T_{PHL}	Propagation Delay, I to either O	4.5 6.5 8.5	45 43 41	55 52 49	61 57 53	ns
T_{TLH}	Output Rising Transition Time	4.5 6.5 8.5	10.0 9.0 8.0	10.0 9.0 8.0	11.0 9.0 8.0	ns
T_{THL}	Output Falling Transition Time	4.5 6.5 8.5	10.0 9.0 8.0	10.0 9.0 8.0	11.0 9.0 8.0	ns
T_{skew}	Delay Skew, OA to OB	4.5 6.5 8.5	8.0 8.0 7.5	8.5 8.5 8.0	10.0 10.0 9.5	ns
C_{IN}	Input Capacitance	-	10	10	10	pF
C_{PDC}	Power Dissipation Capacitance ⁵	-	10	10	10	pF
C_{PDE}	Power Dissipation Capacitance ⁵	-	140	140	140	pF

4. $V_{CC} = 4.5V$, $V_{EE} = -4.5V$, $V_{OPT} = 0V$, $C_L = 25$ pF, $Trise$, $Tfall = 6$ ns. These conditions represent the worst case for slow delays.

5. Total Power Dissipation is calculated by the following formula: $PD = V_{CC}^2 fC_{PDC} + (V_{OPT} - V_{EE})^2 fC_{PDE}$

Specifications Subject to Change Without Notice.

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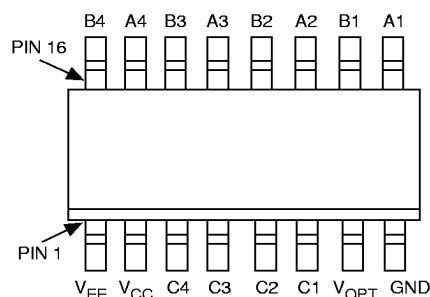
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Truth Table for Quad Driver (SWD-119)

Inputs				Outputs							
C4	C3	C2	C1	B4	A4	B3	A3	B2	A2	B1	A1
0	0	0	0	X	Y	X	Y	X	Y	X	Y
0	0	0	1	X	Y	X	Y	X	Y	Y	X
0	0	1	0	X	Y	X	Y	Y	X	X	Y
0	0	1	1	X	Y	X	Y	Y	X	Y	X
0	1	0	0	X	Y	Y	X	X	Y	X	Y
0	1	0	1	X	Y	Y	X	X	Y	Y	X
0	1	1	0	X	Y	Y	X	Y	X	X	Y
0	1	1	1	X	Y	Y	X	Y	X	Y	X
1	0	0	0	Y	X	X	Y	X	Y	X	Y
1	0	0	1	Y	X	X	Y	X	Y	Y	X
1	0	1	0	Y	X	X	Y	Y	X	X	Y
1	0	1	1	Y	X	X	Y	Y	X	Y	X
1	1	0	0	Y	X	Y	X	X	Y	X	Y
1	1	0	1	Y	X	Y	X	X	Y	Y	X
1	1	1	0	Y	X	Y	X	Y	X	X	Y
1	1	1	1	Y	X	Y	X	Y	X	Y	X

Where X = V_{VAR} , Y = V_{EE}

Functional Schematic (SWD-119)



Ordering Information

Pin No.	Package
SWD-119 PIN	SOIC 8 Lead
SWD-119TR	Forward Tape and Reel
SWD-119RTR	Reverse Tape and Reel

AC Characteristics Over Guaranteed Operating Range⁴ (SWD-119)

Symbol	Parameter	$V_{OPT} - V_{EE}$	Max. Limits			Unit
			-55 to +25 °C	≤ +85 °C	≤ +125 °C	
T_{PLH}	Propagation Delay, I to either O	4.5	45	55	61	ns
		6.5	44	54	59	
		8.5	43	52	57	
T_{PHL}	Propagation Delay, I to either O	4.5	45	55	61	ns
		6.5	43	52	57	
		8.5	41	49	53	
T_{TLH}	Output Rising Transition Time	4.5	10.5	11.0	12.0	ns
		6.5	10.0	10.0	10.0	
		8.5	9.0	9.0	9.0	
T_{THL}	Output Falling Transition Time	4.5	10.0	10.0	11.0	ns
		6.5	9.0	9.0	9.0	
		8.5	8.0	8.0	8.0	
T_{skew}	Delay Skew, OA to OB	4.5	8.0	8.5	10.0	ns
		6.5	8.0	8.5	10.0	
		8.5	7.5	8.0	9.5	
C_{IN}	Input Capacitance	-	10	10	10	pF
C_{PDC}	Power Dissipation Capacitance ⁵	-	10	10	10	pF
C_{PDE}	Power Dissipation Capacitance ⁵	-	140	140	140	pF

4. $V_{CC} = 4.5V$, $V_{EE} = -4.5V$, $V_{OPT} = 0V$, $C_L = 25 pF$, T_{rise} , $T_{fall} = 6 ns$. These conditions represent the worst case for slow delays.5. Total Power Dissipation is calculated by the following formula: $PD = V_{CC}^2 f C_{PDC} + (V_{OPT} - V_{EE})^2 f C_{PDE}$

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