Frequency Multiplying, Peak Reducing EMI Solution

Features

- **Cypress PREMIS™ family offering**
- **Generates an EMI optimized clocking signal at the output**
- **Selectable output frequency range**
- **Single 1.25%, 2.5%, 5% or 10% down or center spread output**
- **Integrated loop filter components**
- **Operates with a 3.3 or 5V supply**
- **Low power CMOS design**
- **Available in 20-pin SSOP (Small Shrunk Outline Package)**

Key Specifications

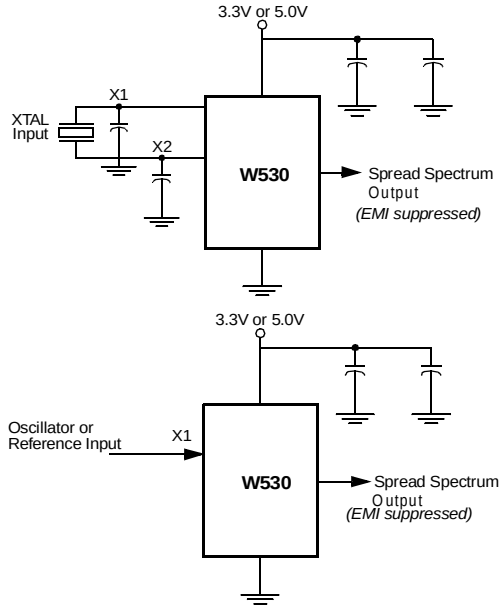
Supply Voltages: ..... V_{DD} = 3.3V±0.3V or V_{DD} = 5V±10%

Frequency range: .....13 MHz ≤ F_{in} ≤ 120 MHz

Cycle to Cycle Jitter: .....250 ps (max)

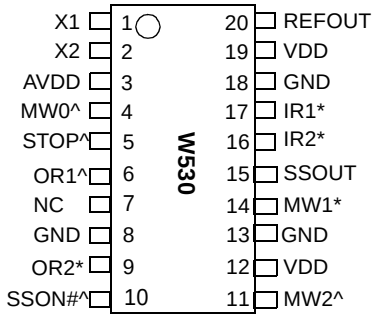
Output duty cycle: .....40/60% (worst case)

Simplified Block Diagram



Pin Configuration[1]

SSOP



Note:

1. Pins marked with ^ are internal pull-down resistors with weak 250 Ω. Pins marked with * are internal pull-up resistors with weak 250 Ω.

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Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
SSOUT	15	I	***Spread Spectrum Control.***
REFOUT	20	O	***Non-Modulated Output:*** This pin provides a copy of the reference frequency. This output will not have the Spread Spectrum feature enabled regardless of the state of logic input SSON#.
X1	1	I	***Crystal Connection or External Reference Frequency Input:*** This pin has dual functions. It may either be connected to an external crystal, or to an external reference clock.
X2	2	I	***Crystal Connection:*** Input connection for an external crystal. If using an external reference, this pin must be left unconnected.
SSON#	10	I	***Spread Spectrum Control (Active LOW):*** Asserting this signal (active LOW) turns the internal modulation waveform on. This pin has an internal pull-down resistor.
MW0:2	4, 14, 11	I	***Modulation Width Selection:*** When the Spread Spectrum feature is turned on, these pins are used to select the amount of variation and peak EMI reduction that is desired on the output signal. MW0: Down, MW1: Up, MW2: Down. (See *Table 2*.)
IR1:2	17, 16	I	***Reference Frequency Selection:*** Logic level provided at this input indicates to the internal logic what range the reference frequency is in and determines the factor by which the device multiplies the input frequency. Refer to *Table 1*. These pins have internal pull-up resistors.
OR1:2	6, 9	I	***Output Frequency Selection Bits:*** These pins select the frequency operation for the output. Refer to *Table 1*. OR1: DOWN, OR2: UP.
NC	7	NC	***No Connection:*** Leave this pin unconnected.
STOP	5	I	***Output Disable:*** When pulled HIGH, stops all outputs at logic low voltage level. This pin has an internal pull-down.
VDD	12, 19	P	***Power Connection:*** Connected to 3.3V or 5V power supply.
AVDD	3	P	***Analog Power Connection:*** Connected to 3.3V or 5V power supply.
GND	8, 13, 18	G	***Ground Connection:*** Connect all ground pins to the common ground plane.

Table 1. Frequency Configuration Table

Range of Fin Frequency		Multiplier Settings		Output / Input	Range of Fout		Required R Settings		Modulation & Power Down Settings	
Min.	Max.	OR2	OR1		Min.	Max.	IR2	IR1	MW2	MW1
14	30	0	1	1	14	30	0	1	*Table 2*	
14	30	1	0	2	28	60	0	1	*Table 2*	
14	30	1	1	4	56	120	0	1	*Table 2*	
25	60	0	1	0.5	13	30	1	0	*Table 2*	
25	60	1	0	1	25	60	1	0	*Table 2*	
25	60	1	1	2	50	120	1	0	*Table 2*	
50	120	0	1	0.25	13	30	1	1	*Table 2*	
50	120	1	0	0.5	25	60	1	1	*Table 2*	
50	120	1	1	1	50	120	1	1	*Table 2*	
Reserved		0	0	N/A	N/A	N/A	As Set	As Set	1	0
Power Down Hi-Z		0	0	N/A	N/A	N/A	As Set	As Set	1	1
Power Down 0		0	0	N/A	N/A	N/A	As Set	As Set	0	0
Power Down 1		0	0	N/A	N/A	N/A	As Set	As Set	0	1

Table 2. Modulation Percentage Selection Table

EMI Reduction	Modulation Setting		Bandwith Limit Frequencies as a % Value of Fout			
			MW0 = 0		MW0 = 1	
	MW2	MW1	Low	High	Low	High
Minimum EMI Control	0	0	98.75%	100%	99.375%	100.625%
Suggested Setting	0	1	97.5%	100%	98.75%	101.25%
Alternate Setting	1	0	95.0%	100%	97.5%	102.5%
Maximum EMI reduction	1	1	90.0%	100%	95%	105%

Overview

The W530 product is one of a series of devices in the Cypress PREMIS family. The PREMIS family incorporates the latest advances in PLL spread spectrum frequency synthesizer techniques. By frequency modulating the output with a low frequency carrier, peak EMI is greatly reduced. Use of this technology allows systems to pass increasingly difficult EMI testing without resorting to costly shielding or redesign.

In a system, not only is EMI reduced in the various clock lines, but also in all signals which are synchronized to the clock. Therefore, the benefits of using this technology increase with the number of address and data lines in the system. The Simplified Block Diagram shows a simple implementation.

Functional Description

The W530 uses a Phase Locked Loop (PLL) to frequency modulate an input clock. The result is an output clock whose frequency is slowly swept over a narrow band near the input signal. The basic circuit topology is shown in *Figure 1*. The input reference signal is divided by Q and fed to the phase detector. A signal from the VCO is divided by P and fed back to the phase detector also. The PLL will force the frequency of the VCO output signal to change until the divided output signal and the divided reference signal match at the phase detector input. The output frequency is then equal to the ratio of P/Q times the reference frequency. (Note: For the W530 the output frequency is nominally equal to the input frequency.) The unique feature of the Spread Spectrum Frequency Timing Generator is that a modulating waveform is superimposed at the input to the VCO. This causes the VCO output to be slowly swept across a predetermined frequency band.

Because the modulating frequency is typically 1000 times slower than the fundamental clock, the spread spectrum process has little impact on system performance.

Frequency Selection With SSFTG

In Spread Spectrum Frequency Timing Generation, EMI reduction depends on the shape, modulation percentage, and frequency of the modulating waveform. While the shape and frequency of the modulating waveform are fixed for a given frequency, the modulation percentage may be varied.

Using frequency select bits (FS2:1 pins), the frequency range can be set (see *Table 2*). Spreading percentage is set with pins MW as shown in *Table 2*.

A larger spreading percentage improves EMI reduction. However, large spread percentages may either exceed system maximum frequency ratings or lower the average frequency to a point where performance is affected. For these reasons, spreading percentage options are provided.

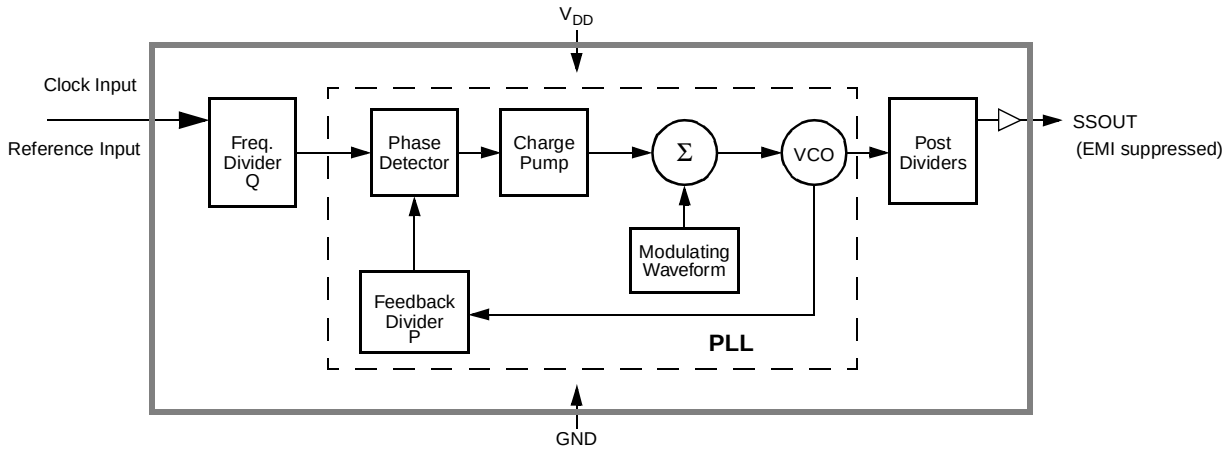


Figure 1. Functional Block Diagram

Spread Spectrum Frequency Timing Generator

The device generates a clock that is frequency modulated in order to increase the bandwidth that it occupies. By increasing the bandwidth of the fundamental and its harmonics, the amplitudes of the radiated electromagnetic emissions are reduced. This effect is depicted in *Table 2*.

As shown in *Table 2*, a harmonic of a modulated clock has a much lower amplitude than that of an unmodulated signal. The reduction in amplitude is dependent on the harmonic number and the frequency deviation or spread. The equation for the reduction is:

$$dB = 6.5 + 9*\log_{10}(P) + 9*\log_{10}(F)$$

Where *P* is the percentage of deviation and *F* is the frequency in MHz where the reduction is measured.

The output clock is modulated with a waveform depicted in *Figure 3*. This waveform, as discussed in “Spread Spectrum Clock Generation for the Reduction of Radiated Emissions” by Bush, Fessler, and Hardin, produces the maximum reduction in the amplitude of radiated electromagnetic emissions. The deviation selected for this chip is described in *Table 2*. *Figure 3* details the Cypress spreading pattern. Cypress does offer options with more spread and greater EMI reduction. Contact your local Sales representative for details on these devices.

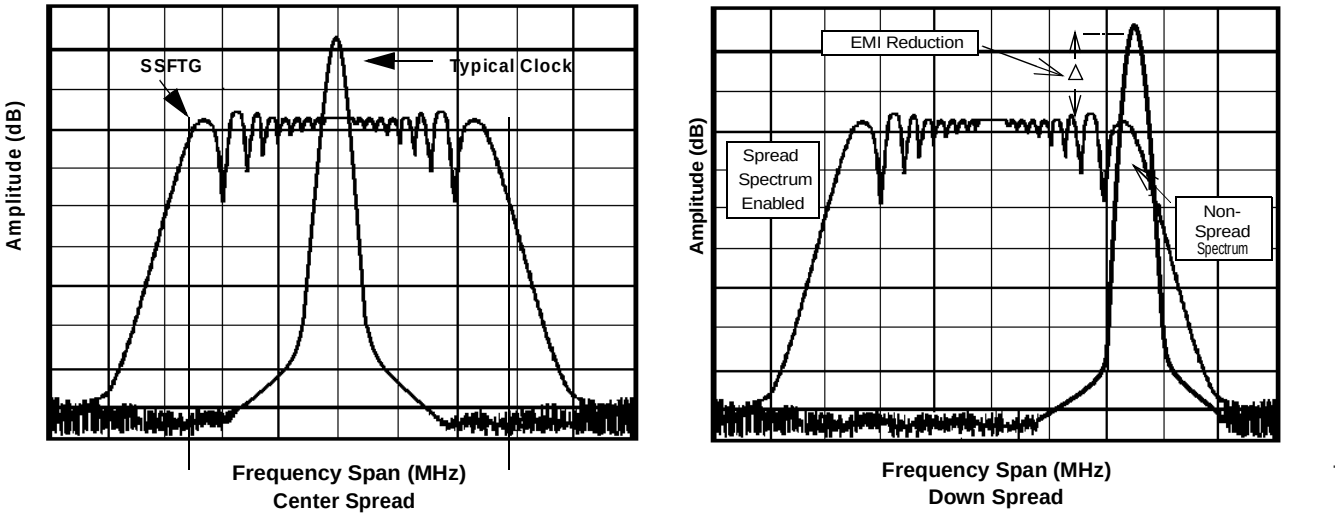


Figure 2. Clock Harmonic with and without SSCG Modulation Frequency Domain Representation

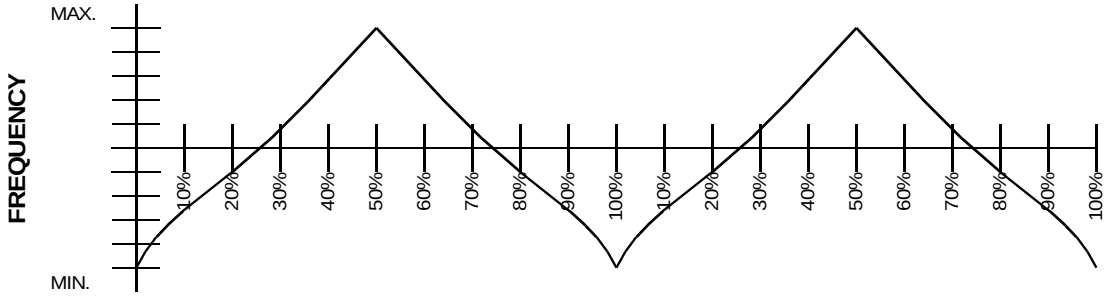


Figure 3. Typical Modulation Profile

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	0 to +70	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
P_D	Power Dissipation	0.5	W

DC Electrical Characteristics: $0°C < T_A < 70°C$, $V_{DD} = 3.3V \pm 0.3V$

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
I_{DD}	Supply Current			18	32	mA
t_{ON}	Power Up Time	First locked clock cycle after Power Good			5	ms
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.4			V
V_{OL}	Output Low Voltage				0.4	V
V_{OH}	Output High Voltage		2.4			V
I_{IL}	Input Low Current	Note 2			–100	µA
I_{IH}	Input High Current	Note 2			10	µA
I_{OL}	Output Low Current	@ 0.4V, V_{DD} = 3.3V		15		mA
I_{OH}	Output High Current	@ 2.4V, V_{DD} = 3.3V		15		mA
C_I	Input Capacitance				7	pF
R_P	Input Pull-Up Resistor			250		kΩ
Z_{OUT}	Clock Output Impedance			25		Ω

Note:
2. Inputs OR1:2 and IR1:2 have a pull-up resistor, Input SSON# has a pull-down resistor.

DC Electrical Characteristics: $0°C < T_A < 70°C$, $V_{DD} = 5V \pm 10\%$

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
I_{DD}	Supply Current			30	50	mA
t_{ON}	Power Up Time	First locked clock cycle after Power Good			5	ms
V_{IL}	Input Low Voltage				$0.15V_{DD}$	V
V_{IH}	Input High Voltage		$0.7V_{DD}$			V
V_{OL}	Output Low Voltage				0.4	V
V_{OH}	Output High Voltage		2.4			V
I_{IL}	Input Low Current	Note 2			–100	µA
I_{IH}	Input High Current	Note 2			10	µA
I_{OL}	Output Low Current	@ 0.4V, $V_{DD} = 5V$		24		mA
I_{OH}	Output High Current	@ 2.4V, $V_{DD} = 5V$		24		mA
C_I	Input Capacitance				7	pF
R_P	Input Pull-Up Resistor			250		kΩ
Z_{OUT}	Clock Output Impedance			25		Ω

AC Electrical Characteristics: $T_A = 0°C$ to $+70°C$, $V_{DD} = 3.3V \pm 0.3V$ or $5V \pm 10\%$

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
f_{IN}	Input Frequency	Input Clock	14		120	MHz
f_{OUT}	Output Frequency	Spread Off	13		120	MHz
t_R	Output Rise Time	15-pF load, 0.8V–2.4V		2	5	ns
t_F	Output Fall Time	15-pF load, 2.4 –0.8V		2	5	ns
t_{OD}	Output Duty Cycle	15-pF load	40		60	%
t_{ID}	Input Duty Cycle		40		60	%
t_{JCYC}	Jitter, Cycle-to-Cycle			250	300	ps

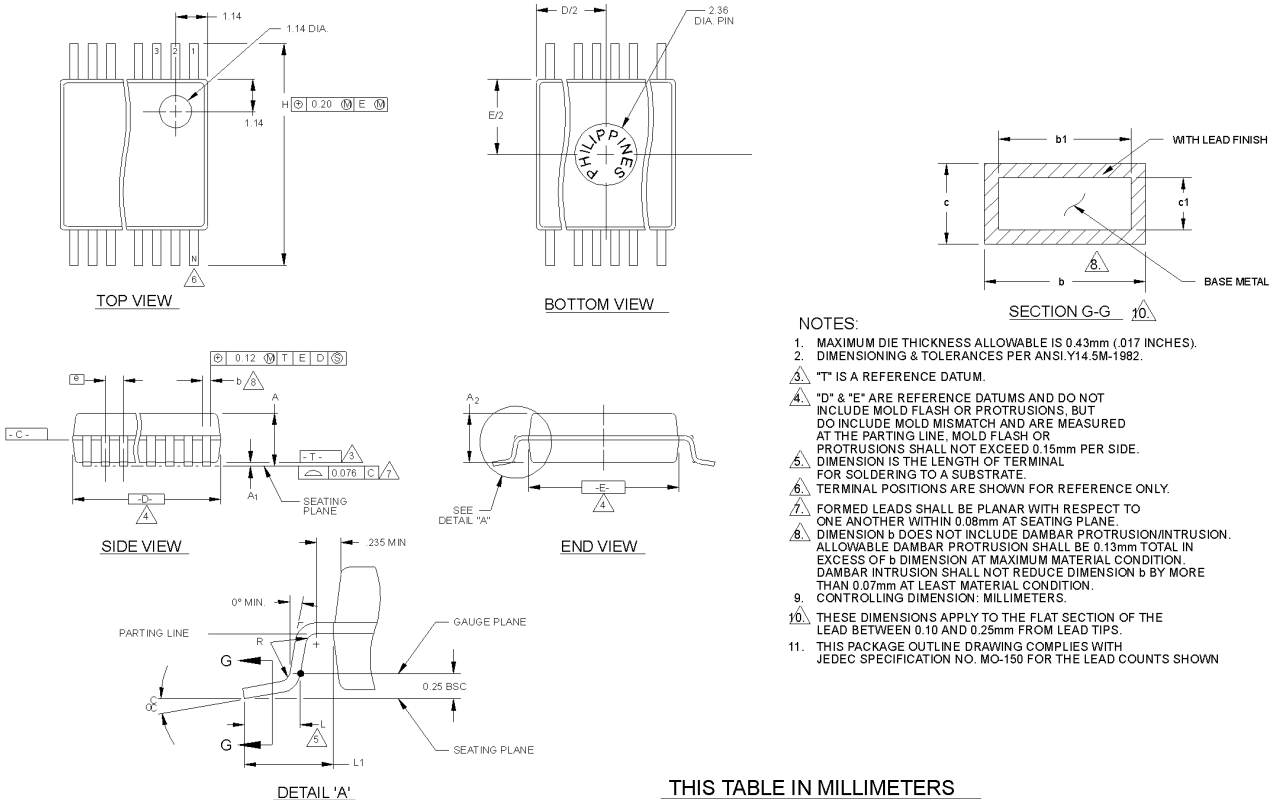
Ordering Information

Ordering Code	Package Name	Package Type
W530	H	20-Pin Plastic SSOP (209-mil)

Document #: 38-00913-*A

Package Diagram

20-Pin Small Shrink Outline Package (SSOP, 209-mil)



NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS 0.43mm (.017 INCHES).
2. DIMENSIONING & TOLERANCES PER ANSI.Y14.5M-1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE PARTING LINE, MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSION IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
7. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.08mm AT SEATING PLANE.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13mm TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN 0.07mm AT LEAST MATERIAL CONDITION.
9. CONTROLLING DIMENSION: MILLIMETERS.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25mm FROM LEAD TIPS.
11. THIS PACKAGE OUTLINE DRAWING COMPLIES WITH JEDEC SPECIFICATION NO. MO-150 FOR THE LEAD COUNTS SHOWN

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE	4			6
	MIN.	NOM.	MAX.		VARIATIONS	D MIN.	D NOM.	D MAX.	N
A	1.73	1.86	1.99		AA	6.07	6.20	6.33	14
A_1	0.05	0.13	0.21		AB	6.07	6.20	6.33	16
A_2	1.68	1.73	1.78		AC	7.07	7.20	7.33	20
b	0.25	-	0.38	8,10	AD	8.07	8.20	8.33	24
b1	0.25	0.30	0.33	10	AE	10.07	10.20	10.33	28
c	0.09	-	0.20	10	AF	10.07	10.20	10.33	30
c1	0.09	0.15	0.16	10					
D	SEE VARIATIONS			4					
E	5.20	5.30	5.38	4					
e	0.65 BSC								
H	7.65	7.80	7.90						
L	0.63	0.75	0.95	5					
L1	1.25 REF.								
N	SEE VARIATIONS			6					
cc	0°	4°	8°						
R	0.09	0.15							

VARIATION AF
IS DESIGNED BUT NOT TOOLED

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE	4			6
	MIN.	NOM.	MAX.		VARIATIONS	D MIN.	D NOM.	D MAX.	N
A	.068	.073	.078		AA	.239	.244	.249	14
A_1	.002	.005	.008		AB	.239	.244	.249	16
A_2	.066	.068	.070		AC	.278	.284	.289	20
b	.010	-	.015	8,10	AD	.318	.323	.328	24
b1	.010	.012	.013	10	AE	.397	.402	.407	28
c	.004	-	.008	10	AF	.397	.402	.407	30
c1	.004	.006	.006	10					
D	SEE VARIATIONS			4					
E	.205	.209	.212	4					
e	.0256 BSC								
H	.301	.307	.311						
L	.025	.030	.037	5					
L1	.049 REF.								
N	SEE VARIATIONS			6					
cc	0°	4°	8°						
R	.004	.006							