# Micro controller servo
## BU38905



The BU38905 is a servo controller for VCRs. It has a high-speed, 8-bit CPU and performs the processing required for the drum, capstan, FV and PV completely in software, allowing a large reduction in the number of external components required. It also has a high-performance linear amplifier so an interface IC is not required. Specialized hardware is included for items that require high-speed processing, to allow efficient utilization of the CPU. Timer and tuner functions are also built-in. The VCR control system can be performed by 1 chip.

### ●Applications
VHS VCRs and camcorders.

### ●Features
1)CPU
499 commands (69 types)
Memory-mapped I/O.
Minimum command execution time: 250ns (8MHz)
2)ROM capacity: 48152×8 bit.
3)RAM capacity: 896×8 bit.
4)Interrupts
Pattern generator: 2
Watchdog timer: 1
External interrupts: 2
FG interrupts: 5
Internal interrupts: 10
Two timers, one interval timer, two 0.5sec serial, VISS, linear time counter, two PTGs
※ Multi-layer interrupts possible.
5)Free-running counter: 19 bit
With 8-bit capture for remote control.
6)PWM output: 12 bit×2
For tuner: 14 bit×1
7)Pattern generator
16 bits from FRC MSB used.
Output
Internal: 4 bit
External (PO): 4 bit
External (special purpose): 4 bit
8)Programmable pre-scaler
For CFG: 7 bit
9)Head amplifier/chroma rotary
Generated from pattern generator output.
10) Built-in AGC. Five-bits used to switch the gain control registers for the CTL amplifier.
11)CTL counter: 1/30 or 1/25
12)Multiplication and division
24 bit×16 bit = 40 bit
16 bit ÷ 16 bit = 16 bit
13)Timer: 8 bit×2
14)Serial input/output: 8 bit×2
SIO2 has automatic transmission buffer.
15)VH PULSE
VSYNC separated from composite synchronous signal. Pseudo V generated from pattern generator output. Superimposed pseudo H synchronized with the composite synchronous signal.
16)VISS/VASS
VASS 0/1 discrimination
VISS discrimination: every 8 bits
Aspect discrimination: done in software
D/A CTL switching
17)Standard I/O
Parallel I/O (PIO): 32 bits
Parallel output (PO): 3 bits
Tri-state input (PI): 4 bits
Tri-state output (PO): 4 bits
18)A/D converter: 8 bits×12 channels
Automatic scanning.
19)Watchdog timer
Setting period: 4
20)Time counter
Interrupt generated every 0.5msec by dividing the 32.7kHz sub-clock.

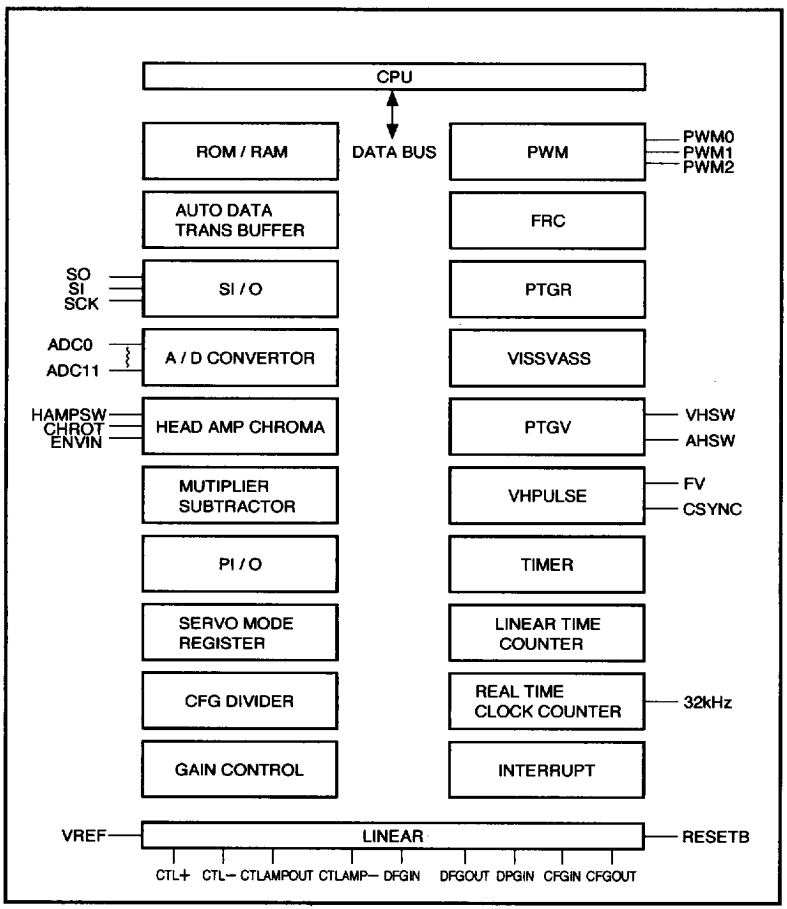
21)Power save

Switch to sub-clock by external interrupt (etc.). Low-power mode.

22)Linear circuits

DFG : amplifier/comparator
CFG : amplifier/comparator
CTL : differential amplifier/comparator
DPG : comparator

●Block diagram



## ●Absolute maximum ratings (Ta=25℃)

| Parameter | Symbol | Limits | Unit |
|---|---|---|---|
| Applied voltage | $V_{DD}$、$V_{DDA}$、$V_{DDB}$ | 0.3～7.0*2 | V |
| Input voltage | $V_{IN}$ | $V_{SS}$−0.3～$V_{DD}$+0.3 | V |
| Power dissipation | Pd | 500*1 | mW |
| Storage temperature | Tstg | −55～125 | ℃ |

*1 Reduced by 5mW for each increase in Ta of 1℃ over 25℃.
*2 Use with $V_{SS}$=$V_{SSA}$=$V_{SSB}$, and $V_{DD}$=$V_{DDA}$=$V_{DDB}$.

## ●Recommended operating conditions

| Parameter | Symbol | Limits | Unit |
|---|---|---|---|
| Power supply voltage | $V_{DD}$、$V_{DDA}$、$V_{DDB}$ | 4.5～5.5 | V |
| Clock frequency | $F_{CK}$ | 8 | MHz |
| Operating temperature | Topr | −25～75 | ℃ |

## ●Pin description

| Pin No. | Pin name | | Function |
|---|---|---|---|
| 1 | $V_{SS}$ | | Logic circuit GND |
| 2 | PO0*2 | PTGVD0 | Parallel output and pattern output |
| 3 | PO1*2 | PTGVD1 | |
| 4 | PO2*2 | PTGRD0 | |
| 5 | PO3*2 | PTGRD1 | |
| 6 | PO4*2 | FRC10 | Parallel output and FRC output |
| 7 | PO5*2 | PBCTL | Parallel output and PBCTL output |
| 8 | PO6*2 | CS2 | Parallel output and serial 2 chip select |
| 9 | SO2 | | Serial I/O2 data I/O |
| 10 | SCK2 | | Serial I/O2 clock I/O |
| 11 | SI1 | | Serial I/O1 data input |
| 12 | SO1*1 | PIO28 | Serial I/O1 data I/O |
| 13 | SCK1 | | Serial I/O1 clock I/O |
| 14 | AHSW*2 | PO7 | Parallel output and AHSW output |
| 15 | HAMPSW | | Head amplifier switch output |
| 16 | CHROT | | Chroma rotary switch output |
| 17 | CSYNC | | Composite signal logic input |
| 18 | FV | | Pseudo Vsync output |
| 19 | EXT1 | PI4 | Parallel input and external interrupt 1 |
| 20 | EXT2 (REM) | | External interrupt 2 |
| 21 | VHSW | | VHSW output |
| 22 | VDDA | | Linear, A/D circuit power supply |
| 23 | DPGIN | | Drum PG (PFG) comparator input |
| 24 | DFGIN | | Drum FG amplifier input |
| 25 | DFGOUT | | Drum FG amplifier output |
| 26 | CFGOUT | | Capstan FG amplifier output |
| 27 | CFGIN | | Capstan FG amplifier input |
| 28 | VREF | | Internal bias and power-on reset |
| 29 | CTLAMP− | | CTL amplifier - input |
| 30 | CTLAMPOUT | | CTL amplifier output |
| 31 | CTL− | | CTL coil - connection |
| 32 | CTL+ | | CTL coil + connection |
| 33 | $V_{SSA}$ | | Linear, A/D circuit GND |
| 34 | ADC0 | | A/D converter |
| 35 | ADC1 | | |

| Pin No. | Pin name | | Function |
|---|---|---|---|
| 36 | ADC2 | | A/D converter |
| 37 | ADC3 | | |
| 38 | ADC4 | | |
| 39 | ADC5 | | |
| 40 | ADC6 | | |
| 41 | ADC7 | | |
| 42 | $V_{DDB}$ | | PWM circuit power supply |
| 43 | $V_{SSB}$ | | PWM circuit power GND |
| 44 | RESETB | | Reset B |
| 45 | TEST | | TEST mode input (normally GND) |
| 46 | PWM0 | | PWM output |
| 47 | PWM1 | | |
| 48 | PWM2 | | |
| 49 | PIO36 | | Parallel I/O |
| 50 | PIO37 | | |
| 51 | PIO38 | | |
| 52 | PIO39 | | |
| 53 | PIO8 | ENVIN | Parallel I/O and ENVIN input |
| 54 | PIO9 | | Parallel I/O |
| 55 | PIO10 | | |
| 56 | PIO11 | | |
| 57 | PIO19 | | |
| 58 | PIO20 | | |
| 59 | PIO16 | | |
| 60 | VDD | | Logic circuit power supply |
| 61 | PIO17 | | Parallel I/O |
| 62 | PIO18 | | |
| 63 | PIO21 | | |
| 64 | PIO22 | | |
| 65 | PIO23 | | |
| 66 | PIO24 | | |
| 67 | PIO25 | | |
| 68 | PIO26 | | |
| 69 | PIO27 | | |
| 70 | PIO29 | | |

| Pin No. | Pin name | | Function |
|---|---|---|---|
| 71 | PIO30 | | Parallel I/O |
| 72 | PIO31 | | |
| 73 | PIO32 | | |
| 74 | PIO33 | | |
| 75 | PIO34 | | |
| 76 | PIO35 | | |
| 77 | CLOCKO1 | | For connection of main oscillator |
| 78 | CLOCKI1 | | |
| 79 | CLOCKI2 | | For connection of sub oscillator |
| 80 | CLOCKO2 | | |

*1 Output signal is xor. Does not become Hi-z even if there is PIO input.
*2 Output is or.

●Electrical characteristics (Unless otherwise specified: Ta=25℃, $V_{DD}$=5V and fosc=8MHz)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions | Measurement Circuit |
|---|---|---|---|---|---|---|---|
| [Logic block] | | | | | | | |
| Circuit current | $I_{DD}$ | — | 10.0 | 25.0 | mA | No load, when reset | Fig.1 |
| <Logic I/O> | | | | | | | |
| Output "H" voltage | $V_H$ | 4.0 | 4.5 | — | V | I=2mA | Fig.3 |
| Output "L" voltage | $V_L$ | — | 0.5 | 1.0 | V | I=2mA | Fig.3 |
| Input "H" voltage | $V_{IH}$ | 4.0 | — | — | V | | — |
| Input "L" voltage | $V_{IL}$ | — | — | 1.0 | V | | — |
| Input "H" current | $I_H$ | — | 0 | 1.0 | μA | Vin=$V_{DD}$ | Fig.4 |
| Input "L" current | $I_L$ | −1.0 | 0 | — | μA | Vin=0 | Fig.4 |
| <Serial I/O> | | | | | | | |
| Input data hold | $T_{SH}$ | 0.16 | — | — | μS | | — |
| Input data setup | $T_{SS}$ | 0.16 | — | — | μS | | — |
| Output data delay | $T_D$ | — | — | 0.3 | μS | Between clock and data | — |
| [Linear block] | | | | | | | |
| Circuit current | $I_{LI}$ | — | 12.0 | 35.0 | mA | No load | Fig.5 |
| <DFG> | | | | | | | |
| Amplifier gain setting range | $G_{DFG}$ | — | — | 50 | dB | | — |
| Comparator threshold | $V_{DFG}$ | ±80 | ±200 | ±360 | $mV_{PP}$ | | Fig.6 |
| <DPG> | | | | | | | |
| Comparator threshold + | $V_{DPG}$ | + 40 | +100 | +180 | $mV_{OP}$ | When positive polarity selected | Fig.7 |
| Comparator threshold − | $V_{DPG}$ | − 40 | −100 | −180 | $mV_{OP}$ | When negative polarity selected | Fig.7 |
| <CFG> | | | | | | | |
| Amplifier gain setting range | $G_{CFG}$ | — | — | 50 | dB | | — |
| Comparator threshold | $V_{CFG}$ | ±55 | ±135 | ±250 | $mV_{PP}$ | | Fig.8 |
| <CTL> | | | | | | | |
| Comparator threshold | $V_{CTL}$ | ±250 | ±480 | ±850 | $mV_{OP}$ | | Fig.10 |
| AGC H threshold | $V_{AGCH}$ | 920 | 1470 | 2000 | $mV_{OP}$ | | Fig.10 |
| AGC L threshold | $V_{AGCL}$ | 500 | 930 | 1480 | $mV_{OP}$ | | Fig.10 |
| <VREF> | | | | | | | |
| VREF pin voltage | $V_{REF}$ | 2.3 | 2.5 | 2.7 | V | No load | Fig.9 |
| [A/D block] | | | | | | | |
| Linearity error | $E_L$ | −3 | 0 | 3 | LSB | | Fig.11 |
| [Power-save mode block] | | | | | | Stop mode | |
| Circuit current 1 | $I_{DD1}$ | — | 10 | 25 | μA | No load, 32kHz oscillation, $V_{DD}$=3.0V | Fig.2 |
| Circuit current 2 | $I_{DD2}$ | — | 0 | 10 | μA | No load, 32kHz oscillation stopped | Fig.12 |

◎Not designed for radiation resistance.

## ●Measurement circuit

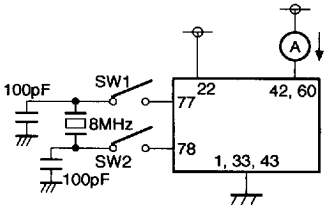



Fig.1

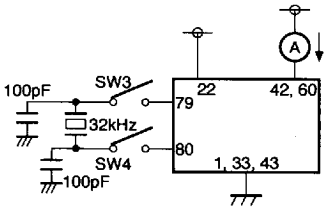



Fig.2

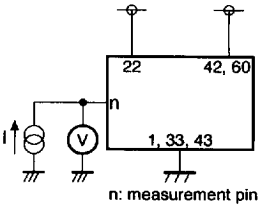



Fig.3

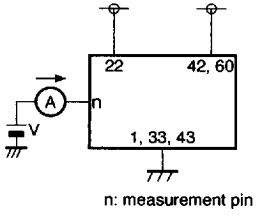



Fig.4

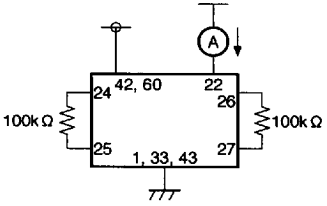



Fig.5

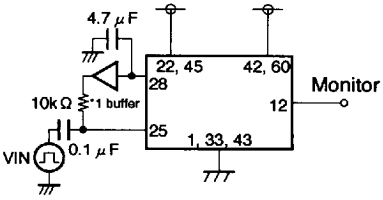



Fig.6

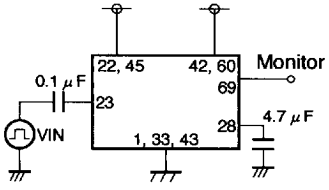



Fig.7

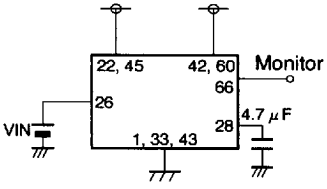



Fig.8

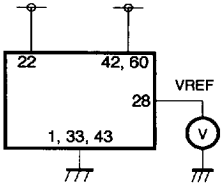



Fig.9

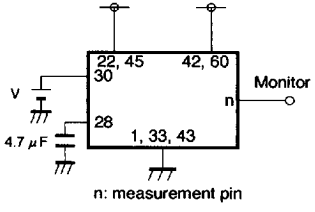



Fig.10

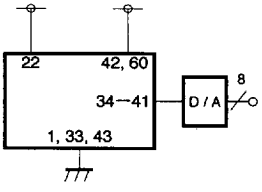



Fig.11

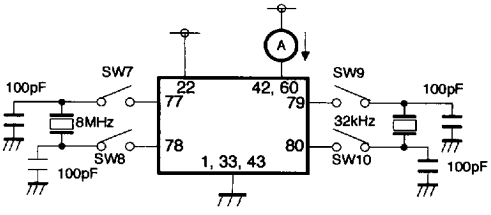



Fig.12

●Application example

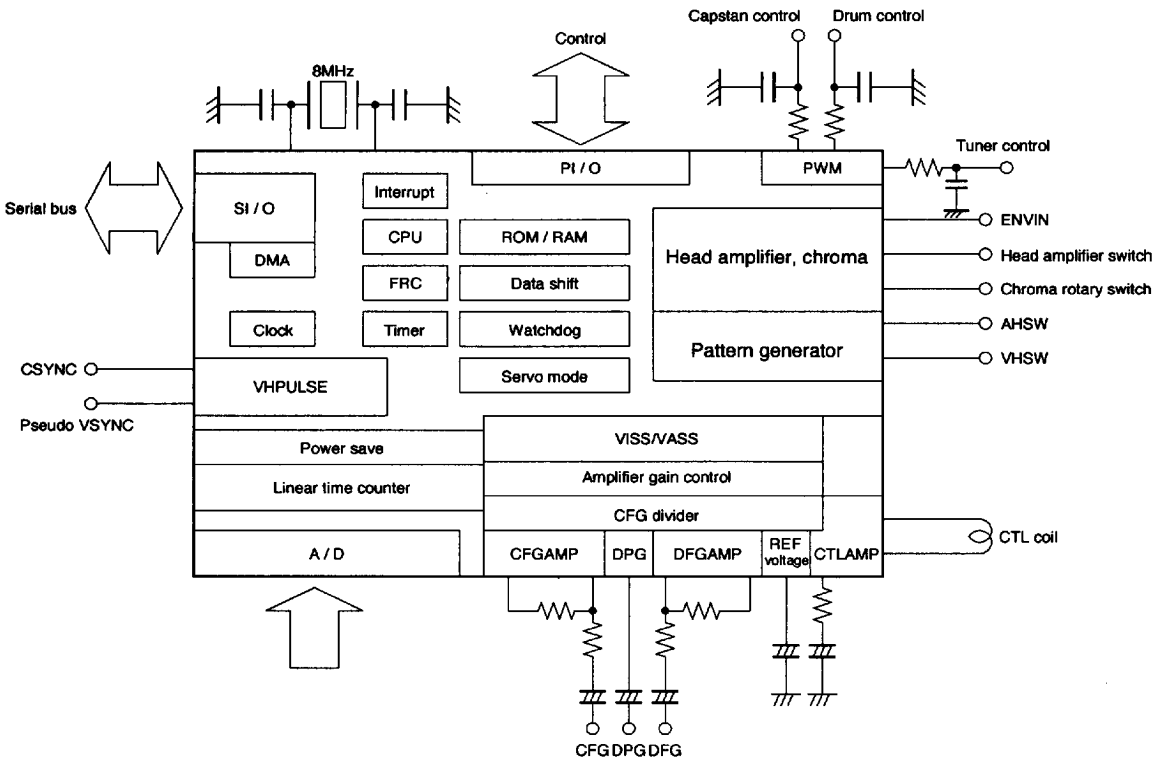



Fig.13

## ●Electrical characteristic curves

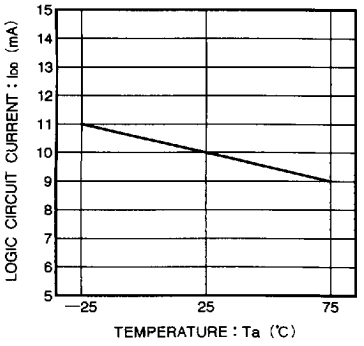



Fig. 14 Logic circuit current vs. temperature.

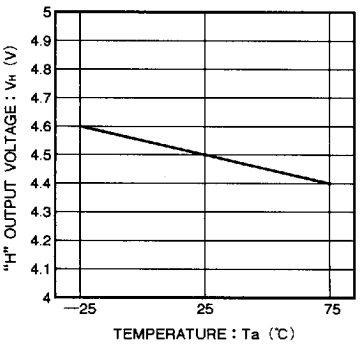



Fig. 15 Logic "H" output voltage vs. temperature.

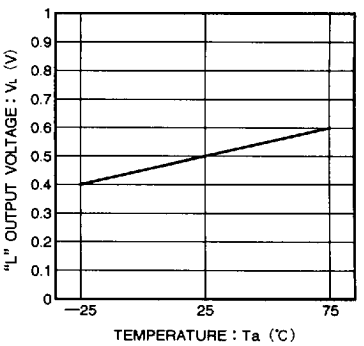



Fig. 16 Logic "L" output voltage vs. temperature.

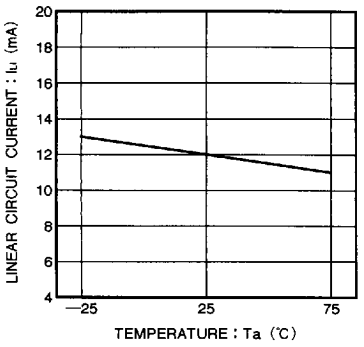
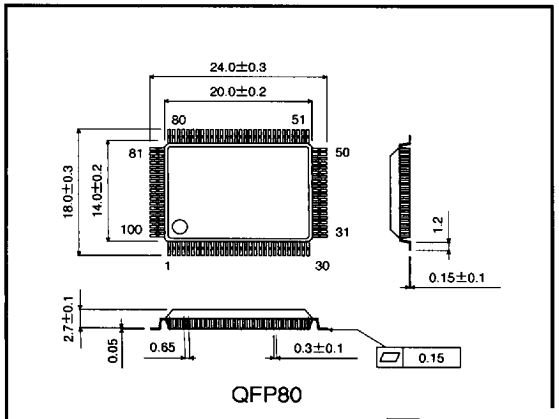



Fig. 17 Linear circuit current vs. temperature.

## ●External dimensions (Units: mm)




QFP80