

Data sheet	
status	Preliminary specification
date of issue	March 1991

BUK439-60A

PowerMOS transistor

T-39-15

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56E D ■ 7110826 0044554 867 ■ PHIN

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

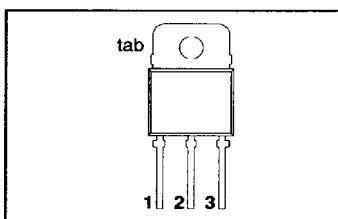
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	50	A
P_{tot}	Total power dissipation	230	W
$R_{DS(ON)}$	Drain-source on-state resistance	13.0	mΩ

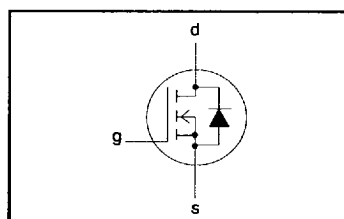
PINNING - SOT93

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	$T_{mb} = 25 \text{ }^\circ\text{C}$	-	50	A
I_D	Drain current (DC)	$T_{mb} = 100 \text{ }^\circ\text{C}$	-	50	A
I_{DM}	Drain current (pulse peak value)	$T_{mb} = 25 \text{ }^\circ\text{C}$	-	400	A
P_{tot}	Total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C}$	-	230	W
T_{slg}	Storage temperature	-	-55	150	$^\circ\text{C}$
T_j	Junction Temperature	-	-	150	$^\circ\text{C}$

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THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j-mb} = 0.54\text{ K/W}$
From junction to ambient	$R_{th\ j-a} = 45\text{ K/W}$

STATIC CHARACTERISTICS

 $T_{mb} = 25\text{ °C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.25\text{ mA}$	60	-	-	V
$V_{GS(TH)}$	Gate threshold voltage	$V_{DS} = V_{GS}; I_D = 1\text{ mA}$	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 60\text{ V}; V_{GS} = 0\text{ V}; T_J = 25\text{ °C}$	-	1	10	μA
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 60\text{ V}; V_{GS} = 0\text{ V}; T_J = 125\text{ °C}$	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 30\text{ V}; V_{DS} = 0\text{ V}$	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 50\text{ A}$	-	11.0	13.0	$\text{m}\Omega$

DYNAMIC CHARACTERISTICS

 $T_{mb} = 25\text{ °C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	$V_{DS} = 25\text{ V}; I_D = 50\text{ A}$	30	42	-	S
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz}$	-	5000	6500	pF
C_{oss}	Output capacitance		-	2000	2500	pF
C_{rss}	Feedback capacitance		-	1000	1500	pF
$t_{d\ on}$	Turn-on delay time	$V_{DD} = 30\text{ V}; I_D = 3\text{ A};$	-	70	120	ns
t_r	Turn-on rise time	$V_{GS} = 10\text{ V};$	-	250	350	ns
$t_{d\ off}$	Turn-off delay time	$R_{GS} = 50\ \Omega;$	-	400	500	ns
t_f	Turn-off fall time	$R_{gen} = 50\ \Omega$	-	400	500	ns
$t_{d\ on}$	Turn-on delay time	$V_{DD} = 30\text{ V}; I_D = 50\text{ A};$	-	15	20	ns
t_r	Turn-on rise time	$V_{GS} = 10\text{ V};$	-	60	90	ns
$t_{d\ off}$	Turn-off delay time	$R_{GS} = 4.7\ \Omega;$	-	40	60	ns
t_f	Turn-off fall time	$R_{gen} = 4.7\ \Omega$	-	50	80	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	12.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

 $T_{mb} = 25\text{ °C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	50	A
I_{DRM}	Pulsed reverse drain current	-	-	-	400	A
V_{SD}	Diode forward voltage	$I_F = 50\text{ A}; V_{GS} = 0\text{ V}$	-	1.1	1.5	V
t_{rr}	Reverse recovery time	$I_F = 50\text{ A}; -di_F/dt = 100\text{ A}/\mu\text{s};$	-	150	-	ns
Q_{rr}	Reverse recovery charge	$V_{GS} = 0\text{ V}; V_R = 30\text{ V}$	-	0.6	-	μC

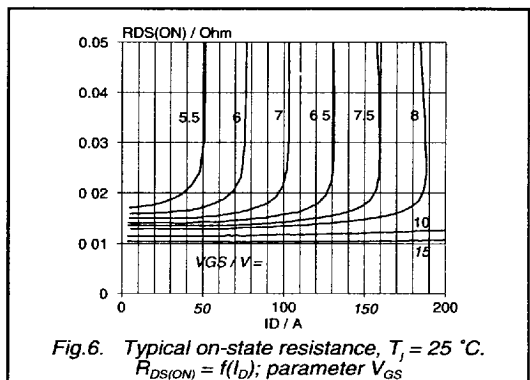
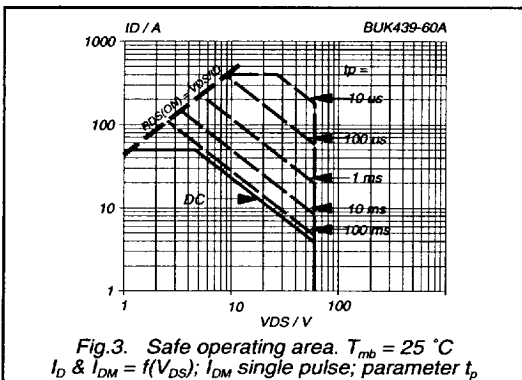
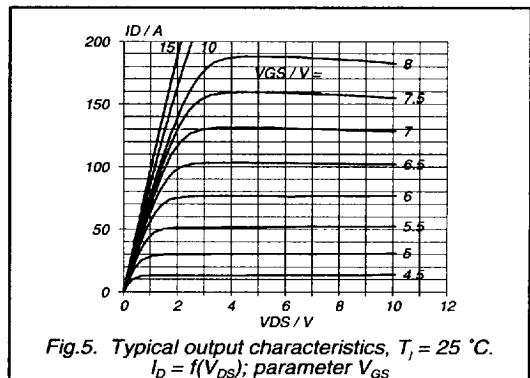
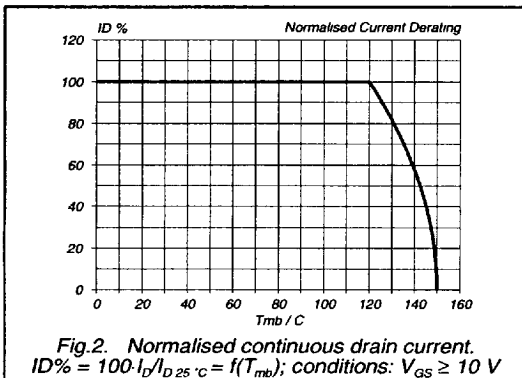
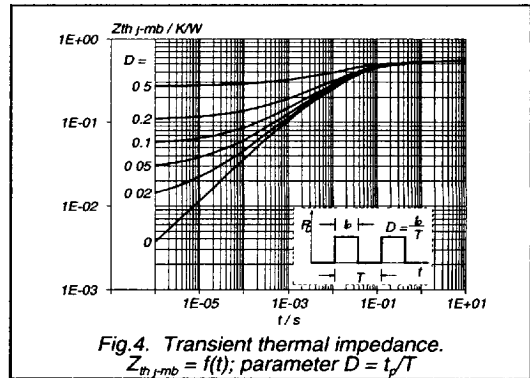
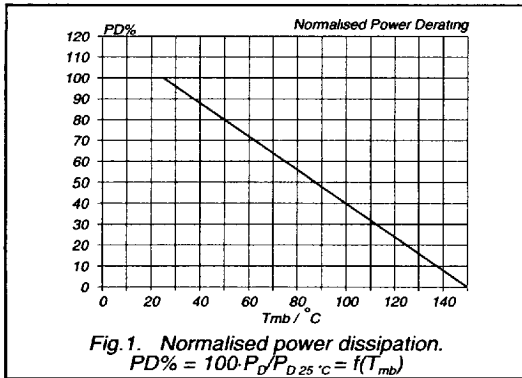
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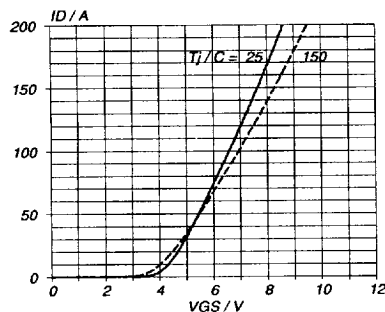


Fig. 7. Typical transfer characteristics.
 $I_D = f(V_{GS})$; conditions: $V_{DS} = 25 \text{ V}$; parameter T_J

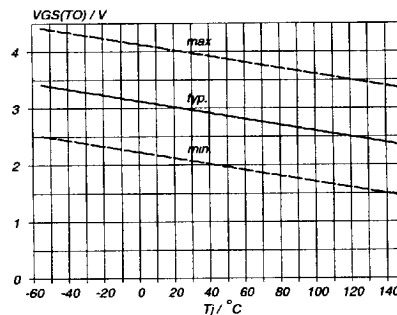


Fig. 10. Gate threshold voltage.
 $V_{GS(T0)} = f(T_J)$; conditions: $I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$

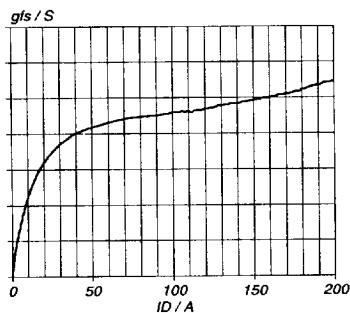


Fig. 8. Typical transconductance, $T_J = 25^\circ\text{C}$.
 $g_{fs} = f(I_D)$; conditions: $V_{DS} = 15 \text{ V}$

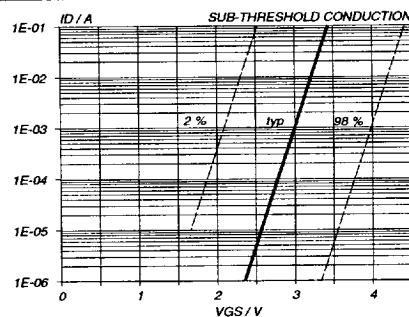


Fig. 11. Sub-threshold drain current.
 $I_D = f(V_{GS})$; conditions: $T_J = 25^\circ\text{C}$; $V_{DS} = V_{GS}$

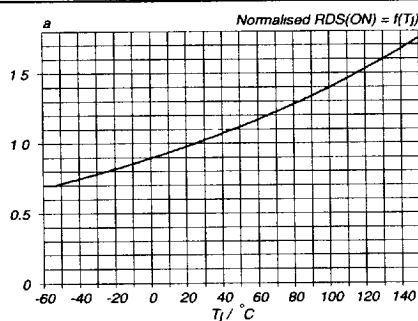


Fig. 9. Normalised drain-source on-state resistance.
 $a = R_{DS(ON)}/R_{DS(ON)25^\circ\text{C}} = f(T_J)$; $I_D = 50 \text{ A}$; $V_{GS} = 10 \text{ V}$

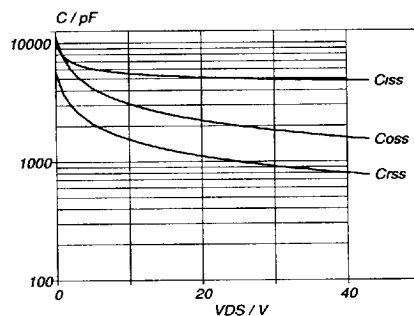


Fig. 12. Typical capacitances, C_{iss} , C_{oss} , C_{rss} .
 $C = f(V_{DS})$; conditions: $V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$

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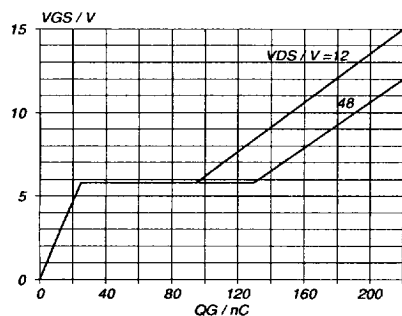


Fig. 13. Typical turn-on gate-charge characteristics.
 $V_{GS} = f(Q_G)$; conditions: $I_D = 50$ A; parameter V_{DS} .

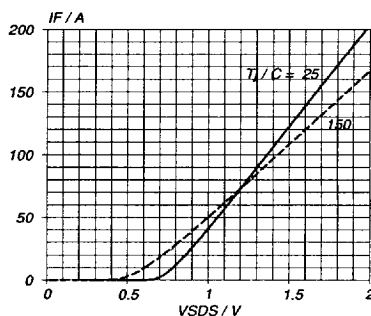


Fig. 14. Typical reverse diode current.
 $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_J .