T-39-15

Philips Components

Data sheet	
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date of issue	March 1991

BUK 539-60A
PowerMOS transistor
Logic level FET

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope. The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

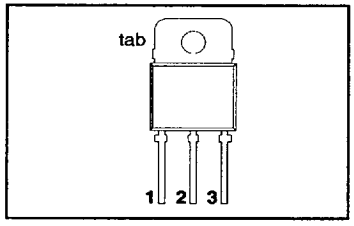
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	50	A
P_{tot}	Total power dissipation	230	W
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 5 V	15.0	mΩ

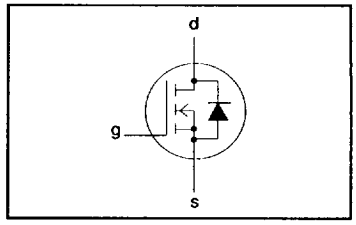
PINNING - SOT93

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50$ µs	-	20	V
I_D	Drain current (DC)	T_{mb} = 25 °C	-	50	A
I_D	Drain current (DC)	T_{mb} = 100 °C	-	50	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	-	400	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	-	230	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Junction Temperature	-	-	150	°C

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THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 0.54 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 45 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	60	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V; V_{GS} = 0 V; T_j =125 °C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 50 A	-	12.0	15.0	mΩ

DYNAMIC CHARACTERISTICS

Tmb = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 50 A	40	60	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	5800	7100	pF
C_{oss}	Output capacitance		-	2000	2500	pF
C_{rss}	Feedback capacitance		-	1000	1500	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	70	120	ns
t_r	Turn-on rise time	V_{GS} = 5 V;	-	250	350	ns
$t_{d\ off}$	Turn-off delay time	R_{GS} = 50 Ω;	-	600	750	ns
t_f	Turn-off fall time	R_{gen} = 50 Ω	-	400	500	ns
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 50 A;	-	15	25	ns
t_r	Turn-on rise time	V_{GS} = 5 V;	-	100	130	ns
$t_{d\ off}$	Turn-off delay time	R_{GS} = 4.7 Ω;	-	60	100	ns
t_f	Turn-off fall time	R_{gen} = 4.7 Ω	-	80	120	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	12.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

Tmb = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	50	A
I_{DRM}	Pulsed reverse drain current	-	-	-	400	A
V_{SD}	Diode forward voltage	I_F = 50 A ; V_{GS} = 0 V	-	1.1	1.5	V
t_{rr}	Reverse recovery time	I_F = 50 A; -dI_F/dt = 100 A/µs;	-	150	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.6	-	µC

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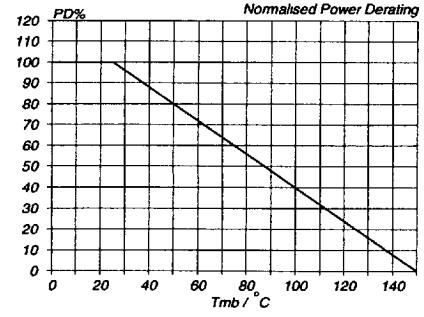

Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\,25\,°C}$ = f(T_{mb})

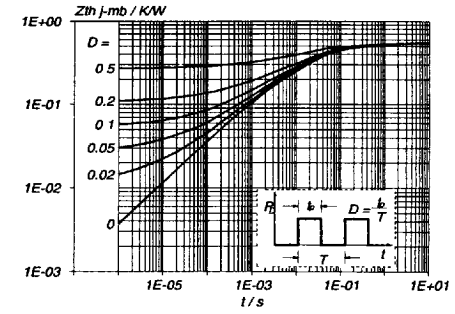

Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb}$ = f(t); parameter D = t_p/T

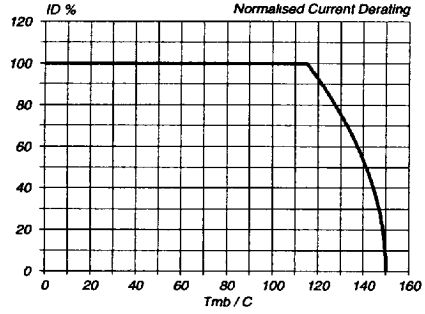

Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\,25\,°C}$ = f(T_{mb}); conditions: V_{GS} ≥ 10 V

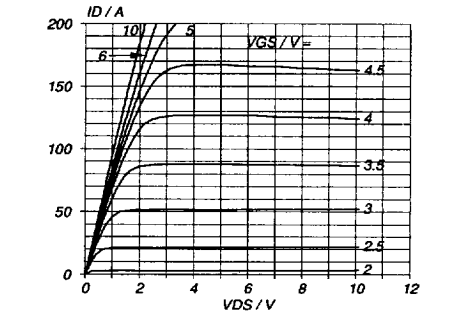

Fig.5. Typical output characteristics, T_j = 25 °C.
I_D = f(V_{DS}); parameter V_{GS}

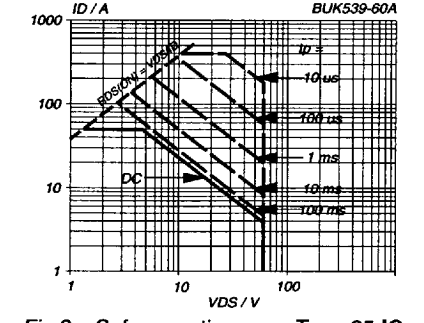

Fig.3. Safe operating area. T_{mb} = 25 °C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

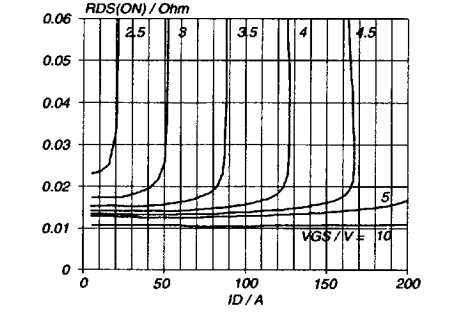

Fig.6. Typical on-state resistance, T_j = 25 °C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

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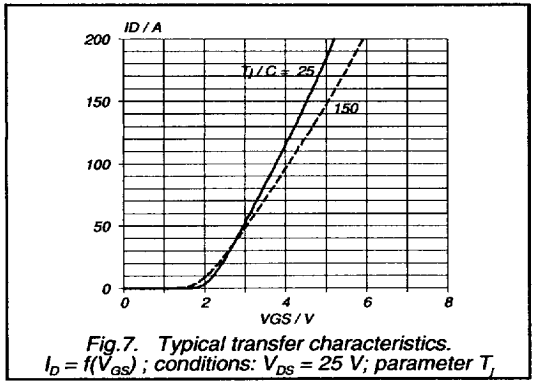

Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

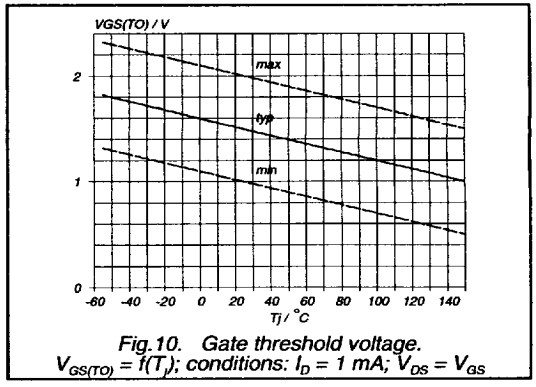

Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

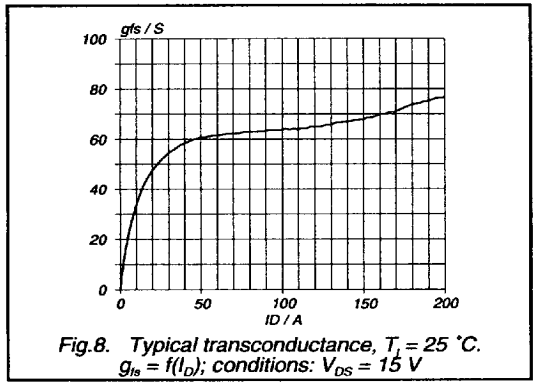

Fig.8. Typical transconductance, T_j = 25 °C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 15 V

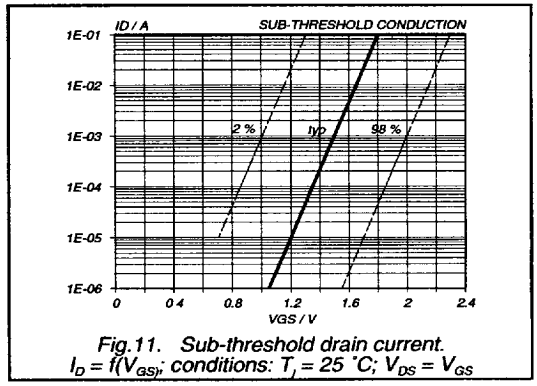

Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 °C; $V_{DS} = V_{GS}$

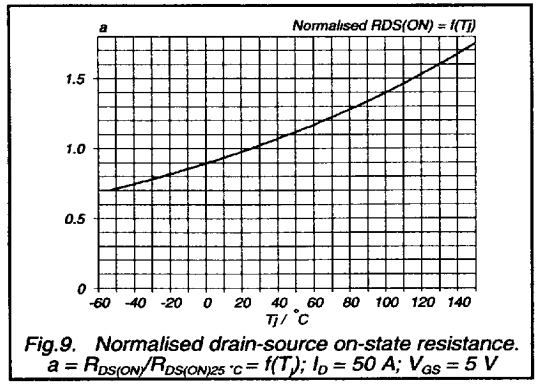

Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,°C} = f(T_j)$; I_D = 50 A; V_{GS} = 5 V

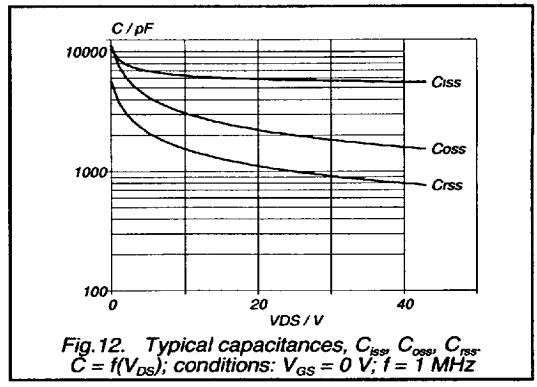

Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

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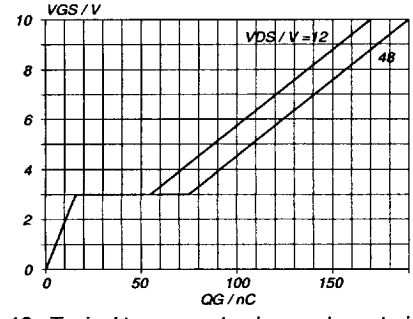

Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; conditions: $I_D = 50$ A; parameter V_{DS}

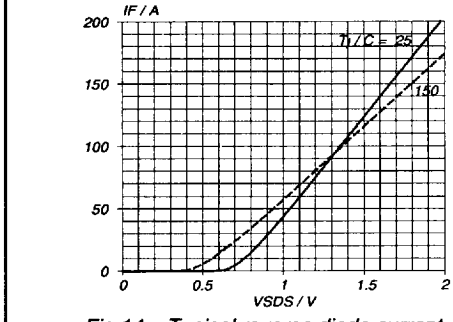

Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j