CMD

Microcircuits

C3052
C3053
C3054
C3057

CMOS Monolithic Serial Interface PCM Codec/Filter Family

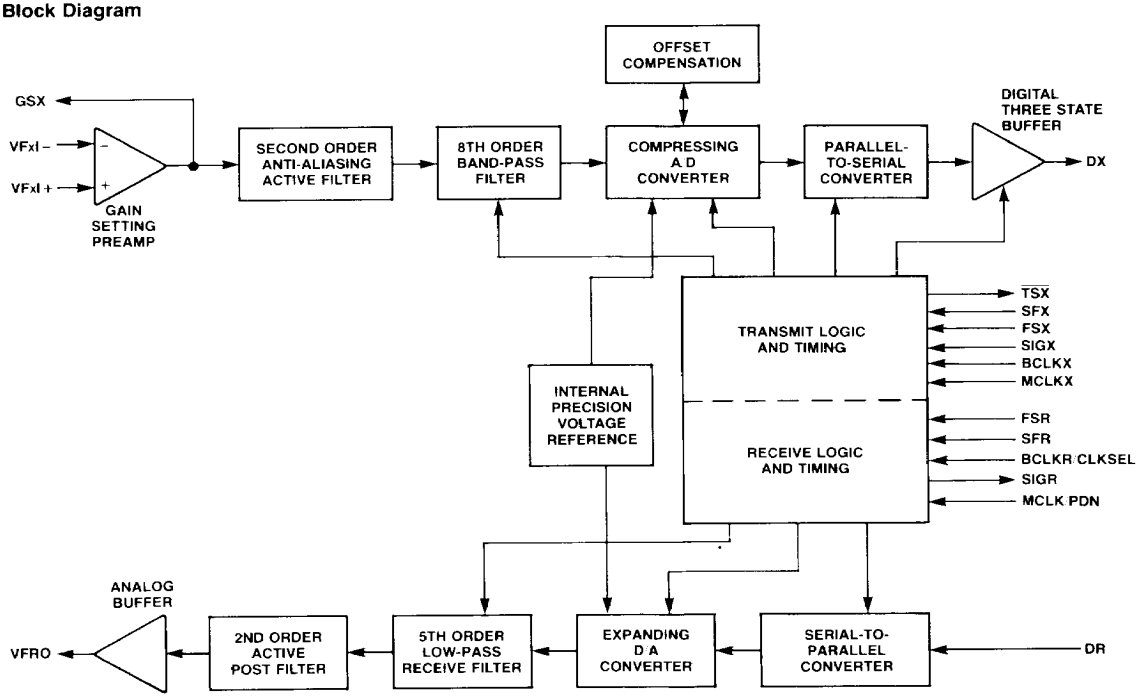
General Description

CMD's family of CMOS monolithic μ-law and A-law CODEC/filter circuits provide precision A/D and D/A signal conversion as well as the transmit and receive filtering required for companded PCM systems. Within each device, the encode section features an input gain adjust amplifier, an active RC anti-aliasing filter, offset compensation circuitry, and a switched-capacitor band-pass filter for rejecting frequencies outside a 200 to 3400 Hz band. Filtered signals are sampled and encoded into the compressed μ-law or A-law format and shifted out through the serial interface. The decode section features an expanding decoder for reconstructing the μ-law or A-law encoded signal, a low-pass filter with Sin x/x correction followed by an active RC smoothing filter, and a output power amplifier capable of driving low impedance loads. All devices within the CMD CODEC/filter family meet or exceed AT&T D3/D4 and CCITT specifications, and are manufactured using CMD's state-of-the-art CMOS process technology for increased noise immunity, higher reliability and reduced power consumption.

Features

- Four complete CODEC/filtering systems:
  - — C3052 — μ-law with signaling (18 pin version)
  - — C3053 — μ-law with signaling (20 pin version)
  - — C3054 — μ-law without signaling (16 pin version)
  - — C3057 — A-law (16 pin version)
- Pin compatible with industry standard (3052,53,54,57)
- Low power CMOS design; 60 mW operating (typ), 3 mW standby (typ)
- Low-pass and high-pass transmit filtering
- Receive low-pass filtering with Sin x/x correction
- Resistor programmable gain setting preamp for transmit section
- Synchronous or asynchronous transmit and receive operation
- Serial I/O interface
- 1.536 MHz, 1.544 MHz, or 2.048 MHz master clock timing; variable bit clock timing from 64 KHz to 2.048 MHz
- Short and long frame sync timing
- Active RC anti-aliasing and post filters
- Precision internal voltage reference and offset compensation circuits
- Automatic power-down by removing frame sync's and/or single pin power-down
- TTL or CMOS compatible interface
- ± 5V power input

Block Diagram



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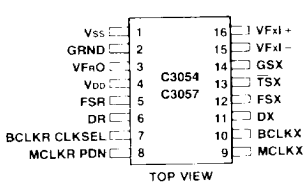
Pin Function Table

Pin	Description
V_{SS}	Negative power supply. V_{SS} = −5V ± 5%
GRND	Ground reference for all signals. Internally connected to both analog and digital ground.
VF_{RO}	Receive channel analog output.
V_{DD}	Positive power supply. V_{DD} = +5V ± 5%
FSR	Receive channel 8 KHz frame synchronization pulse input. Sync'd with receive bit clock, this signal determines when PCM data is to be shifted into the receive channel data input, DR. This pin may also be used to specify short frame sync receive signaling frames in the 18 and 20 pin signaling devices (C3052 and C3053).
DR	Receive channel data input. PCM data will be clocked into DR on the eight consecutive clocks of BCLKR following the FSR rising edge. See timing diagrams.
BCLKR/ CLKSEL	Receive channel bit clock input. BCLKR is used to shift PCM data into the receive channel data input, DR. BCLKR may vary from 64 KHz to 2.048 MHz but must be synchronous with MCLKR and FSR. In synchronous operation, this pin is used as a logic input to specify the master clock frequency (Table 1). In this case, BCLKX is used for both the transmit and receive channel bit clocks.
MCLKR/ PDN	Receive channel master clock input. MCLKR must be 1.536 MHz, 1.544 MHz, or 2.048 MHz. In synchronous operation, this pin is used as a power-down control. In this case, MCLKX is used for both transmit and receive master clocks and MCLKR/PDN is connected continuously low. When MCLKR/PDN is connected high, the device is powered down.
MCLKX	Transmit channel master clock input. May be 1.536 MHz, 1.544 MHz, or 2.048 MHz. In synchronous operation, MCLKX is used for all internal master clock timing (both transmit and receive).
BCLKX	Transmit channel bit clock input. BCLKX is used to shift out the PCM data at the transmit channel output, DX. BCLKX may vary from 64 KHz to 2.048 MHz, but must be synchronous with MCLKX and FSX. In synchronous operation, BCLKX is used for all internal bit clock timing (both transmit and receive).
DX	Transmit channel data output. PCM data is shifted out of this three-state output on the eight consecutive transmit bit clocks following a rising edge of FSX. See timing diagrams.
FSX	Transmit channel 8 KHz frame synchronization pulse input. Sync'd with BCLKX, this signal determines when the encoded PCM data is shifted out the transmit channel data output, DX. This pin may also be used to specify short frame sync transmit signaling frames in the 18 and 20 pin signaling devices (C3052 and C3053).
$\overline{TSX}$	Transmit channel timeslot indicator output. This active low open drain output pulses low during output of valid transmit data.
GSX	Analog output of the transmit channel input gain-adjust amplifier. GSX may be used to externally set gain of the transmit channel. Connected externally to VFxI− for a gain of 1.
VFxI−	Inverting input to the transmit channel input gain-adjust amplifier.
VFxI+	Non-inverting input to the transmit channel input gain-adjust amplifier.
SIGR	Receive channel signaling bit output. During a receive signaling frame, the eighth bit of the incoming PCM data is output at SIGR. This output pin is only used in the 18 and 20 pin signaling devices (C3052 and C3053).
SIGX	Transmit channel signaling bit input. During a transmit signaling frame, data at this input is transmitted as the eighth bit of the PCM word at the transmit data output, DX. This input pin is only used in the 18 and 20 pin signaling devices (C3052 and C3053). If not used, this pin should be left open circuit or tied high.
SFR	Receive channel signaling frame sync input. This pin is only used in the 20 pin signaling version (C3053). It is used to specify a long frame sync receive signaling frame. When high during FSR, the eighth bit of the incoming PCM word is output at SIGR. If not used, this pin should be left open circuit or tied low.
SFX	Transmit channel signaling frame sync input. This pin is only used in the 20 pin signaling version (C3053). It is used to specify a long frame sync transmit signaling frame. When high during FSX, data at SIGX is inserted into the eighth bit of the PCM word. If not used, this pin should be left open circuit or tied low.

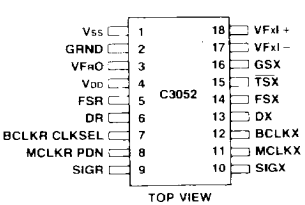
Pin Configurations

Dual-In-Line Package



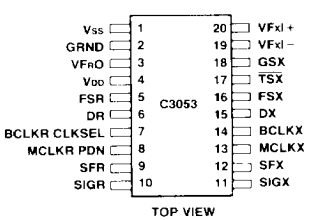
TOP VIEW

Dual-In-Line Package



TOP VIEW

Dual-In-Line Package



TOP VIEW

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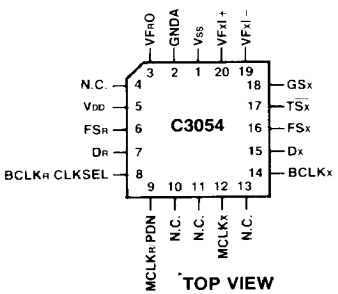
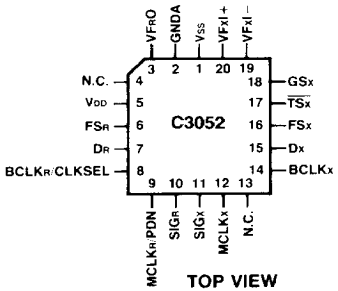
Pin Configurations (Continued)

Plastic Chip Carriers



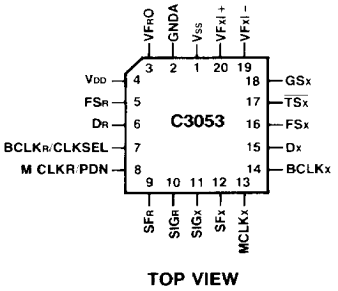
TOP VIEW

Plastic Chip Carriers



TOP VIEW

Plastic Chip Carriers



TOP VIEW

Functional Description

Power-up/Power-down

When power is first applied, this device immediately goes into power-down mode. In power-down mode, all circuits except those required for power-up are deactivated and DX and VFRO outputs are placed in high impedance states. Minimum power is consumed in this mode as the device waits to power up.

In synchronous operation, the device can be powered up by pulsing FSX and/or FSR while applying a TTL or CMOS low level to MCLKR/PDN. In asynchronous operation, the device is powered up by pulsing FSX and/or FSR while a clock is applied to the MCLKR/PDN pin. In either case, the PCM data output, DX, will be valid after the second FSX pulse.

The device is automatically powered down in the absence of both FSX and FSR pulses. Approximately 1.5 ms after both FSX and FSR are continuously low, the device goes into power-down mode. In addition, the device can be powered down at any time by applying a TTL or CMOS high level to the MCLKR/PDN pin.

Synchronous and Asynchronous Operation

The C3052 series CODEC/filters may operate in synchronous or asynchronous mode. Synchronous operation is when MCLKX and BCLKX are used as the master clocks and bit clocks, respectively, for both the transmit and receive channels. This allows MCLKR/PDN to be used as a power-down control and BCLKR/CLKSEL to be used to specify the master clock frequency. Internal circuitry detects if clocks are present on MCLKR/PDN and BCLKR/CLKSEL and if not, MCLKX and BCLKX are automatically used for both transmit and receive sections. MCLKX may be 1.536 MHz, 1.544 MHz, or 2.048 MHz. BCLKX may be from 64 KHz to 2.048 MHz.

Asynchronous operation is when separate transmit and receive master clocks and transmit and receive bit clocks are applied. In this mode, MCLKX and MCLKR must be 1.536 MHz or 1.544 MHz for the μ-law devices, and must be 2.048 MHz for the A-law devices. BCLKX and BCLKR may vary from 64 KHz to 2.048 MHz.

In either mode of operation, FSX must be synchronous with BCLKX and MCLKX. FSR must be synchronous with BCLKR and MCLKR. When operating in the synchronous mode, the BCLKR/CLKSEL pin should be used to specify the master clock frequencies. If the master clock frequency is 1.536 MHz or 1.544 MHz, BCLKR/CLKSEL should be connected high for μ-law devices and low for A-law devices. If the master clock frequency is 2.048 MHz, BCLKR/CLKSEL should be connected low for μ-law and high for A-law. If the BCLKR/CLKSEL input is being clocked, the master clock must be 1.536 MHz or 1.544 MHz for μ-law and 2.048 MHz for A-law. The following table summarizes what the master clock frequencies must be depending on the state of the BCLKR/CLKSEL pin.

Table 1. Master clock frequency specification

BCLKR/CLKSEL		Master clock frequency
1	(μ-law versions)	1.536 MHz or 1.544 MHz*
0	(μ-law versions)	2.048 MHz
clocked	(μ-law versions)	1.536 MHz or 1.544 MHz
1	(A-law version)	2.048 MHz
0	(A-law version)	1.536 MHz or 1.544 MHz
clocked	(A-law version)	2.048 MHz

*Note that the device automatically compensates for the 193rd clock pulse in each frame for the 1.544 MHz master clock.

Short and Long Frame Sync's

The CODEC/filter will operate with either short or long frame sync pulses. A short frame sync pulse is one bit clock period long (or two, for short frame signaling). A long frame sync pulse is three or more bit clock periods long. Upon power initialization, the device assumes short frame sync timing. The CODEC/filter will use the transmit frame sync pulse, FSX, to determine whether short or long frame sync's are being applied. Thus both transmit and receive channels must use the same length frame sync pulse. All 4 versions of the CODEC/filter operate in either short or long frame mode. Details of short and long frame timing are specified in the 'CODEC/filter Timing' section.

Signaling

The C3052 and the C3053 CODEC/filters contain circuitry to extract signaling information in the PCM data stream. During a transmit signaling frame, the encoder encodes the incoming analog signal and inserts the data present on the SIGX pin in place of the least significant (eighth) bit of the encoded PCM word. The 7 encoded bits of the PCM word and the signaling bit are shifted out through DX. Similarly, during a receive signaling frame, the least significant bit of the PCM word read in from DR, is latched and stored on the SIGR output pin until updated at the end of the next signaling frame. The decoder interprets the lost LSB as "1/2" to minimize noise and distortion.

Signaling in short frame sync mode may be performed by either the 18 pin signaling device (C3052) or the 20 pin signaling device (C3053). If the 20 pin signaling device is used, then pins SFX and SFR are not used and must be connected low or left open circuit. A frame sync pulse two bit clock periods long is used to indicate a signaling frame.

Signaling in long frame sync mode can only be performed by using the 20 pin signaling device (C3053). The two extra pins, SFX and SFR, are used to indicate signaling frames. A pulse on SFX indicates a transmit signaling frame and a pulse on SFR indicates a receive signaling frame.

Transmit Channel Operation

Gain Setting Input Amplifier — The transmit channel input is a gain setting input amplifier which can be used for passband gain adjustment (see Figure 1). It can be connected to provide a gain of 20 dB without degrading the noise performance of the filter. The amplifier can be used in the inverting or differential amplifier mode.

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Functional Description (Continued)

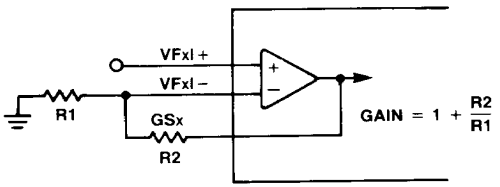

Figure 1. Transmit Filter Gain Adjustment

Transmit Filter — Before the incoming analog signal is sampled and encoded, a transmit filter bandlimits the signal to 4 KHz and rejects any 50 Hz and 60 Hz components. A minimum attenuation of 30 dB and 26 dB is provided at 50 Hz and 60 Hz, respectively. The transmit filter consists of an active RC anti-aliasing filter followed by an 8th order switched capacitor bandpass filter. The bandpass filter consists of a 5th order lowpass and 3rd order highpass section. The transmit filter provides a passband flatness and stopband attenuation which exceeds the Bell D3 and D4 specifications as well as the CCITT G.712 recommendations.

μ-law/A-law Encoder — The encoding begins with the transmit frame sync pulse, FSX. The output of the transmit filter is sampled and held on a switched capacitor array. An analog to digital conversion is then performed according to μ-law (C3052, C3053, C3054) or A-law (C3057) coding conventions (see Table 2). Any DC offset due to the filters or comparator is cancelled by an on-chip offset compensation circuit. The offset compensation circuit uses a sign bit integration technique where the sign bit is averaged over a long time to compute the offset which is then subtracted from the input to the encoder. The encoded 8-bit PCM word is clocked out of DX at the beginning of the next encode cycle. The open drain TSX output pulses low during valid DX data.

Receive Channel Operation

μ-law/A-law Decoder — The decoding begins with the receive frame sync pulse, FSR. The 8-bit PCM word is serially latched in at DR on eight consecutive receive bit clocks. A digital to analog conversion is then performed on the PCM data according to the μ-law or A-law format.

Receive Lowpass Filter — The output of the D/A converter is followed by a 5th order lowpass switched capacitor filter clocked at 128 KHz. This filter performs the required lowpass filtering and sin x/x correction necessary to accurately recover the original analog signal. The filter provides passband flatness and stopband rejection which fulfills or exceeds the Bell D3 and D4 specifications and the CCITT G.172 recommendations. The 5th order lowpass filter is followed by an active RC lowpass smoothing filter.

Output Power Amplifier — The receive channel analog output is a low impedance power amplifier capable of driving loads as low as 600 ohms.

Precision Voltage Reference

The CODEC/filter devices are equipped with an on-chip temperature and power supply stable bandgap voltage reference. The bandgap voltage reference supplies individual references to both the transmit and receive channels for extremely accurate gain responses.

Table 2. μ-law/A-law Encoding Format

Input at GSx	μ-law	A-law (1)
V_{in} = + Full Scale (2)	1 0 0 0 0 0 0 0	1 0 1 0 1 0 1 0
V_{in} = + 0 volts	1 1 1 1 1 1 1 1	1 1 0 1 0 1 0 1
V_{in} = – 0 volts	0 1 1 1 1 1 1 1	0 1 0 1 0 1 0 1
V_{in} = – Full Scale	0 0 0 0 0 0 0 0	0 0 1 0 1 0 1 0

1. A-law includes even bit inversion for transmission.
2. Full Scale is 2.5V.

CODEC/filter Timing

Transmit Channel, Short Frame Sync Timing

FSX must be one or two bit clock periods long and must go high while BCLKX is high. On the first rising edge of BCLKX after FSX, DX is enabled and the sign bit is output. The next seven BCLKX rising edges output the remaining seven bits (MSB to LSB). The following BCLKX rising edge disables the DX output. In a signaling frame, FSX is a two bit clock periods long and the signaling bit is transmitted in place of the LSB. The signaling bit at SIGX must be valid at least 100 ns before and 50 ns after the seventh BCLKX falling edge.

Transmit Channel, Long Frame Sync Timing

FSX must be three or more bit clock periods long. When BCLKX is 64 KHz, FSX must be low for a minimum of 160 ns. FSX may go high while BCLKX is high or low. The rising edge of FSX or the rising edge of BCLKX, whichever comes later, enables the DX output and clocks out the sign bit. The next seven BCLKX rising edges clock out the remaining seven bits. The DX output is disabled by the eighth BCLKX falling edge or by FSX going low, whichever comes later. If the signaling frame sync pulse, SFX, is present, the signaling bit is transmitted in place of the LSB. The signaling data bit must be valid at least 100 ns before and 50 ns after the 7th BCLKR falling edge. SFX must be high at least 60 ns before the falling edge of FSX. In addition, it must be high at least 60 ns before and 100 ns after the seventh BCLKX falling edge.

Receive Channel, Short Frame Sync Timing

FSR must be one or two bit clock periods long. FSR must go high while BCLKR (or BCLKX, if BCLKR is not clocked) is high. With FSR high during a falling edge of BCLKR, the next falling edge of BCLKR latches in the sign bit. The following seven BCLKR falling edges latch in the remaining seven bits (MSB to LSB). If FSR is two bit clock periods long, the last bit latched in from DR is stored at SIGR within 300 ns after the eighth BCLKR falling edge.

Receive Channel, Long Frame Sync Timing

FSR must be three or more bit clock periods long. If BCLKR is 64 KHz, FSR must be low for at least 160 ns. FSR may go high while BCLKR is high or low. The first falling edge of BCLKR after the FSR risinge dge latches in the sign bit. The next seven BCLKR falling edges latch in the remaining seven bits. If the signaling frame sync pulse, SFR, is present, the last bit latched in from DR is stored at SIGR within 300 ns after the 8th BCLKR falling edge. SFR must be high at least 60 ns before the FSR falling edge. It must also be high at least 60 ns before and 100 ns after the seventh BCLKR falling edge.

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Timing Specifications

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Master Clocks						MCLKX or MCLKR
Frequency	1/t_{PM}		1.536		MHz	
			1.544		MHz	
			2.048		MHz	
Width of High	t_{WMH}	160			nS	
Width of Low	t_{WML}	160			nS	
Rise Time	t_{RM}			50	nS	
Fall Time	t_{FM}			50	nS	
Bit Clocks						BCLKX or BCLKR
Period	t_{PB}	485	488	15725	nS	
Width of High	t_{WBH}	160			nS	
Width of Low	t_{WBL}	160			nS	
Rise Time	t_{RB}			50	nS	
Fall Time	t_{FB}			50	nS	
Time from MCLKX/R Rising edge to BCLKX/R Rising Edge	t_{MRBR}	0			nS	
Hold Time from Bit Clock High to Frame Sync Rising Edge	t_{HOLD}	0			nS	Short Frame Mode Only
Set-Up Time from Frame Sync High to Bit Clock Falling Edge	t_{SF}	50			nS	Short Frame Mode Only
Hold Time from Bit Clock Low to Frame Sync Falling Edge	t_{HF}	100			nS	Short Frame Mode Only
Hold Time from Bit Clock Low to Frame Sync Rising Edge	t_{HBF}	0			nS	Long Frame Mode Only
Set-Up Time from Frame Sync High to Bit Clock Falling Edge	t_{SFB}	80			nS	Long Frame Mode Only
Hold Time from Bit Clock Low to Frame Sync Falling Edge	t_{HBFI}	100			nS	Long Frame Mode Only, After 3rd Bit Clock Period
Minimum Width of FSX or FSR Low Level	t_{WFL}	160			nS	Long Frame Mode Only, 64 KHz Bit Clocks
Delay Time from 1st BCLKX High to TSX Low	t_{XDP}			140	nS	Load = 150 pF plus 2 LSTTL Loads
Delay Time from FSX or BCLKX Rising Edge, Whichever Comes Later, to DX Data Valid	t_{DZF}	20		165	nS	1st Data Bit Only, CL = 0 pF to 150 pF
Delay Time from BCLKX High to DX Data Valid	t_{DBD}	0		180	nS	Load = 150 pF plus 2 LSTTL Loads
Delay Time from 8th BCLKX Low to DX Data Output Disabled	t_{DZC}	50		165	nS	
Set-Up Time from DR Valid to BCLKR falling Edge	t_{SDB}	50			nS	
Hold Time from BCLKR Low to DR Invalid	t_{HBD}	50			nS	
Set-Up Time from SIGX Valid to 7th BCLKX Falling Edge	t_{SSGB}	100			nS	C3052 and C3053 Only
Hold Time from 7th BCLKX Falling to SIGX Invalid	t_{HBSG}	50			nS	C3052 and C3053 Only
Delay Time from 8th BCLKR Low to SIGR Valid	t_{DFSSG}			300	nS	C3052 and C3053 Only, Load = 50 pF plus 2 LSTTL Loads
Set-Up Time from SFX/R High to FSX/R Falling Edge	t_{SSFF}	60			nS	C3053 Only
Set-Up Time from SFX/R High to 7th BCLKX/R Falling Edge	t_{SSFB}	60			nS	C3053 Only
Hold Time from 7th BCLKX/R Low to SFX/R Falling Edge	t_{HBSF}	100			nS	C3053 Only

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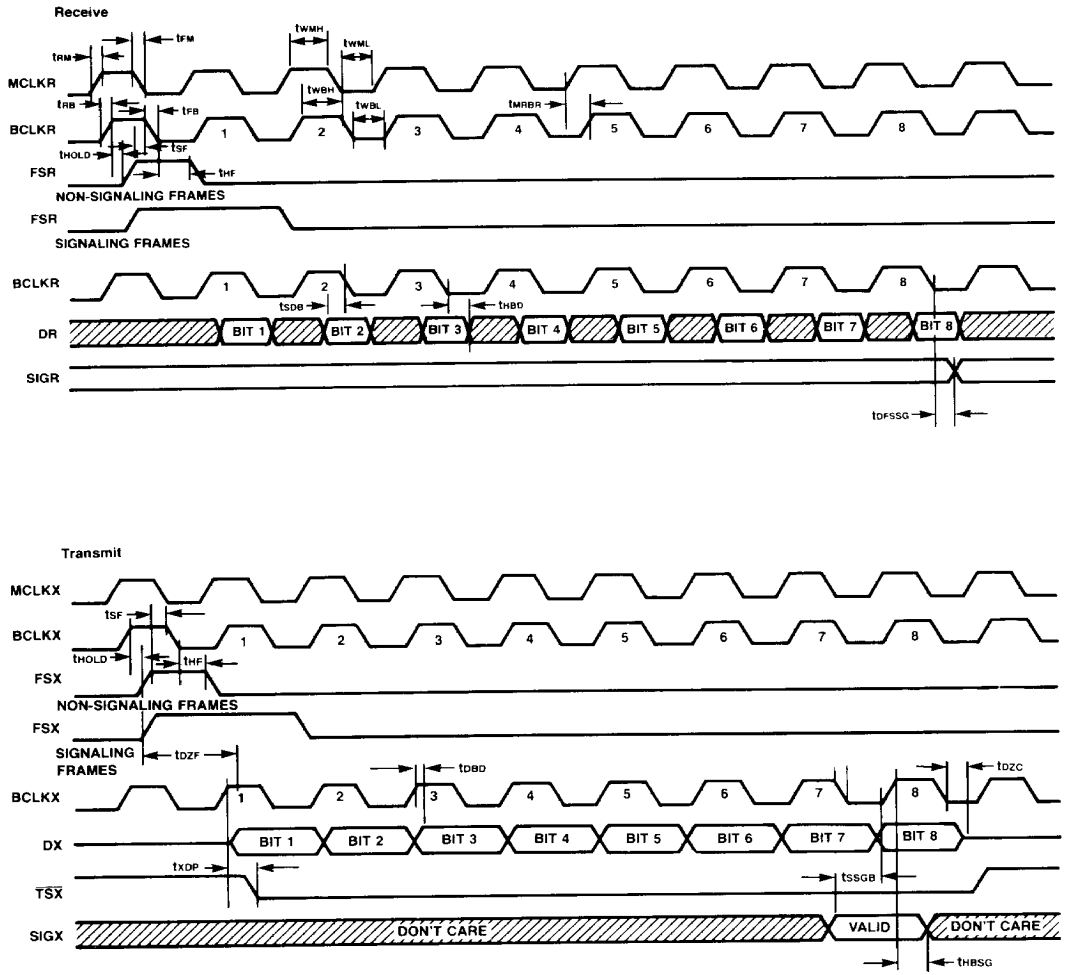

Figure 2. Short Frame Sync Timing

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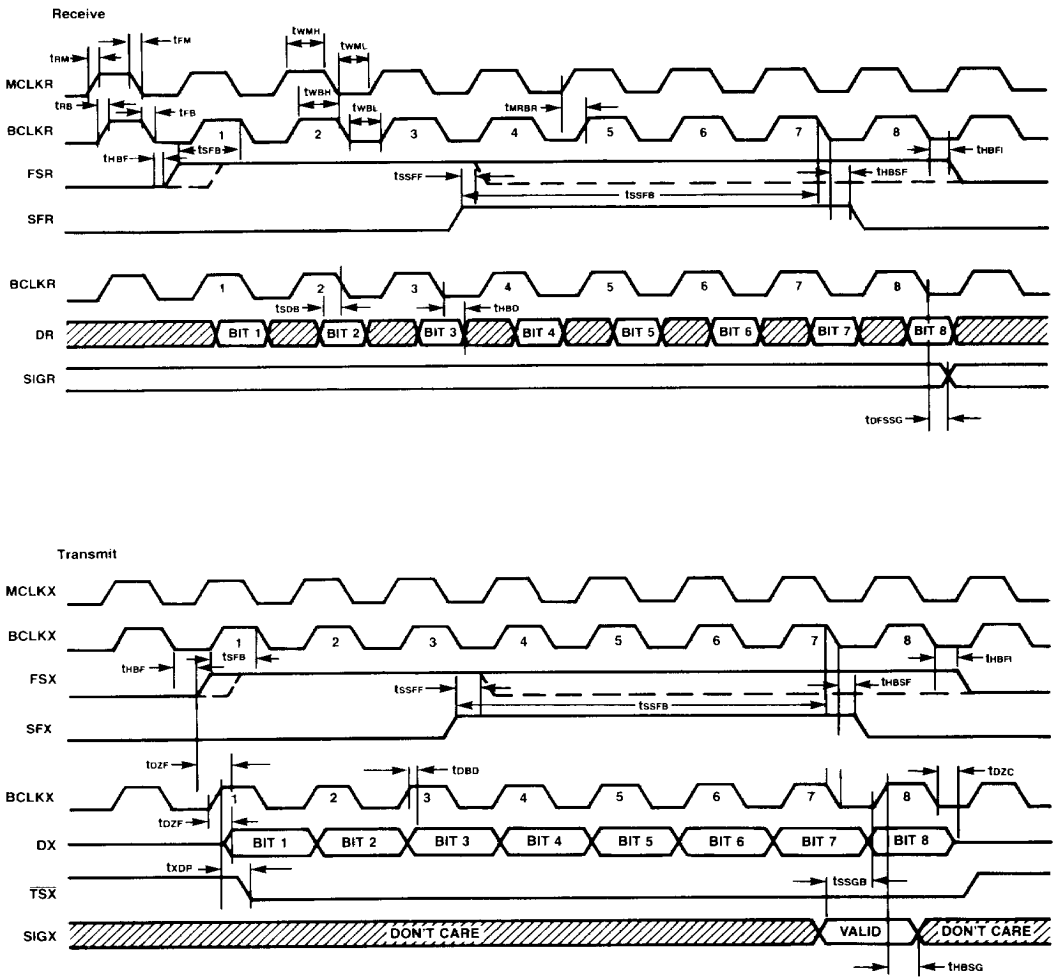

Figure 3. Long Frame Sync Timing

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Absolute Maximum Ratings:

Exceeding these ratings may result in permanent damage. Functional operation under these conditions is not implied.

Parameter	Symbol	Value
V_{DD} with respect to GRND	V_{DDC}	7V
V_{SS} with respect to GRND	V_{SSC}	7V
Voltage at any Analog Input or Output	V_{AMAX}	V_{DD} + 0.3V to V_{SS} − 0.3V
Voltage at any Digital Input or Output	V_{DMAX}	V_{DD} + 0.3V to GRND − 0.3V
Operating Temperature	T_A	− 25°C to + 125°C
Storage Temperature	T_S	− 65°C to + 150°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated values.

DC and Operating Characteristics:

Unless otherwise noted: GRND = 0V, V_{DD} = + 5V, V_{SS} = − 5V, T_A = 0°C to 70°C

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Operating Supply Voltages	V_{DD} V_{SS}	4.75 −5.25	5.0 −5.0	5.25 4.75	V V	Ref. to GRND
V_{DD} Power-down Current	I_{DDO}		0.5	1.5	mA	Device in Power-down Mode
V_{SS} Power-down Current	I_{SSO}		0.05	0.3	mA	Device in Power-down Mode
V_{DD} Operating Current	I_{DD1}		6.0	9.0	mA	Active Operation
V_{SS} Operating Current	I_{SS1}		6.0	9.0	mA	Active Operation
Digital Interface						
Input Low Voltage	V_{IL}			0.6	V	All Digital Inputs
Input High Voltage	V_{IH}	2.2			V	All Digital Inputs
Output Low Voltage SIGR DX TSX	V_{OL}			 0.4 0.4 0.4	 V V V	 I = 1.0 mA I = 3.2 mA I = 3.2 mA, Open Drain
Output High Voltage SIGR DX	V_{OH}	 2.4 2.4			 V V	 I = − 1.0 mA I = 3.2 mA
Input Low Current	I_{IL}	10		10	μA	All Digital Inputs, GRND ≤ V_{IN} ≤ V_{IL}
Input High Current	I_{IH}	− 10		10	μA	All Digital Inputs, V_{IH} ≤ V_{IN} ≤ V_{DD}
High Impedance State Output Current	I_{OZ}	− 10		10	μA	DX output, GRND ≤ V_{OUT} ≤ V_{DD}
Transmit Filter Gain Setting Input Amplifier						
Input Leakage Current, VFxI +, VFxI −	I_{BX}	200		200	nA	2.5V ≤ V_{IN} ≤ 2.5V
Input Resistance, VFxI +, VFxI −	R_{IX}	10			M ohms	−2.5V ≤ V_{IN} ≤ 2.5V
Input Offset Voltage, VFxI +, VFxI −	V_{OSX}	− 20		20	mV	
Common Mode Rejection, VFxI +, VFxI −	CMRRx	60			dB	− 2.5V ≤ V_{IN} ≤ 2.5V
Common Mode Range, VFxI	V_{CMX}	− 2.5		2.5	V	
Power Supply Rejection, GSx	PSRRx	60			dB	
DC Open Loop Voltage Gain, GSx	A_{VOLX}	70			dB	
Open Loop Unity Gain Bandwidth, GSx	fc	1.0			MHz	
Output Voltage Swing, GSx	V_{OX}	± 2.8			V	R_L ≥ 10K ohms
Load Capacitance, GSx	C_{LX}			50	pF	
Minimum Load Resistance, GSx	R_{LX}	10			K ohms	

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DC and Operating Point Characteristics (Continued)

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Receive Filter Output Amplifier						
Output Resistance, VFRO	ROR		1	3	ohms	
Minimum Load Resistance, VFRO	RLR	600			ohms	VFRO = ± 2.5V
Load Capacitance, VFRO	CLR			500	pF	
DC Output Offset Voltage, VFRO	VOSR	−200		200	mV	

Transmit Channel Transmission Characteristics:

Unless otherwise noted: T_A = 0°C to 70°C, V_{DD} = 5V ± 5%, V_{SS} = −5V ± 5%, GRND = 0V, f = 1020 Hz, VFXI+ = 0 dBmO, transmit gain setting input amplifier set for non-inverting unity gain.

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Absolute gain at 1020 Hz	GAX	−0.15		0.15	dB	0 dBmO Input Signal T_A = 25°C, V_{DD} = 5V, V_{SS} = −5V Nominal 0 dBmO level is 4 dBm (600 ohms) = 1.2276 V_{rms}
Frequency Response	GRX					Gain Relative to Gain at
16 Hz				−38	dB	1020 Hz, 0 dBmO Input Signal
50 Hz				−30	dB	
60 Hz				−26	dB	
200 Hz		−1.8		−0.1	dB	
300 Hz to 3000 Hz		−0.15		0.15	dB	
3300 Hz		−0.35		0.05	dB	
3400 Hz		−0.7		0	dB	
4000 Hz				−14	dB	
4600 Hz and Above				−32	dB	
Gain Variation with Temperature at 1020 Hz	GAXT	−0.1		0.1	dB	0 dBmO Input Signal
Gain Variation with Supplies at 1020 Hz	GAXS	−0.05		0.05	dB	0 dBmO Input Signal Supplies = ± 5%
Gain Variation with Level at 1020 Hz	GAXL					Reference Level = −10 dBmO
VFXI+ = −40 dBmO to +3 dBmO		−0.2		0.2	dB	Sinusoidal Test Method
VFXI+ = −50 dBmO to −40 dBmO		−0.4		0.4	dB	
VFXI+ = −55 dBmO to −50 dBmO		−1.2		1.2	dB	
V_{DD} Power Supply Rejection	PPSRX	40			dBC	100 mV_{rms} at f Hz added to V_{DD} f = 0 KHz to 50 KHz V_{DD} = 5.0V, VFXI+ = −30 dBm
V_{SS} Power Supply Rejection	NPSRX	40			dBC	100 mV_{rms} at f Hz added to V_{SS} f = 0 KHz to 50 KHz V_{SS} = −5.0V, VFXI+ = −30 dBm
C Message Idle Channel Noise	NXC		12	15	dBrnCO	C3052, C3053, C3054 VFXI+ = −50 dBm
P Message Idle Channel Noise	NXP		74	−69	dBmOp	C3057 VFXI+ = −50 dBm
Crosstalk, Receive to Transmit	CTRX		90	−70	dB	0 dBmO Receive PCM Level f = 300 Hz to 3400 Hz VFXI+ = −30 dBm
Signal to Total Distortion	STDX					Sinusoidal Test Method
VFXI+ = 3 dBmO		33			dBC	
VFXI+ = 0 dBmO to −30 dBmO		36			dBC	
VFXI+ = −40 dBmO		29			dBC	
VFXI+ = −55 dBmO		14			dBC	
Harmonic Distortion						1020 Hz 0 dBmO Input Signal
	D2HDX			−46	dB	Measure 2nd harmonic
	D3HDX			−46	dB	Measure 3rd harmonic
Absolute Envelope Delay	DAX			315	μS	f = 1600 Hz, dØ/dW
Delay Relative to DAX	DAXR					
f = 500−1000 Hz				220	μS	Deviation of envelope delay
f = 1000−1600 Hz				75	μS	at freq. f, from that at 1600 Hz
f = 1600−2600 Hz				105	μS	
f = 2600−3000 Hz				155	μS	

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Receive Channel Transmission Characteristics:
Unless otherwise noted: T_A = 0°C to 70°C, V_{DD} = 5V ± 5%, V_{SS} = −5V ± 5%, GRND = 0V, PCM code = Ideally encoded 0 dBmO Signal at 1020 Hz.

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Absolute gain at 1020 Hz	G_{AR}	−0.15		0.15	dB	0 dBmO PCM Level T_A = 25°C, V_{DD} = 5V, V_{SS} = −5V Nominal 0 dBmO Level is 4 dBm (600 ohms) = 1.2276 V_{rms}
Frequency Response 0 Hz to 3000 Hz 3300 Hz 3400 Hz 4000 Hz	G_{RR}	 −0.15 −0.35 −0.7		 0.15 0.05 0 −14	 dB dB dB dB	Gain Relative to Gain at 1020 Hz 0 dBmO PCM Level
Gain Variation with Temperature at 1020 Hz	G_{ART}	−0.1		0.1	dB	0 dBmO PCM Level
Gain Variation with Supplies at 1020 Hz	G_{ARS}	−0.05		0.05	dB	0 dBmO PCM Level Supplies = ± 5%
Gain Variation with Level at 1020 Hz PCM Level = −40 dBmO to +3 dBmO PCM Level = −50 dBmO to −40 dBmO PCM Level = −55 dBmO to −50 dBmO	G_{ARL}	 −0.2 0.4 −1.2		 0.2 0.4 1.2	 dB dB dB	Reference Level = Ideally encoded −10 dBmO Signal at 1020 Hz Sinusoidal Test Method
Receive Output Level	V_{RO}	−2.5		2.5	Volts	R_L = 600 ohms
V_{DD} Power Supply Rejection 0 Hz to 4000 Hz 4 KHz to 25 KHz 25 KHz to 50 KHz V_{SS} Power Supply Rejection 0 Hz to 4000 Hz 4 KHz to 25 KHz 25 KHz to 50 KHz	PPSRR NPSRR 	 40 40 36 40 40 36			 dBC dB dB dBC dB dB	100 mV_{rms} at f Hz added to V_{DD} V_{DD} = 5.0V, PCM code = positive zero 100 mV_{rms} at f Hz added to V_{SS} V_{SS} = −5.0V, PCM code = positive zero
C Message Idle Channel Noise P Message Idle Channel Noise	NRC1 NRC2 NRP		8 −82	11 12 −79	dBrnCO dBrnCO dBmOp	C3052, C3053, C3054 −50 dBm activation signal C3052, C3053, C3054 PCM code = alternating positive and negative zero C3057 −50 dBm activation signal
Crosstalk, Transmit to Receive	CTRR		90	−75	dB	0 dBmO Transmit Input Signal f = 300 Hz to 3400 Hz DR = steady PCM code
Signal to Total Distortion PCM Level = 3 dBmO PCM Level = 0 dBmO to −30 dBmO PCM Level = −40 dBmO PCM Level = −55 dBmO	STDR	 33 36 30 15			 dBC dBC dBC dBC	Sinusoidal Test Method
Harmonic Distortion	 D2HDR D3HDR			−46 −46	 dB dB	1020 Hz, 0 dBmO PCM Code Measure 2nd Harmonic Measure 3rd Harmonic
Absolute Envelope Delay Delay Relative to DAR f = 500–1000 Hz f = 1000–1600 Hz f = 1600–2600 Hz f = 2600–3000 Hz	DAR DARR	 −40 −30		200 125 175	μS μS μS μS μS	f = 1600 Hz, DAR = dØ/dW Deviation of Envelope Delay at freq. f to that of 1600 Hz
Spurious Out-of-band Signals at the Channel Output f = 4600 Hz to 7600 Hz f = 7600 Hz to 8400 Hz f = 8400 Hz to 100 KHz	SOS			 −32 −40 −32	 dB dB dB	Loop Around Measurement Apply 0 dBmO, 300 Hz–3400 Hz signal at VFxI+, Measure at V_{FRO}
Intermodulation (Non-linear) Distortion	IMD			−52	dB	Bell System 4 Tone Method per Bell System Technical Ref. #41009

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Applications

The primary applications for the C3052 Family is in telephone systems:

- Switching — Digital PBX's and Central Office Switching Systems
- Transmission — D3/D4 Type Channel Banks and Subscriber Carrier Systems
- Subscriber Instruments — Digital Handsets and Office Workstations

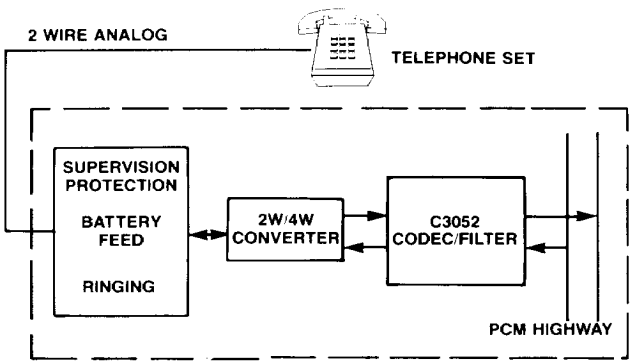

Figure 4. Typical Line Termination for Channel Bank

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