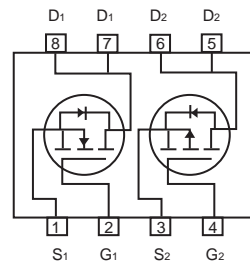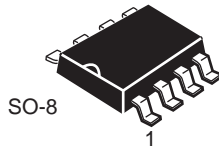# CEM6659

Dual Enhancement Mode Field Effect Transistor (N and P Channel)   PRELIMINARY

5

FEATURES

- 60V, 4.1A, $R_{DS(ON)}$ = 68mΩ @V_{GS} = 10V.

  $R_{DS(ON)}$ = 86mΩ @V_{GS} = 4.5V.

- -60V, -3.1A, $R_{DS(ON)}$ = 130mΩ @V_{GS} = -10V.

  $R_{DS(ON)}$ = 170mΩ @V_{GS} = -4.5V.

- Super high dense cell design for extremely low $R_{DS(ON)}$.

- High power and current handing capability.

- Lead free product is acquired.

- Surface mount Package.

SO-8

1

ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise noted

Parameter	Symbol	N-Channel	P-Channel	Units
Drain-Source Voltage	V_{DS}	60	-60	V
Gate-Source Voltage	V_{GS}	$\pm$20	$\pm$20	V
Drain Current-Continuous	I_D	4.1	-3.1	A
Drain Current-Pulsed [a]	I_{DM}	15	-12	A
Maximum Power Dissipation	P_D	2.0		W
Operating and Store Temperature Range	T_J,T_{stg}	-55 to 150		$^{\circ}$C

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Ambient [b]	$R_{\theta JA}$	62.5	$^{\circ}$C/W

This is preliminary information on a new product in development now .
Details are subject to change without notice .

Rev 1.   2006.May
http://www.cetsemi.com

1

CEM6659

N-Channel Electrical Characteristics $T_A = 25°C$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V$, $I_D = 250\mu A$	60			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60V$, $V_{GS} = 0V$			1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{GS} = 20V$, $V_{DS} = 0V$			100	μA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{GS} = -20V$, $V_{DS} = 0V$			-100	μA
On Characteristics [c]						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$	1		3	V
Static Drain-Source	$R_{DS(on)}$	$V_{GS} = 10V$, $I_D = 4.1A$		56	68	$m\Omega$
On-Resistance		$V_{GS} = 4.5V$, $I_D = 3.5A$		66	86	$m\Omega$
Dynamic Characteristics [d]						
Forward Transconductance	g_{FS}	$V_{DS} = 10V$, $I_D = 4.1A$		5		S
Input Capacitance	C_{iss}	$V_{DS} = 25V$, $V_{GS} = 0V$, f = 1.0 MHz		670		pF
Output Capacitance	C_{oss}			80		pF
Reverse Transfer Capacitance	C_{rss}			45		pF
Switching Characteristics [d]						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30V$, $I_D = 1A$, $V_{GS} = 10V$, $R_{GEN} = 6\Omega$		11	25	ns
Turn-On Rise Time	t_r			3	10	ns
Turn-Off Delay Time	$t_{d(off)}$			30	60	ns
Turn-Off Fall Time	t_f			3	10	ns
Total Gate Charge	Q_g	$V_{DS} = 30V$, $I_D = 4.1A$, $V_{GS} = 10V$		13	17	nC
Gate-Source Charge	Q_{gs}			1.7		nC
Gate-Drain Charge	Q_{gd}			2.6		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current [b]	I_S				4.1	A
Drain-Source Diode Forward Voltage [c]	V_{SD}	$V_{GS} = 0V$, $I_S = 2A$			1.2	V

Notes :
a.Repetitive Rating : Pulse width limited by maximum junction temperature.
b.Surface Mounted on FR4 Board, t ≤ 10 sec.
c.Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
d.Guaranteed by design, not subject to production testing.

P-Channel Electrical Characteristics $T_A = 25\degree C$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V$, $I_D = -250\mu A$	-60			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -60V$, $V_{GS} = 0V$			-1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{GS} = 20V$, $V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{GS} = -20V$, $V_{DS} = 0V$			-100	nA
On Characteristics [b]						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$, $I_D = -250\mu A$	-1		-3	V
Static Drain-Source	$R_{DS(on)}$	$V_{GS} = -10V$, $I_D = -3.1A$		100	130	$m\Omega$
On-Resistance		$V_{GS} = -4.5V$, $I_D = -2.8A$		130	170	$m\Omega$
Dynamic Characteristics [c]						
Forward Transconductance	g_{FS}	$V_{DS} = -10V$, $I_D = -3.1A$		5		S
Input Capacitance	C_{iss}	$V_{DS} = -30V$, $V_{GS} = 0V$, f = 1.0 MHz		885		pF
Output Capacitance	C_{oss}			85		pF
Reverse Transfer Capacitance	C_{rss}			80		pF
Switching Characteristics [c]						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -30V$, $I_D = -1A$, $V_{GS} = -10V$, $R_{GEN} = 6\Omega$		12	25	ns
Turn-On Rise Time	t_r			4	15	ns
Turn-Off Delay Time	$t_{d(off)}$			38	80	ns
Turn-Off Fall Time	t_f			12	25	ns
Total Gate Charge	Q_g	$V_{DS} = -30V$, $I_D = -3.1A$, $V_{GS} = -10V$		11	14	nC
Gate-Source Charge	Q_{gs}			2.4		nC
Gate-Drain Charge	Q_{gd}			1.6		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current	I_S				-3.1	A
Drain-Source Diode Forward Voltage [b]	V_{SD}	$V_{GS} = 0V$, $I_S = -1.3A$			-1.2	V

Notes :
a.Repetitive Rating : Pulse width limited by maximum junction temperature.
b.Pulse Test : Pulse Width $\leq$ 300μs, Duty Cycle $\leq$ 2%.
c.Guaranteed by design, not subject to production testing.
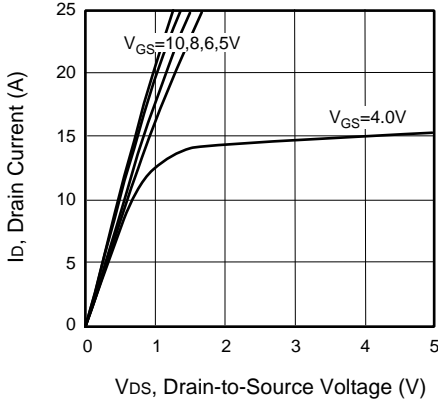
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N-CHANNEL
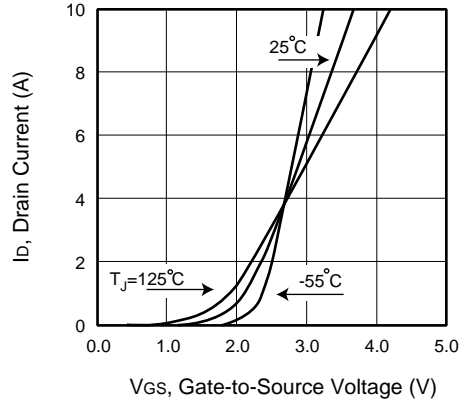

Figure 1. Output Characteristics

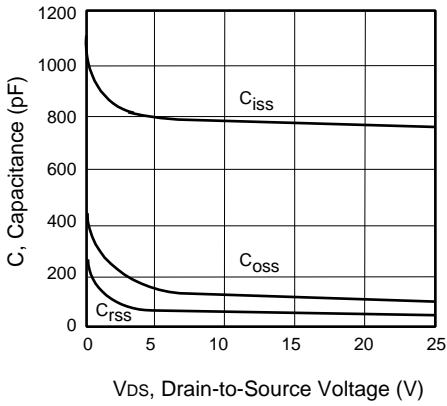**Figure 2. Transfer Characteristics**

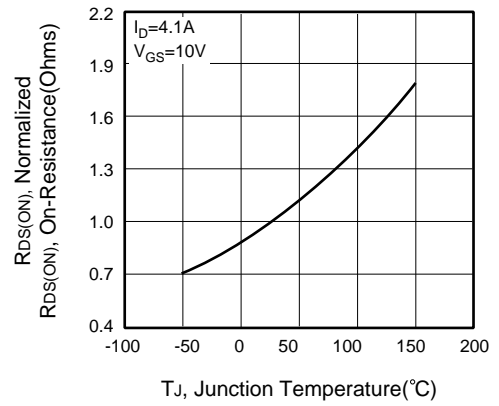**Figure 3. Capacitance**

Figure 4. On-Resistance Variation with Temperature

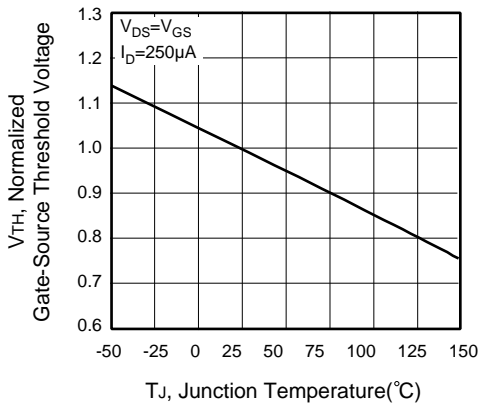**Figure 5. Gate Threshold Variation with Temperature**
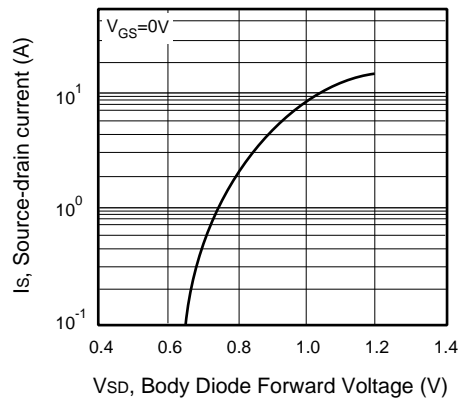

Figure 6. Body Diode Forward Voltage Variation with Source Current

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P-CHANNEL
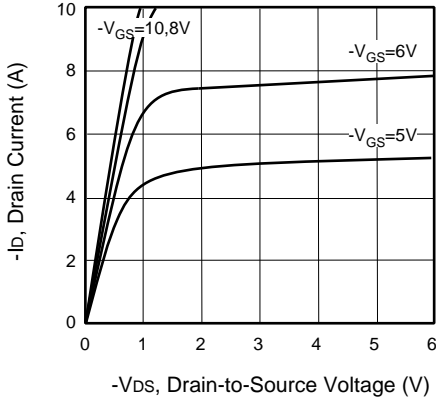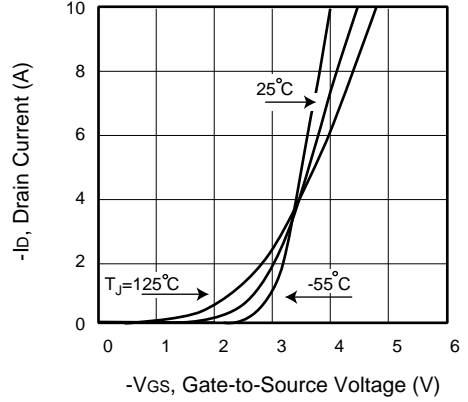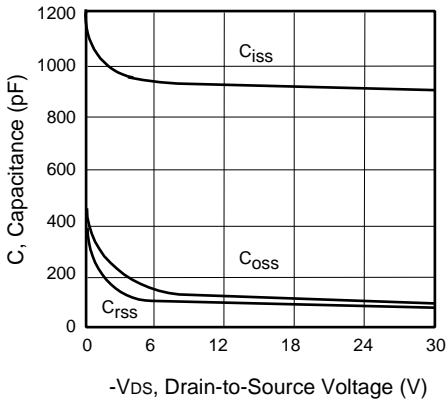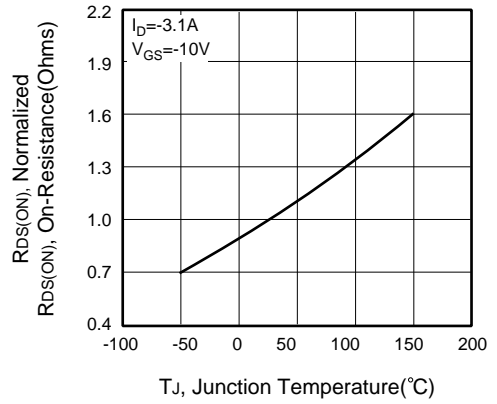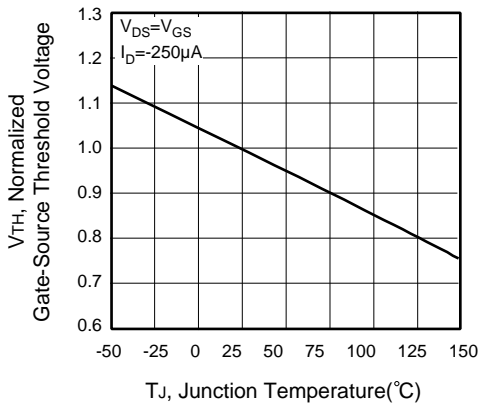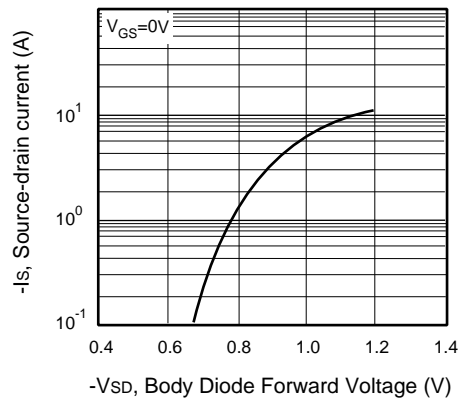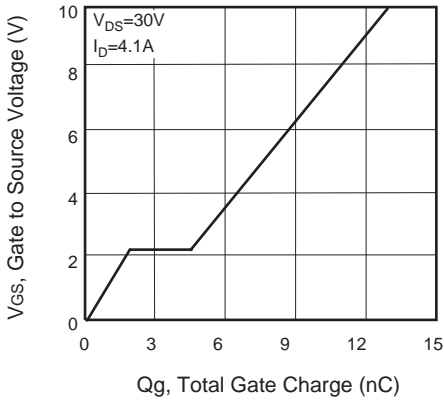

Figure 1. Output Characteristics

Figure 2. Transfer Characteristics

Figure 3. Capacitance

Figure 4. On-Resistance Variation with Temperature

Figure 5. Gate Threshold Variation with Temperature

Figure 6. Body Diode Forward Voltage Variation with Source Current
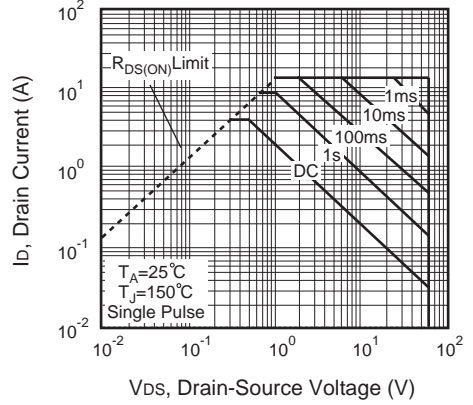
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Figure 13. Gate Charge
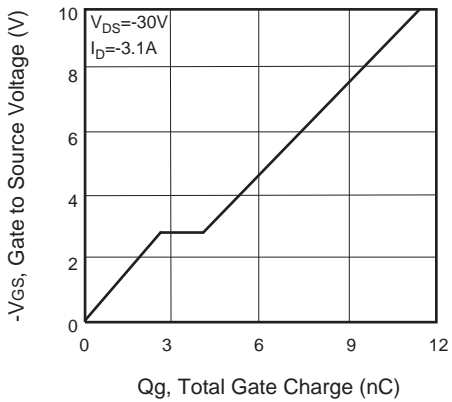

Figure 14. Maximum Safe Operating Area

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Figure 15. Gate Charge

Figure 16. Maximum Safe Operating Area

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Figure 17. Switching Test Circuit

Figure 18. Switching Waveforms

1. $R_{JA}(t) = r(t) * R_{JA}$
2. R_{JA}=See Datasheet
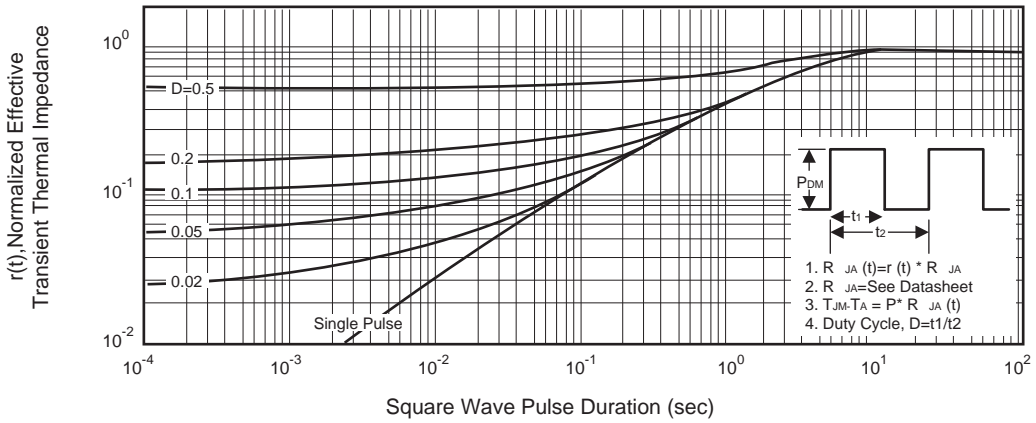3. $T_{JM} - T_A = P * R_{JA}(t)$
4. Duty Cycle, D=t1/t2

Figure 19. Normalized Thermal Transient Impedance Curve