Semiconductor Corporation

CS1232-U

Micromonitor Die

T-65-13

Features

- Halts and restarts an out-of-control microprocessor
- Holds microprocessor in check during power transients
- Automatic restart after power failure
- Monitors pushbutton for external reset
- Monitors microprocessor power supply to be within 5% or 10% of 5 V
- No discrete components needed
- Pin compatible with DS1232

General Description

The CS1232 is a monitor for microprocessors which checks program execution, power source quality, and external reset status.

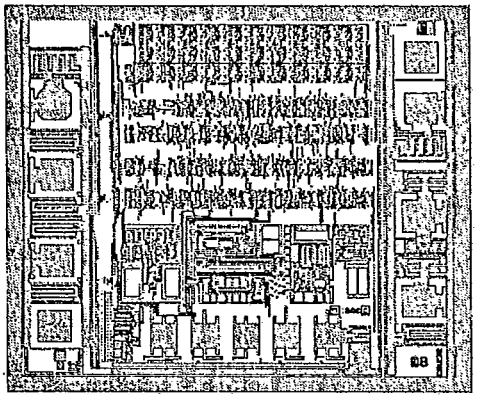
The power status (V_{CC}) is monitored by a comparator and a precision temperature-compensated reference. Reset is forced active by an internal signal when V_{CC} goes out-of-tolerance. Reset signals stay active for a minimum for 250 ms after V_{CC} returns to an in-tolerance condition. This allows both power supply and processor to stabilize.

The pushbutton reset control input is debounced and the active reset minimum pulse width of 250 ms is guaranteed.

The internal watchdog timer forces the reset signals active if the strobe input is not driven low prior to time out. The CS1232 timer can be set to operate at time out settings of approximately 150ms, 600ms, and 1.2 seconds.

ORDERING INFORMATION:

Model	Temp. Range
CS1232-U	0 °C to 70 °C



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Dice Information | The CS1232-U dice are functionally identical to packaged CS1232 devices. For general application information, refer to the packaged product data sheets.

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T-65-13

ANALOG CHARACTERISTICS (T_{MIN} to T_{MAX}, V_{CC} = 4.5 to 5.5V)

Parameter	Symbol	min	typ	max	Units
V_{CC} Trip Point (TOL = GND) (Note 1)	V_{CCTP}	–	4.62	–	V
V_{CC} Trip Point (TOL = V_{CC}) (Note 1)	V_{CCTP}	–	4.37	–	V
Operating Current (Note 2)	I_{CC}	–	0.4	2.0	mA

Notes: 1. All Voltages Referenced To Ground
2. Measured with outputs open

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	min	typ	max	Units
Operating Temperature		0	–	+70	°C
Supply Voltage (Note 1)	V_{CC}	4.5	5.0	5.5	V

DIGITAL CHARACTERISTICS (T_{MIN} to T_{MAX}, V_{CC} = 4.5V to 5.5V)

Parameter	Symbol	min	typ	max	Units
$\overline{ST}$ and $\overline{PBRST}$ Input High Level (Note 1)	V_{IH}	2.0	–	V_{CC} +0.3	V
$\overline{ST}$ and $\overline{PBRST}$ Input Low Level (Note 1)	V_{IL}	−0.3	–	+ 0.8	V
Output High Current @2.4 V RST only	I_{OH}	−1.0	−2.0	–	mA
Output Low Current @0.4 V RST, $\overline{RST}$	I_{OL}	2.0	3.0	–	mA
Input Leakage (Note 3)	I_{IL}	−1.0	–	+ 1.0	uA
Input Capacitance T_A = 25 °C	C_{IN}	–	–	5	pF
Output Capacitance T_A = 25 °C	C_{OUT}	–	–	7	pF

Note: 3. $\overline{PBRST}$ is internally pulled up to Vcc with an internal impedance of 100 kΩ typical.

Specifications are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Parameter	min	typ	max	Units
Voltage on any Pin Relative to Ground	− 1.0	−	+7.0	V
Input Current	−	−	±10	mA
Storage Temperature	− 55	−	+125	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes

SWITCHING CHARACTERISTICS (T_{MIN} to T_{MAX}, V_{CC} = 5V ± 10%)

Parameter	Symbol	min	typ	max	Units
$\overline{PBRST}$ = V_{IL}	t_{PB}	20	−	−	ms
RESET Active Time	t_{RST}	250	610	1000	ms
$\overline{ST}$ Pulse Width	t_{ST}	20	−	−	ns
V_{CC} Detect to RST and $\overline{RST}$	t_{RPD}	−	−	100	ns
V_{CC} Slew Rate from 4.75V - 4.25V	t_F	300	−	−	us
V_{CC} Detect to RST and $\overline{RST}$ (Note 4)	t_{RPU}	250	610	1000	ms
V_{CC} Slew Rate from 4.25V - 4.75V	t_R	0	−	−	ns
$\overline{ST}$ Pulse Period TD pin at Ground TD pin floating TD pin connected to V_{CC} (Note 5)	t_{TD}	 62.5 250 500	 − − −	 250 1000 2000	 ms ms ms

Note: 4. t_R = 5 µs
5. t_{TD} is the maximum elapsed time between $\overline{ST}$ pulses which will keep the watchdog timer from forcing RST and $\overline{RST}$ to the active state for a time of t_{RST}.
6. $\overline{RST}$ is an N-channel open drain output.

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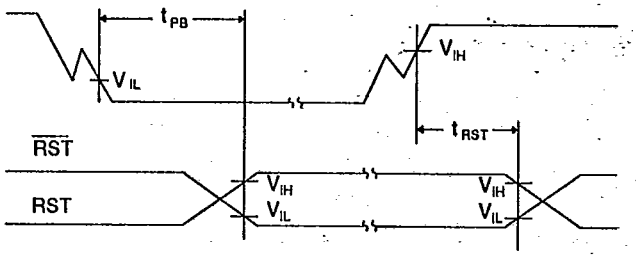
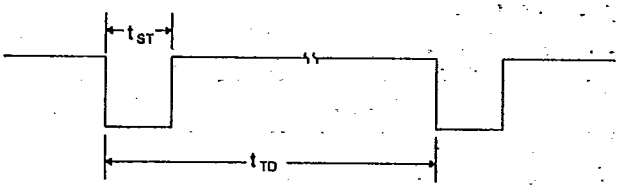
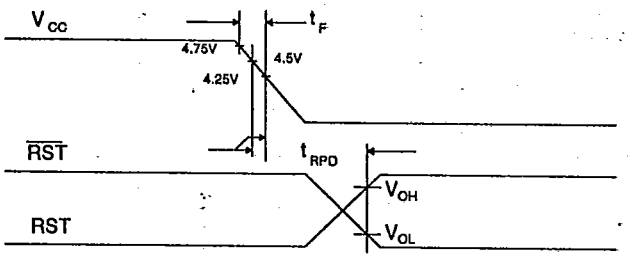


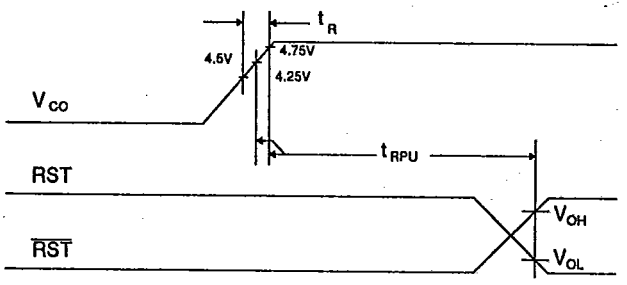
Timing Diagram—Pushbutton Reset



Timing Diagram—Strobe Input



Timing Diagram—Power Down



Timing Diagram—Power Up

GENERAL INFORMATION

Crystal Semiconductor Procedure 42AA00007 outlines the General Requirements for Die Sales. The document includes information on wafer fabrication, manufacturing flow, screening/inspection procedures, packing, shipping, and change notification.

Assembly Information

1. Die size: 0.061" by 0.069" (± 0.002").

2. The CS1232-U is suited for die attach through either eutectic or adhesive means. When eutectic die attach is used, Crystal Semiconductor recommends either a 99.9% Au or 98% Au/2% Si preform of the appropriate size. The backside of the die should be electrically connected to V_{CC}.

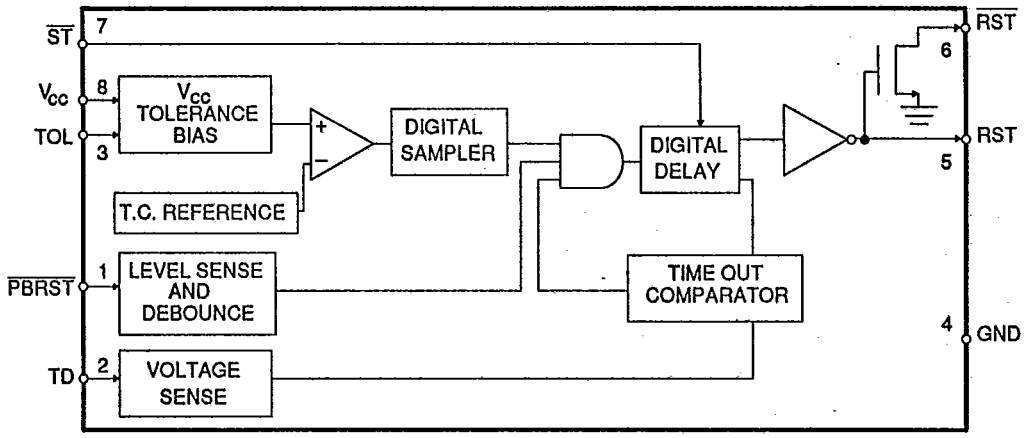
3. Die thickness shall be 0.0175" ± 0.0035". If tighter tolerances are required, contact the factory.

4. The maximum number of die per waffle pack carrier is 100.

5. The cavity dimensions for each die within the waffle pack are 0.080" by 0.080" (Waffle Pack Type H20-080).

5. The CS1232-U requires no particular bonding sequence.

6. The CS1232 product qualification determined that each pin on the device can typically withstand electrostatic discharges up to 3000V and 300 mA dc latch currents. This meets Crystal's minimum criteria of 2500V and 100 mA respectively. Still, Crystal Semiconductor strongly recommends proper handling procedures and in-circuit application.



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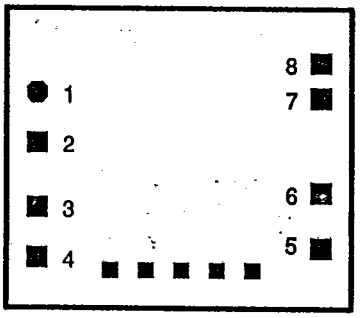
Bonding Diagram for CS1232-U



1 -	$\overline{\text{PBRST}}$	5 -	RST
2 -	TD	6 -	$\overline{\text{RST}}$
3 -	TOL	7 -	$\overline{\text{ST}}$
4 -	GND	8 -	V_{CC}