64K x 32 Static RAM Module

Features

- **High-density 2-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 25 ns**
- **Independent byte and word controls**
- **Low active power**
  - **4.8W (max.)**
- **Hermetic SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of .270 in.**
- **Small PCB footprint**
  - **1.8 sq. in.**

Functional Description

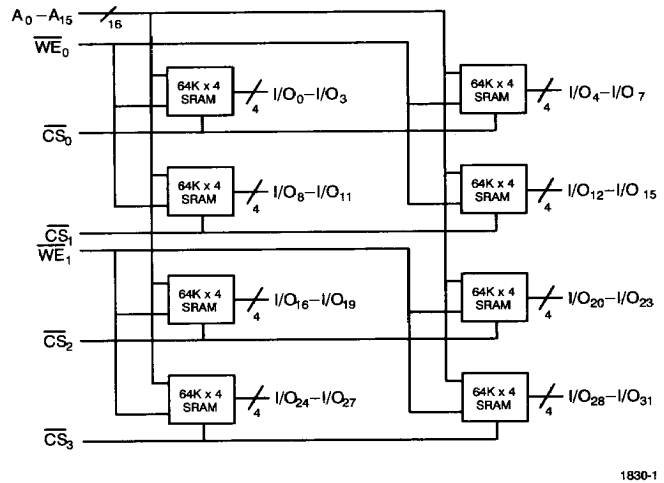
The CYM1830 is a high-performance 2-megabit static RAM module organized as 64K words by 32 bits. This module is constructed from eight 64K x 4 SRAMs in LCC packages mounted on a ceramic substrate with pins. Four chip selects ($\overline{CS}_0$ $\overline{CS}_1$, $\overline{CS}_2$ and $\overline{CS}_3$) are used to independently enable the four bytes. Two write enables ($\overline{WE}_0$ and $\overline{WE}_1$) are used to independently write to either upper or lower 16-bit word of RAM. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects and write enables.

Writing to each byte is accomplished when the appropriate chip select ($\overline{CS}_x$) and write enable ($\overline{WE}_x$) inputs are both LOW. Data on the input/output pins ($\overline{I/O}_x$) is written into the memory location specified on the address pins (A_0 through A_{15}).

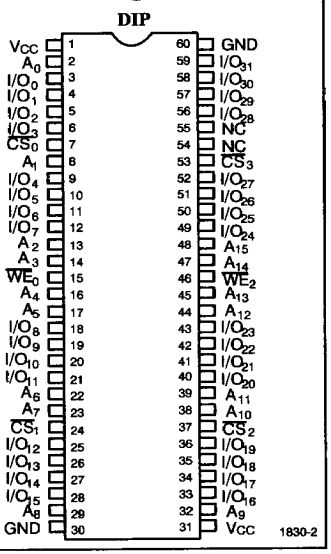
Reading the device is accomplished by taking the chip selects ($\overline{CS}_x$) LOW, while write enables ($\overline{WE}_x$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data input/output pins ($\overline{I/O}_x$).

The Data input/output pins stay in the high-impedance state when write enables ($\overline{WE}_x$) are LOW, or the appropriate chip selects are HIGH.

Logic Block Diagram



Pin Configuration



Selection Guide

		1830-25	1830-30	1830-35	1830-45	1830-55
Maximum Access Time (ns)		25	30	35	45	55
Maximum Operating Current (mA)	Commercial	880	880	880	880	880
	Military			880	880	880
Maximum Standby Current (mA)	Commercial	320	320	320	320	320
	Military			320	320	320

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military [4]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	CYM1830		Units
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−20	+20	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−10	+10	µA
I_{OS}	Output Short Circuit Current [1]	V_{CC} = Max., V_{OUT} = GND		−350	mA
I_{CC}	V_{CC} Operating Supply Current by 16 Mode	V_{CC} = Max., I_{OUT} = 0 mA $\overline{CS}_X \le V_{IL}$		880	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current [2]	Max. V_{CC}, $\overline{CS}_X \ge V_{IH}$ Min. Duty Cycle = 100%		320	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current [2]	Max. V_{CC}, $\overline{CS}_X \ge V_{CC}$ − 0.3V, $V_{IN} \ge V_{CC}$ − 0.3V or $V_{IN} \le 0.3V$		160	mA

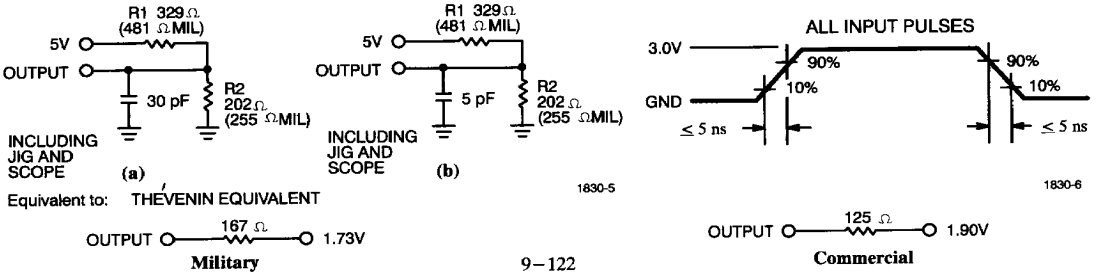
Capacitance [3]

Parameters	Description	Test Conditions	Max.	Units
C_{INA}	Input Capacitance, Address Pins	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	90	pF
C_{INB}	Input Capacitance, I/O Pins		30	pF
C_{OUT}	Output Capacitance		30	pF

Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
3. Tested initially and after any design or process changes that may affect these parameters.
4. T_A is the "instant on" case temperature.

AC Test Loads and Waveforms



Switching Characteristics Over the Operating Range [5]

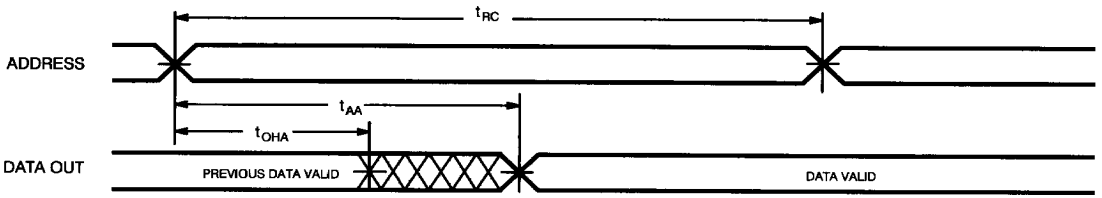
Parameters	Description	1830-25		1830-30		1830-35		1830-45		1830-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	25		30		35		45		55		ns
t_{AA}	Address to Data Valid		25		30		35		45		55	ns
t_{OHA}	Output Hold from Address Change	3		3		3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		25		30		35		45		55	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z [7]	3		3		3		3		3		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z [6, 7]		15		15		20		20		20	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		25		30		35		45		55	ns
WRITE CYCLE [8]												
t_{WC}	Write Cycle Time	25		30		35		45		55		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		25		30		40		40		ns
t_{AW}	Address Set-Up to Write End	20		25		30		40		40		ns
t_{HA}	Address Hold from Write End	2		2		2		2		2		ns
t_{SA}	Address Set-Up to Write Start	2		2		2		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		25		30		40		ns
t_{SD}	Data Set-Up to Write End	15		20		20		25		25		ns
t_{HD}	Data Hold from Write End	2		2		2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [7]	1		3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [6, 7]	0	15	0	20	0	20	0	20	0	20	ns

Notes:

5. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
6. t_{HZCS} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
7. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device.
8. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. $\overline{WE}$ is HIGH for read cycle.
10. Device is continuously selected, $\overline{CS}$ = V_{IL}.
11. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
12. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms [10]

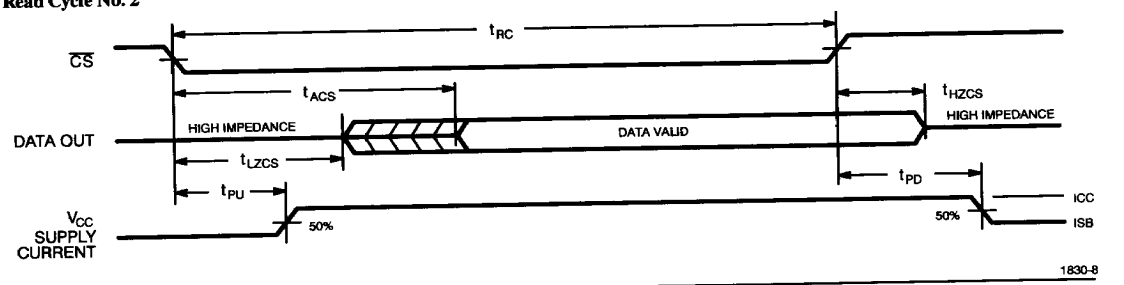
Read Cycle No. 1 [9, 10]



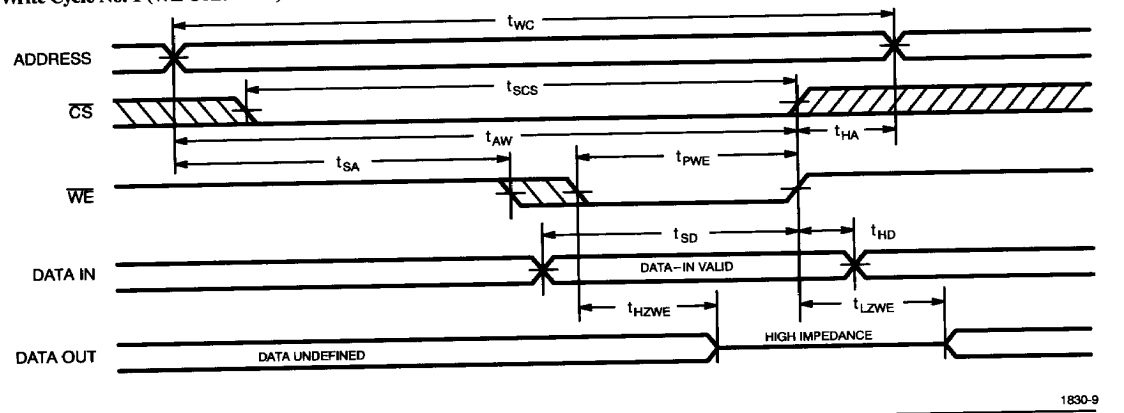
1830-7

Switching Waveforms (continued)

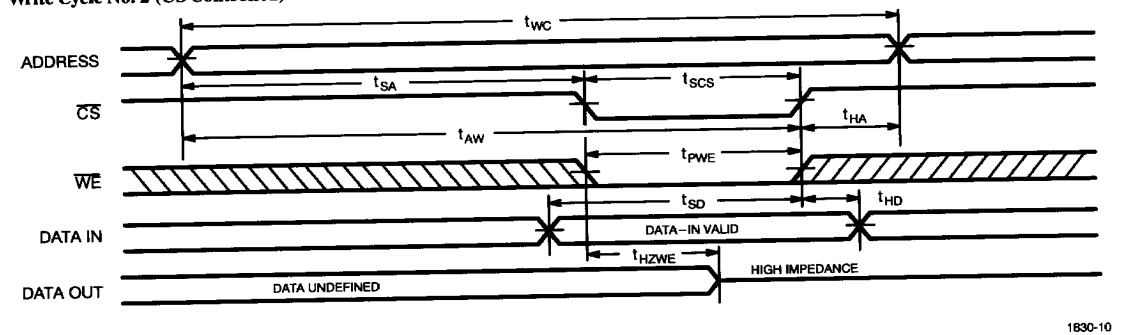
Read Cycle No. 2 [9, 10]



Write Cycle No. 1 ($\overline{WE}$ Controlled) [8]



Write Cycle No. 2 ($\overline{CS}$ Controlled) [8, 12]



Truth Table

$\overline{CS}_x$	$\overline{WE}_x$	Input/Outputs	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

Ordering Information

Speed	Ordering Code	Package Type	Operating Range
25	CYM1830HD-25C	HD06	Commercial
30	CYM1830HD-30C	HD06	Commercial
35	CYM1830HD-35C	HD06	Commercial
	CYM1830HD-35MB	HD06	Military
45	CYM1830HD-45C	HD06	Commercial
	CYM1830HD-45MB	HD06	Military
55	CYM1830HD-55C	HD06	Commercial
	CYM1830HD-55MB	HD06	Military

Document #: 38–M–00017–A