EISA 9000

EISA Bus Master Interface Chip for High Performance Controllers

Preliminary December1990

Features

- Efficient EISA Bust Master Interface for high perfomance adapter cards
- Supports EISA Burst Mode Data rates to 33 MBytes/sec
- BIOS PROM and ID PROM support
- Clock to 25 MHz
- Direct connect to System Bus of all Host Interface Control Signals
- Low power CMOS in 128 Pin Plastic QFP Package

General Description

The EISA 9000 is designed to provide the most compact, inexpensive and highest performance EISA bus master interface for adapter boards that use controller chips with internally or externally generated DMA address and data functions. The EISA 9000 provides a complete Bus Master Interface for proprietary controllers, Intel 80386SX/DX, 80486, 80960 and other Intel bus mode compatible processors.

Use of the PLX Technology 9000 series of bus master chips minimizes hardware and software development costs and time because one basic adapter hardware and software driver design can be used for EISA, AT or Micro Channel applications.

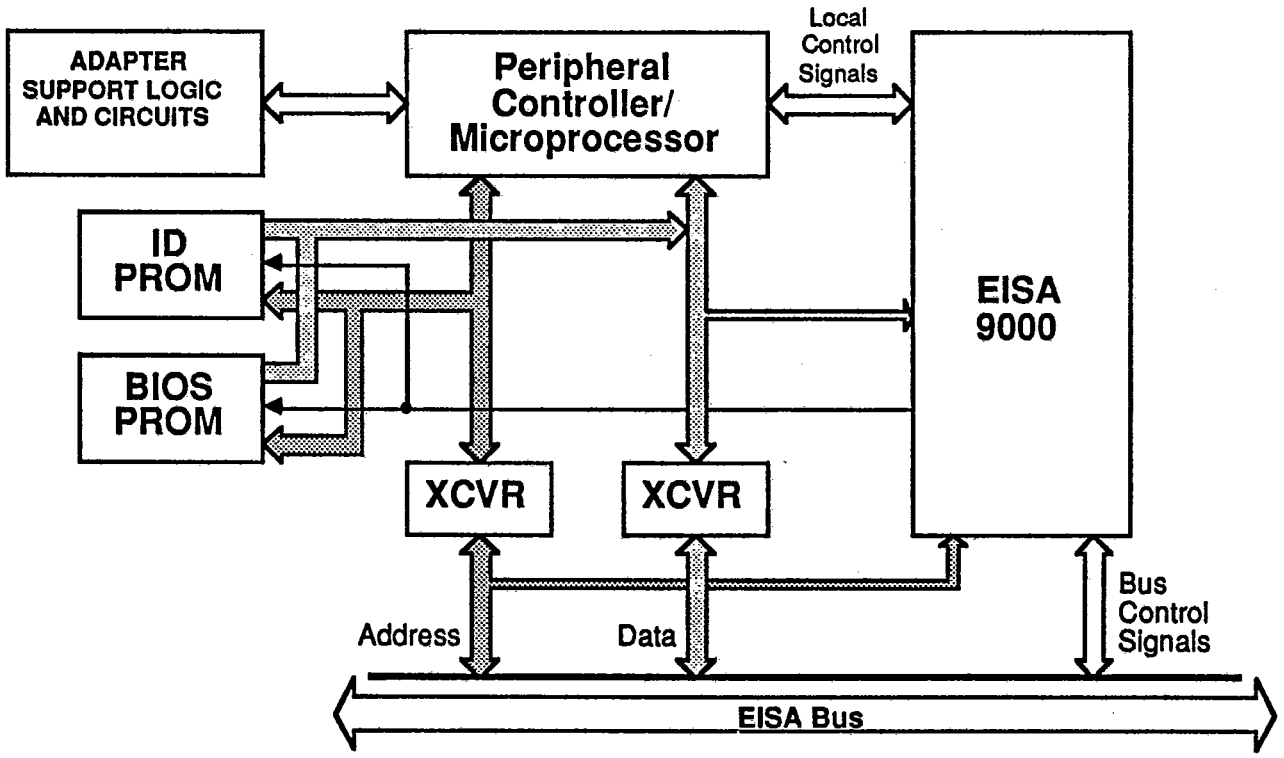

FIGURE 1. Typical Adapter Block Diagram

EISA 9000 GENERAL DESCRIPTION

The EISA 9000 is designed to provide the most compact, inexpensive and highest performance EISA bus interface for boards which use controller chips that generate DMA address and data functions internally or externally.

EISA bus master adapters which use the EISA 9000 offer substantial performance advantages over slave adapters. For example, a bus master can achieve up to eight times the system bus transfer rate of a typical sixteen bit AT slave implementation and at a competitive cost. Performance is also enhanced by the more efficient protocol processing of the intelligent controller. The bus master implementation frees the host processor from managing bus data transfer operations, which improves overall system performance.

Using the PLX Technology 9000 series of bus master chips also reduces total hardware and software development costs for adapter manufacturers designing EISA, Micro Channel and AT compatible boards. In addition to the EISA 9000 interface chip, PLX technology provides the MC 9000 and AT 9000, which are Micro Channel and AT bus master chips respectively, that have local interfaces identical to the EISA 9000. Therefore, by using the 9000 series, similar hardware designs and software drivers can be used for all three buses.

EISA 9000 FUNCTIONS

The EISA 9000 is a 128 pin plastic QFP CMOS bus master interface chip. The local handshake signals are compatible with 386 and 486 control signals but they may be used with non-Intel mode adapter functions also. Two mode pins select 386SX or DX compatible (2X clock) or 486 compatible (1X clock) operation.

Data Transfer Modes

The EISA 9000 supports both 16 and 32 bit Burst Data Transfers, depending on the data width and bursting capability of the controller. In addition, the EISA 9000 supports slave mode for initialization of registers and access to other adapter board slave devices such as BIOS ROM, ID PROM or other memory and I/O devices.

Configuration Registers

The EISA 9000 contains five internal configuration registers. The configuration registers contain configuration data which is loaded from the host during I/O setup. Included in these registers are the interrupt request level, PREEMPT timer configuration, data size, I/O address decode bits, and memory address decode bits. The EISA 9000 also provides four external user bits for application specific configuration information.

Specific EISA 9000 functions

1. **Master Control Signal Protocol Converter.** The chip converts all handshakes of the local controller to EISA handshakes.
2. **Slave controller.** The EISA 9000 includes an EISA slave interface for control of adapter

board slave devices.

3. **Address decoder.** The EISA 9000 decodes host address bits A16-A13, A11-A0 and contains an enable pin for an external A31-A17 or A24-A17 address decoder. The EISA 9000 decodes these addresses to generate chip selects.
4. **Interrupt generator.** The EISA 9000 can generate one of four host interrupts from one local interrupt, programmable through configuration registers.
5. **External Buffer Controller.** The EISA 9000 generates all buffer enable and direction signals for external address and data transceivers.
6. **Clock.** The EISA 9000 runs from an inexpensive crystal and can generate a clock up to 40 MHz for external and internal use.
7. **User programmable configuration bits.** The EISA 9000 provides up to four external bits which can be configured through the configuration registers.
8. **Bus drivers.** All signals generated by the EISA 9000 drive the EISA bus directly, without requiring external drivers.
9. **Maximum bus hold time controller.** Through the configuration registers the user may program a maximum time which the adapter may hold the bus.
10. **Adapter ID mapping.** The adapter ID number is mapped into I/O space to allow the option to implement the adapter ID in an ID PROM.
11. **BURST Transfer Address Controller.** During EISA BURST transfers, the EISA 9020 generates A(2-9) to ensure proper timing between data and address signals.

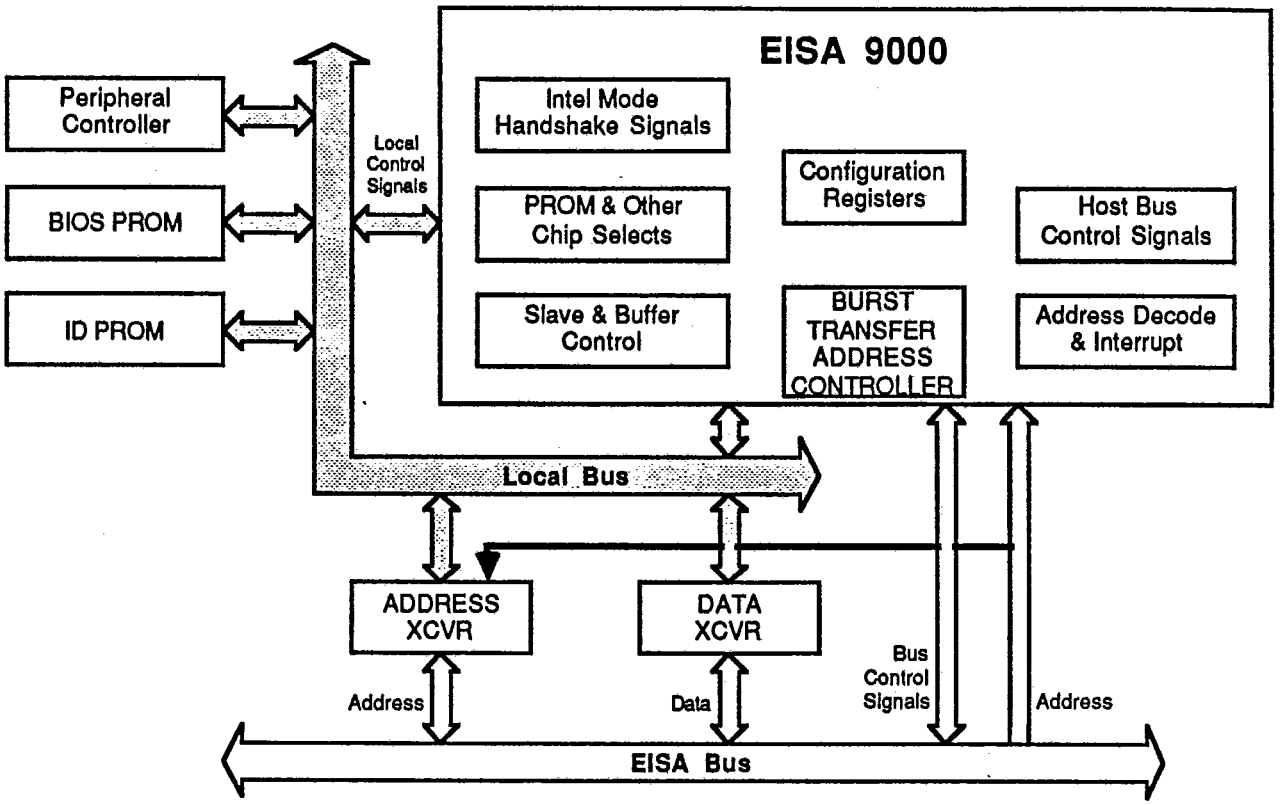

FIGURE 2. EISA 9000 Functional Block Diagram

Package Mechanical Dimensions