EISA 9020

EISA Bus Master Interface Chip for Intel 82596 LAN Controller

Preliminary DECEMBER 1990

Features

EISA Bus Master Interface for Intel 82596 CA/SX/DX Ethernet Controllers

- Supports EISA Burst Mode Data rates to 33 MB/sec
- BIOS PROM and Node ID PROM support
- Clock to 25 MHz
- Direct connect to System Bus of all Host Interface Control Signals
- Low power CMOS in 128 Pin Plastic QFP Package

General Description

The EISA 9020 is designed to provide the most compact, inexpensive and highest performance EISA bus master interface for adapter boards that use the Intel 82596 Ethernet controller.

Use of the PLX Technology 9000 series of bus master chips minimizes hardware and software development costs and time because one basic adapter hardware and driver design can be used for EISA, AT or Micro Channel applications.

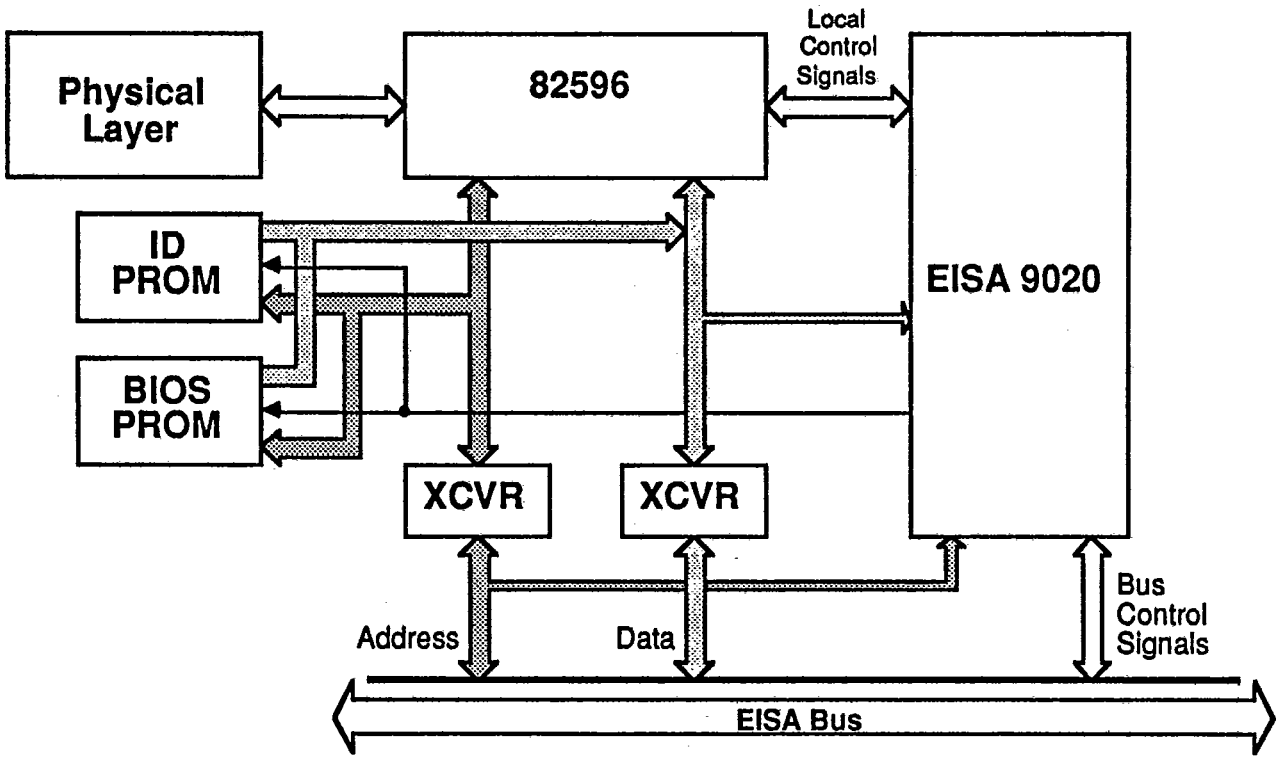

FIGURE 1. Typical Adapter Block Diagram

EISA 9020 GENERAL DESCRIPTION

The EISA 9020 is designed to provide the most compact, inexpensive and highest performance EISA bus interface for boards which use the Intel 82596SX, DX and CA.

EISA bus master adapters which use intelligent LAN controllers and the EISA 9020 offer substantial performance advantages over slave adapters. For example, a bus master can achieve up to eight times the system bus transfer rate of a typical sixteen bit AT slave implementation and at a competitive cost. LAN performance is also enhanced by the more efficient protocol processing of the 82596. The bus master implementation frees the host processor from managing bus data transfer operations, which improves overall system performance.

Using the PLX Technology 9000 series of bus master chips also reduces total hardware and software development costs for LAN adapter manufacturers designing EISA, Micro Channel and AT compatible boards. In addition to the EISA 9020 interface chip, PLX Technology provides the MC 9020 and AT 9020, which are Micro Channel and AT bus master chips that have local interfaces identical to the EISA 9020. Therefore, by using the 9000 series, similar hardware designs and software drivers can be used for all three buses; EISA, AT and Micro Channel.

EISA 9020 FUNCTIONS

The EISA 9020 is a 128 pin plastic QFP CMOS bus master interface chip. Two mode pins select SX, DX or CA operation.

Data Transfer Modes

The EISA 9020 supports both 16 and 32 bit Burst Data Transfers, depending on the data width and bursting capability of the controller. In addition, the EISA 9020 supports slave mode for initialization of registers and access to other adapter board slave devices such as BIOS ROM, Node ID PROM or other memory and I/O devices.

Configuration Registers

The EISA 9020 contains five internal configuration registers. The configuration registers contain configuration data which is loaded from the host during I/O setup. Included in these registers are the interrupt request level, PREEMPT timer configuration, data size, I/O address decode bits, and PROM address decode bits. The EISA 9020 also provides four external user bits for application specific configuration information.

The card ID information is supplied external to the EISA 9020 and is contained in the Node ID PROM.

Specific EISA 9020 functions

EISA 9020 major functions include:

1. **Master Control Signal Protocol Converter.** The chip converts all handshakes of the local controller to EISA handshakes.

2. **Slave controller.** The EISA 9020 includes an EISA slave interface for control of adapter board slave devices.
3. **Address decoder.** The EISA 9020 decodes host address bits A16-A13, A11-A2 and contains an enable pin for an external A31-A17 or A24-A17 address decoder. The EISA 9020 decodes these addresses to generate chip selects.
4. **Interrupt generator.** The EISA 9020 can generate one of four host interrupts from one local interrupt, programmable through configuration registers.
5. **External Buffer Controller.** The EISA 9020 generates all buffer enable and direction signals for external address and data transceivers.
6. **Clock.** The EISA 9020 runs from an inexpensive crystal and generates a clock at 25 MHz for external and internal use.
7. **User programmable configuration bits.** The EISA 9020 provides up to four external bits which can be configured through the configuration registers.
8. **Bus drivers.** All signals generated by the EISA 9020 drive the EISA bus directly, without requiring external drivers.
9. **Maximum bus hold time controller.** Through the configuration registers the user may program a maximum time which the adapter may hold the bus.
10. **BURST Transfer Address Controller.** During EISA BURST transfers, the EISA 9020 generates A(2-9) to ensure proper timing between data and address signals.
11. **Adapter ID mapping.** The adapter ID number is mapped into I/O space to allow the option to implement the adapter ID in an ID PROM.

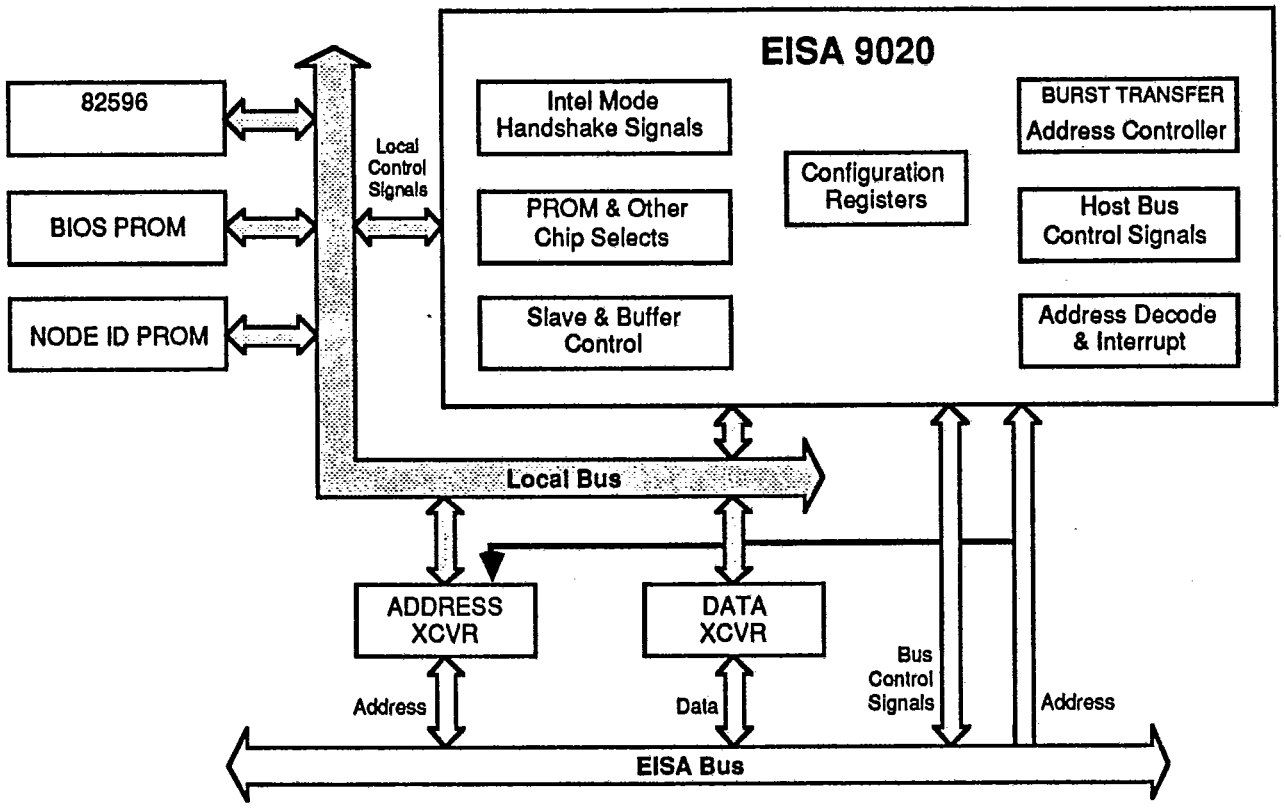

FIGURE 2. EISA 9020 Functional Block Diagram

Package Mechanical Dimensions