MC100LVEL14

3.3V ECL 1:5 Clock Distribution Chip

The MC100LVEL14 is a low skew 1:5 clock distribution chip designed explicitly for low skew clock distribution applications. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. The LVEL14 is functionally and pin compatible with the EL14 but is designed to operate in ECL or PECL mode for a voltage supply range of –3.0 V to –3.8 V (or 3.0 V to 3.8 V).

The LVEL14 features a multiplexed clock input to allow for the distribution of a lower speed scan or test clock along with the high speed system clock. When LOW (or left open and pulled LOW by the input pulldown resistor) the SEL pin will select the differential clock input.

The common enable ($\overline{EN}$) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of the input clock, therefore all associated specification limits are referenced to the negative edge of the clock input.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

- 50 ps Output-to-Output Skew
- Synchronous Enable/Disable
- Multiplexed Clock Input
- ESD Protection: >2 KV HBM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC}= 3.0 V to 3.8 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE} = –3.0 V to –3.8 V
- Internal Input Pulldown Resistors on CLK
- Q Output will Default LOW with Inputs Open or at V_{EE}
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 303 devices

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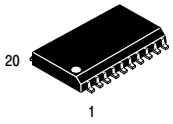
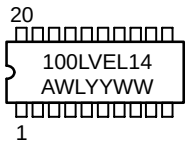


SOIC–20
DW SUFFIX
CASE 751D

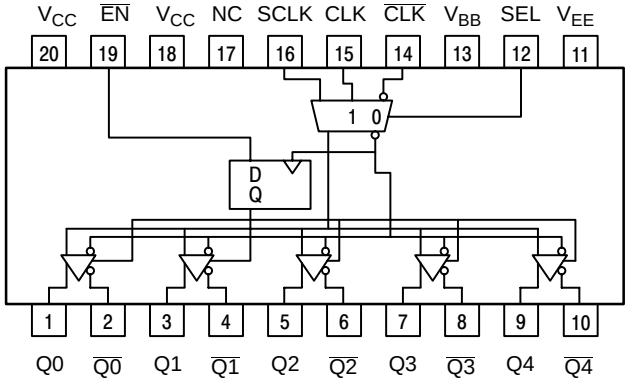
MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEL14DW	SOIC–20	38 Units/Rail
MC100LVEL14DWR2	SOIC–20	1000 Units/Reel



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. Pinout (Top View) **and Logic Diagram**

PIN DESCRIPTION

PIN	FUNCTION
CLK, $\overline{CLK}$	ECL Diff Clock Inputs
SCLK	ECL Scan Clock Input
$\overline{EN}$	ECL Sync Enable
SEL	ECL Clock Select Input
$Q_{0–4}$, $\overline{Q_{0–4}}$	ECL Diff Clock Outputs
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

FUNCTION TABLE

CLK	SCLK	SEL	$\overline{EN}$	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
X	X	X	H	L*

*On next negative transition of CLK or SCLK
X = Don't Care

MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8 to 0	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 –6 to 0	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	90 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	20 SOIC	30 to 35	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

LVPECL DC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V (Note 2)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		32	40		32	40		34	42	mA
V_{OH}	Output HIGH Voltage (Note 3)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 3)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage (Single Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single Ended)	1490		1825	1490		1825	1490		1825	mV
V_{BB}	Output Voltage Reference	1.87		2	1.95		2.05	1.99		2.11	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 7)										
	Vpp < 500 mV	1.3		2.9	1.2		2.9	1.2		2.9	V
	Vpp ≧ 500 mV	1.5		2.9	1.4		2.9	1.4		2.9	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current Others	0.5			0.5			0.5			μA
	$\overline{CLK}$	–300			–300			–300			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

2. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
3. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
4. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

LVNECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 5)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		32	40		32	40		34	42	mA
V_{OH}	Output HIGH Voltage (Note 6)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 6)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{BB}	Output Voltage Reference	–1.43		–1.30	–1.35		–1.25	–1.31		–1.19	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 7)										
	Vpp < 500 mV	–2.0		–0.4	–2.1		–0.4	–2.1		–0.4	V
	Vpp ≧ 500 mV	–1.8		–0.4	–1.9		–0.4	–1.9		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current Others	0.5			0.5			0.5			μA
	$\overline{CLK}$	–300			–300			–300			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

5. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
6. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
7. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

AC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 8)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Toggle Frequency (SeeFigure 2.)		> 1			> 1			> 1		GHz
t_{PLH} t_{PHL}	Prop CLK to Q (Diff) Delay CLK to Q (SE) SCLK to Q	520 470 470		720 770 770	580 530 530	680 680 680	780 830 830	630 580 580		830 880 880	ps
t_{SKEW}	Part-to-Part Skew Within-Device Skew (Note 9)			200 50			200 50			200 50	ps
t_{JITTER}	Cycle–to–Cycle Jitter (SeeFigure 2.)		0.2	< 1		0.2	< 1		0.2	< 1	ps
t_S	Setup Time $\overline{EN}$	0			0			0			ps
t_H	Hold Time $\overline{EN}$	0			0			0			ps
V_{PP}	Input Swing CLK (Note 10)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	230		500	230		500	230		500	ps

8. V_{EE} can vary ±0.3 V.
9. Skews are specified for identical LOW-to-HIGH or HIGH-to-LOW transitions.
10. $V_{PP(}$min) is minimum input swing for which AC parameters guaranteed.

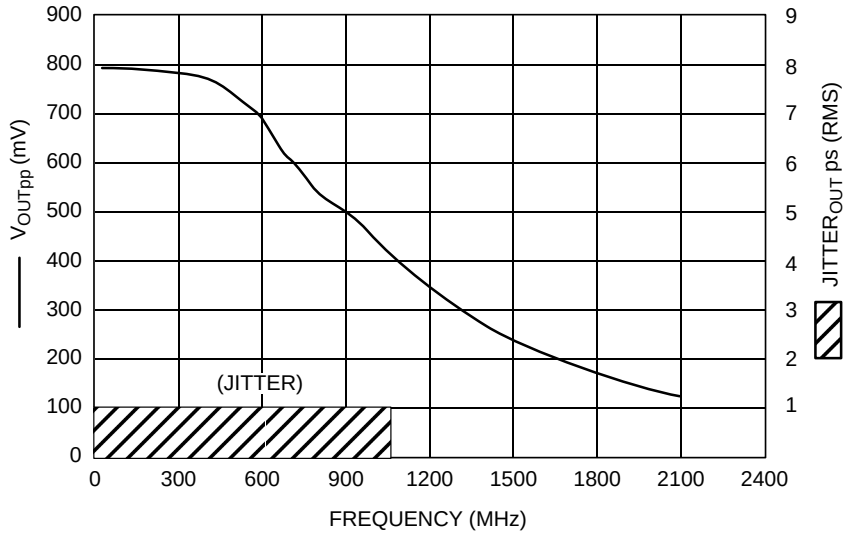


Figure 2. F_{max}/Jitter

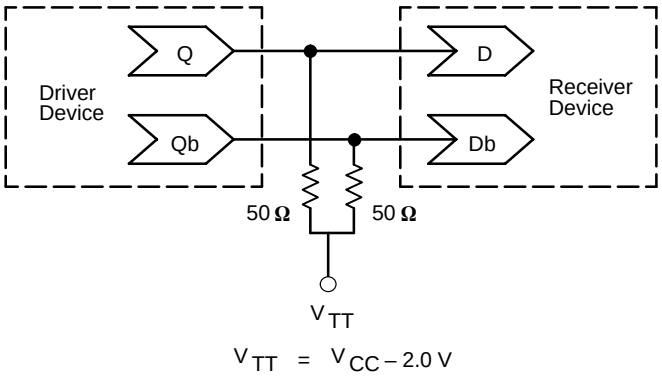


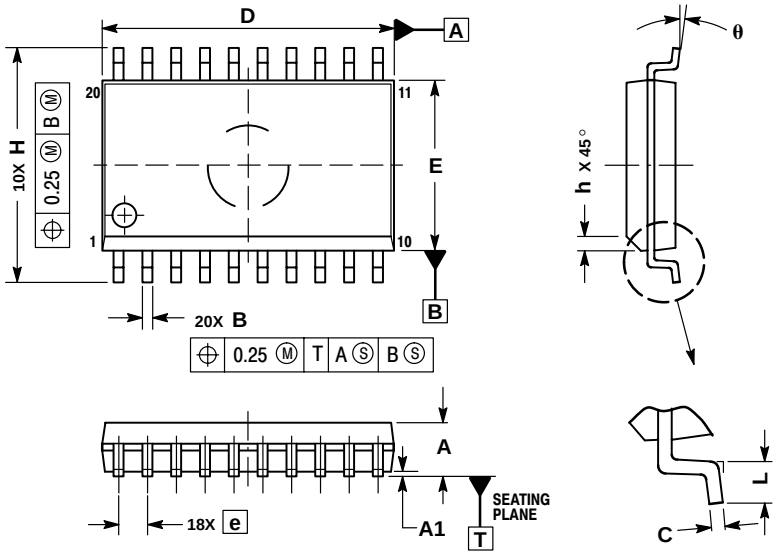
Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

PACKAGE DIMENSIONS

SOIC–20
DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D–05
ISSUE F



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

Notes

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