Data Sheet, V 1.0, Oct. 2003

TC1912

32-Bit Single-Chip Microcontroller

Microcontrollers

Infineon technologies

Never stop thinking.

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TC1912
PRELIMINARY
Revision History: 2003-10 V 1.0

Previous Version:

Page	**Subjects (major changes since last revision)**

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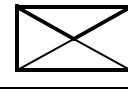

PRELIMINARY

TC1912 Features

The TC1912 offers a 32 bit TriCore based microcontroller/DSP, which is mainly designed for automotive telematics applications. Due to its high integration, this microcontroller/DSP offers high system performance at minimized cost. Typical telematics functions processed by RISC-, DSP- and speech- (CODEC) modules are now combined in one component. This combination of the CODEC and standard peripherals (SSC/SPI, ASC and IIC), makes this engine tailored for a wide variety of telematics applications: navigation, emergency call, speech interface or communication interface.

- TriCore CPU/DSP with 4-Stage Pipeline:
  - 66 MHz max. CPU clock frequency, 50 MHz max. FPI Bus clock frequency.
  - 32-bit super-scalar TriCore main CPU
  - 4-GByte unified memory space support
  - Fast context-switching
  - Dual 16 x 16 Multiply-accumulate (MAC) unit
  - 64-bit Local Memory Bus (LMB)
  - 32-bit Flexible Peripheral Interface Bus (FPI)
  - 32-bit wide External Bus Unit (EBU)
- On-chip memories:
  - 24 KByte Code Scratch-Pad RAM (CSRAM)
  - 8 KByte Instruction Cache (ICACHE)
  - 24 KByte Data Scratch-Pad RAM (DSRAM)
  - 8 KByte Data Cache (DCACHE)
  - 64 KByte fast LMB SRAM
  - 16 KByte FPI SRAM (of which 8 KByte Stand-By SRAM)
- Product Specific Peripherals:
  - 14-bit double CODEC with flexible sample rates and FIFO support
  - 8 External Interrupt Inputs
- Automotive Peripherals:
  - Two independent CAN-nodes (TwinCAN) with gateway support
- Standard Peripherals:
  - 3 x asynchronous serial interface (ASC) with IrDa-support
  - 1 SPI-compatible synchronous serial interface
  - IIC module
  - 3 x 32 bit timer
  - Real time clock (RTC)
  - Watchdog timer (WDT)
- Clock Generation Unit with PLL
- Debug Support: OCDS Level 1 with JTAG interface
- Dual voltage supply (1.8V core, 3.3V I/O)
- Power saving features
- -40°C to +85°C temperature range
- LBGA-208 package

PRELIMINARY

Block Diagram.

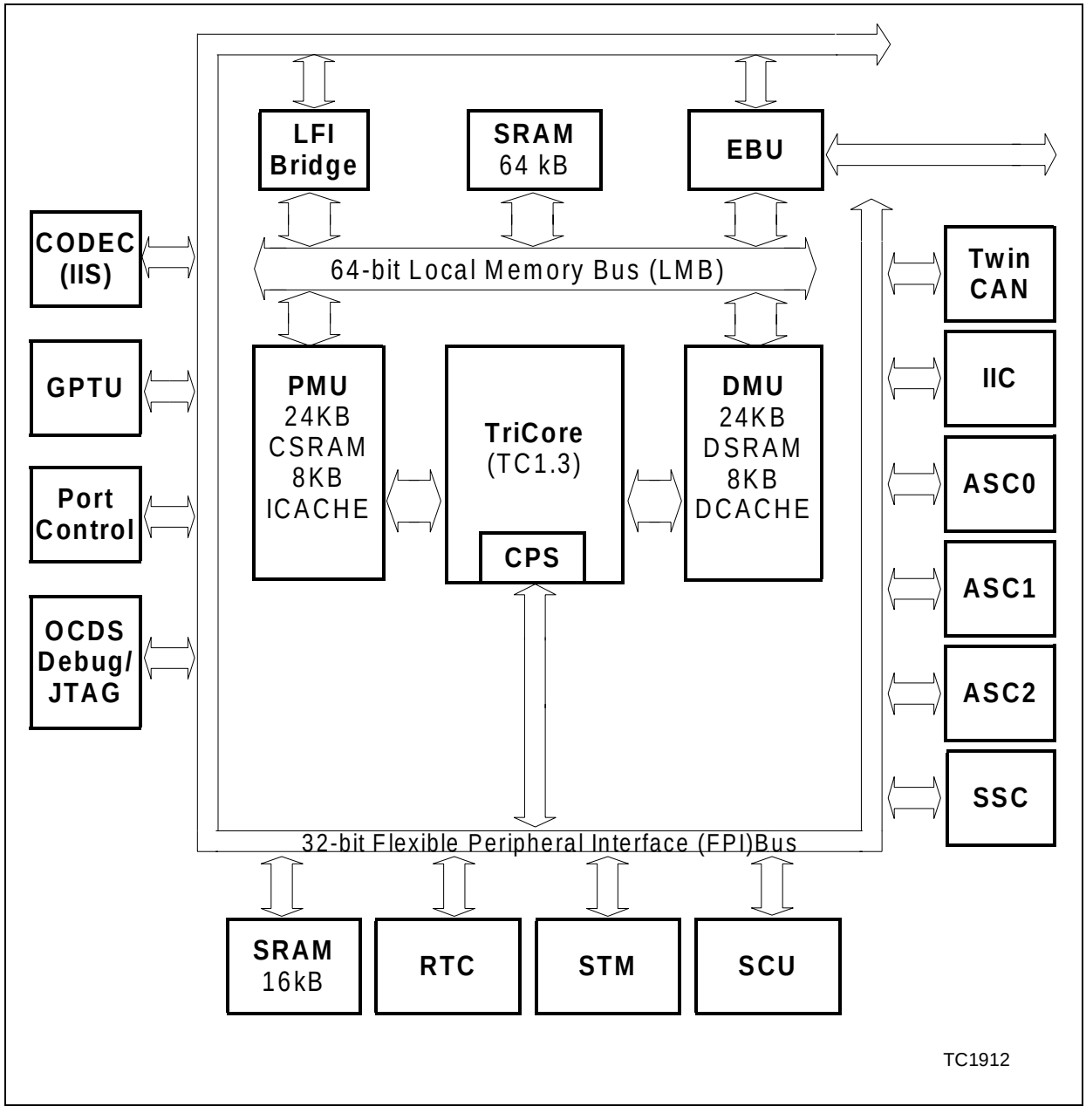

Figure 1 TC1912 Device Block Diagram

Target applications

- Bluetooth gateway (host for BT stack e.g. for Handsfree with EC/NR or remote diagnostics)
- Stand-alone speech Human Machine Interface
- Basic communication gateway
- Digital Audio processing (MP3 player, shock proof controller etc.)

PRELIMINARY

Logic Symbol

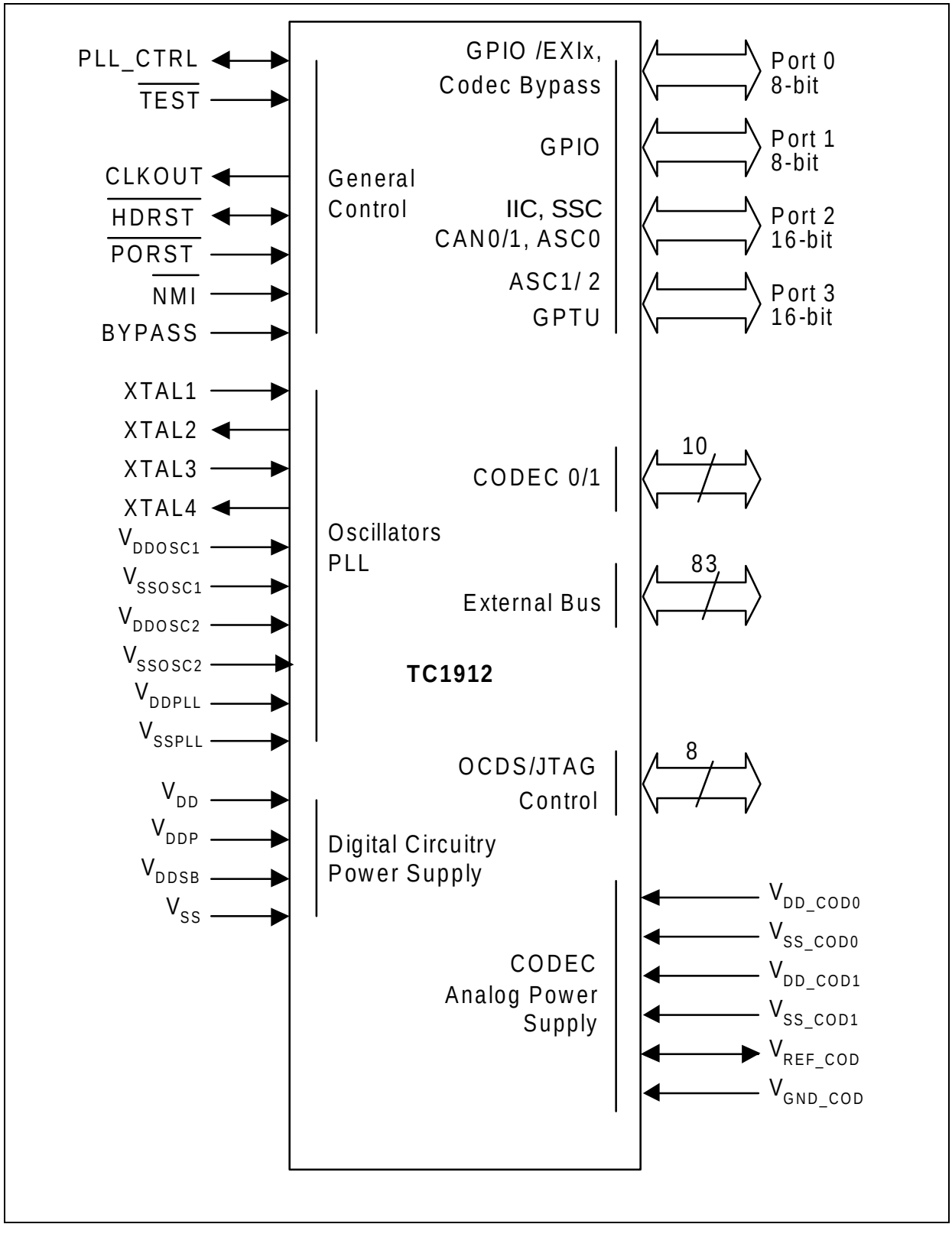

Figure 2 TC1912 Device Logic Symbol

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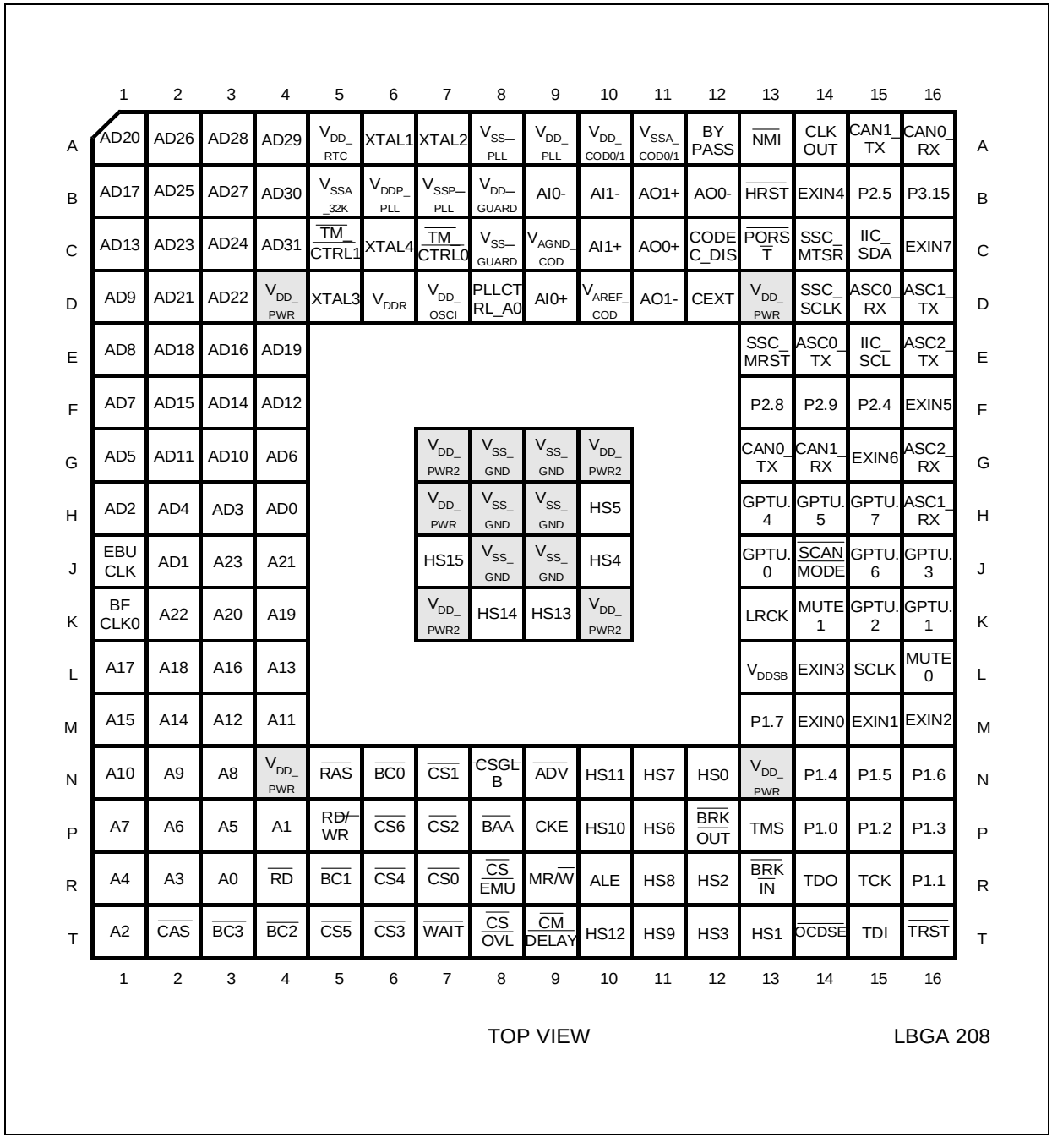
Pin Configuration



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	AD20	AD26	AD28	AD29	V_{DD_RTC}	XTAL1	XTAL2	V_{SS_PLL}	V_{DD_PLL}	$V_{DD\_COD0/1}$	$V_{SSA\_COD0/1}$	BY PASS	$\overline{NMI}$	CLK OUT	CAN1_TX	CAN0_RX	A
B	AD17	AD25	AD27	AD30	V_{SSA_32K}	V_{DDP_PLL}	V_{SSP_PLL}	V_{DD_GUARD}	AI0-	AI1-	AO1+	AO0-	$\overline{HRST}$	EXIN4	P2.5	P3.15	B
C	AD13	AD23	AD24	AD31	$\overline{TM}$_CTRL1	XTAL4	$\overline{TM}$_CTRL0	V_{SS_GUARD}	V_{AGND_COD}	AI1+	AO0+	CODEC_DIS	$\overline{PORST}$	SSC_MTSR	IIC_SDA	EXIN7	C
D	AD9	AD21	AD22	V_{DD_PWR}	XTAL3	V_{DDR}	V_{DD_OSCI}	PLLCTRL_A0	AI0+	V_{AREF_COD}	AO1-	CEXT	V_{DD_PWR}	SSC_SCLK	ASC0_RX	ASC1_TX	D
E	AD8	AD18	AD16	AD19									SSC_MRST	ASC0_TX	IIC_SCL	ASC2_TX	E
F	AD7	AD15	AD14	AD12									P2.8	P2.9	P2.4	EXIN5	F
G	AD5	AD11	AD10	AD6				V_{DD_PWR2}	V_{SS_GND}	V_{SS_GND}	V_{DD_PWR2}		CAN0_TX	CAN1_RX	EXIN6	ASC2_RX	G
H	AD2	AD4	AD3	AD0				V_{DD_PWR}	V_{SS_GND}	V_{SS_GND}	HS5		GPTU.4	GPTU.5	GPTU.7	ASC1_RX	H
J	EBU CLK	AD1	A23	A21				HS15	V_{SS_GND}	V_{SS_GND}	HS4		GPTU.0	$\overline{SCAN}$ MODE	GPTU.6	GPTU.3	J
K	BF CLK0	A22	A20	A19				V_{DD_PWR2}	HS14	HS13	V_{DD_PWR2}		LRCK	MUTE1	GPTU.2	GPTU.1	K
L	A17	A18	A16	A13									V_{DDSB}	EXIN3	SCLK	MUTE0	L
M	A15	A14	A12	A11									P1.7	EXIN0	EXIN1	EXIN2	M
N	A10	A9	A8	V_{DD_PWR}	$\overline{RAS}$	$\overline{BC0}$	$\overline{CS1}$	$\overline{CSGLB}$	$\overline{ADV}$	HS11	HS7	HS0	V_{DD_PWR}	P1.4	P1.5	P1.6	N
P	A7	A6	A5	A1	RD/$\overline{WR}$	$\overline{CS6}$	$\overline{CS2}$	$\overline{BAA}$	CKE	HS10	HS6	$\overline{BRKOUT}$	TMS	P1.0	P1.2	P1.3	P
R	A4	A3	A0	$\overline{RD}$	$\overline{BC1}$	$\overline{CS4}$	$\overline{CS0}$	$\overline{CS}$ EMU	MR/$\overline{W}$	ALE	HS8	HS2	$\overline{BRKIN}$	TDO	TCK	P1.1	R
T	A2	$\overline{CAS}$	$\overline{BC3}$	$\overline{BC2}$	$\overline{CS5}$	$\overline{CS3}$	$\overline{WAIT}$	$\overline{CS}$ $\overline{OVL}$	$\overline{CM}$ DELAY	HS12	HS9	HS3	HS1	$\overline{OCDSE}$	TDI	$\overline{TRST}$	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

TOP VIEW LBGA 208

Figure 3 TC1912 Pinning

PRELIMINARY

Pin List

Table 1 Pin Definitions and Functions

Symbol	BGA BALL	In/ Out[1)]	Functions	
			External Bus Unit Interface external address/data bus (multiplexed bus mode) or data bus (demultiplexed bus mode) for the EBU:	
AD0	H4	I/O,s	AD0	Address/data bus / Data bus line 0
AD1	J2	I/O,s	AD1	Address/data bus / Data bus line 1
AD2	H1	I/O,s	AD2	Address/data bus / Data bus line 2
AD3	H3	I/O,s	AD3	Address/data bus / Data bus line 3
AD4	H2	I/O,s	AD4	Address/data bus / Data bus line 4
AD5	G1	I/O,s	AD5	Address/data bus / Data bus line 5
AD6	G4	I/O,s	AD6	Address/data bus / Data bus line 6
AD7	F1	I/O,s	AD7	Address/data bus / Data bus line 7
AD8	E1	I/O,s	AD8	Address/data bus / Data bus line 8
AD9	D1	I/O,s	AD9	Address/data bus / Data bus line 9
AD10	G3	I/O,s	AD10	Address/data bus / Data bus line 10
AD11	G2	I/O,s	AD11	Address/data bus / Data bus line 11
AD12	F4	I/O,s	AD12	Address/data bus / Data bus line 12
AD13	C1	I/O,s	AD13	Address/data bus / Data bus line 13
AD14	F3	I/O,s	AD14	Address/data bus / Data bus line 14
AD15	F2	I/O,s	AD15	Address/data bus / Data bus line 15
AD16	E3	I/O,s	AD16	Address/data bus / Data bus line 16
AD17	B1	I/O,s	AD17	Address/data bus / Data bus line 17
AD18	E2	I/O,s	AD18	Address/data bus / Data bus line 18
AD19	E4	I/O,s	AD19	Address/data bus / Data bus line 19
AD20	A1	I/O,s	AD20	Address/data bus / Data bus line 20
AD21	D2	I/O,s	AD21	Address/data bus / Data bus line 21
AD22	D3	I/O,s	AD22	Address/data bus / Data bus line 22
AD23	C2	I/O,s	AD23	Address/data bus / Data bus line 23
AD24	C3	I/O,s	AD24	Address/data bus / Data bus line 24
AD25	B2	I/O,s	AD25	Address/data bus / Data bus line 25
AD26	A2	I/O,s	AD26	Address/data bus / Data bus line 26
AD27	B3	I/O,s	AD27	Address/data bus / Data bus line 27
AD28	A3	I/O,s	AD28	Address/data bus / Data bus line 28
AD29	A4	I/O,s	AD29	Address/data bus / Data bus line 29
AD30	B4	I/O,s	AD30	Address/data bus / Data bus line 30
AD31	C4	I/O,s	AD31	Address/data bus / Data bus line 31

PRELIMINARY

Table 1 Pin Definitions and Functions

Symbol	BGA BALL	In/ Out[1)]	Functions	
			External Bus Unit Interface (continued) external address bus for the EBU or chip select output lines.	
A0	R3	I/O,s	A0	Address bus line 0
A1	P4	I/O,s	A1	Address bus line 1
A2	T1	I/O,s	A2	Address bus line 2
A3	R2	I/O,s	A3	Address bus line 3
A4	R1	I/O,s	A4	Address bus line 4
A5	P3	I/O,s	A5	Address bus line 5
A6	P2	I/O,s	A6	Address bus line 6
A7	P1	I/O,s	A7	Address bus line 7
A8	N3	I/O,s	A8	Address bus line 8
A9	N2	I/O,s	A9	Address bus line 9
A10	N1	I/O,s	A10	Address bus line 10
A11	M4	I/O,s	A11	Address bus line 11
A12	M3	I/O,s	A12	Address bus line 12
A13	L4	I/O,s	A13	Address bus line 13
A14	M2	I/O,s	A14	Address bus line 14
A15	M1	I/O,s	A15	Address bus line 15
A16	L3	I/O,s	A16	Address bus line 16
A17	L1	I/O,s	A17	Address bus line 17
A18	L2	I/O,s	A18	Address bus line 18
A19	K4	I/O,s	A19	Address bus line 19
A20	K3	I/O,s	A20	Address bus line 20
A21	J4	I/O,s	A21	Address bus line 21
A22	K2	I/O,s	A22	Address bus line 22
A23	J3	I/O,s	A23	Address bus line 23
$\overline{CS0}$	R7	O,u	$\overline{CS0}$	Chip select output 0
$\overline{CS1}$	N7	O,u	$\overline{CS1}$	Chip select output 1
$\overline{CS2}$	P7	O,u	$\overline{CS2}$	Chip select output 2
$\overline{CS3}$	T6	O,u	$\overline{CS3}$	Chip select output 3
$\overline{CS4}$	R6	O,u	$\overline{CS4}$	Chip select output 4
$\overline{CS5}$	T5	O,u	$\overline{CS5}$	Chip select output 5
$\overline{CS6}$	P6	O,u	$\overline{CS6}$	Chip select output 6
$\overline{CSEMU}$	R8	O,u	$\overline{CSEMU}$	Chip select for emulator region
$\overline{CSOVL}$	T8	O,u	$\overline{CSOVL}$	Chip select for emulator overlay memory

PRELIMINARY

Table 1 Pin Definitions and Functions

Symbol	BGA BALL	In/ Out[1)]	Functions
			External Bus Unit Interface (continued)
			control bus for the EBU control lines.
$\overline{RD}$	R4	I/O,u	$\overline{RD}$ Read control line
RD/$\overline{WR}$	P5	I/O,u	RD/$\overline{WR}$ Write control line
$\overline{ALE}$	R10	O,d	$\overline{ALE}$ Address latch enable
$\overline{ADV}$	N9	O,u	$\overline{ADV}$ Address valid output
$\overline{BC0}$	N6	I/O,u	$\overline{BC0}$ Byte control line 0
$\overline{BC1}$	R5	I/O,u	$\overline{BC1}$ Byte control line 1
$\overline{BC2}$	T4	I/O,u	$\overline{BC2}$ Byte control line 2
$\overline{BC3}$	T3	I/O,u	$\overline{BC3}$ Byte control line 3
$\overline{WAIT}$	T7	I/O,u	$\overline{WAIT}$ Wait input
$\overline{BAA}$	P8	O,u	$\overline{BAA}$ Burst address advance output
EBUCLK	J1	O,u	EBUCLK External Bus Clock
BFCLK0	K1	O,u	BFCLK0 Additional clock
$\overline{CSGLB}$	N8	O,u	$\overline{CSGLB}$ Chip Select Global
$\overline{CMDELAY}$	T9	I,u	$\overline{CMDELAY}$ Command Delay
MR/$\overline{W}$	R9	O,u	MR/$\overline{W}$ Motorola-style Read/Write
CKE	P9	O,u	CKE Clock Enable
$\overline{RAS}$	N5	O,u	$\overline{RAS}$ Row Address Strobe
$\overline{CAS}$	T2	O,u	$\overline{CAS}$ Column Address Strobe
P0			**Port 0**
			Port 0 is an 8-bit general purpose I/O port, overlaid with codec digital signals and external interrupt inputs (P0.[3:0]).
P0.0	M14	I/O	EXI0IN External interrupt input 0
P0.1	M15	I/O	EXI1IN External interrupt input 1 or DATA_IN
P0.2	M16	I/O	EXI2IN External interrupt input 2 or DATA_OUT
P0.3	L14	I/O	EXI3IN External interrupt input 3 or MCLK
P0.4	L15	I/O	GPIO or SCLK
P0.5	K13	I/O	GPIO or LRCK
P0.6	L16	I/O	GPIO or MUTE0
P0.7	K14	I/O	GPIO or MUTE1

PRELIMINARY

Table 1 Pin Definitions and Functions

Symbol	BGA BALL	In/ Out[1)]	Functions
P1			**Port 1** Port 1 is a 8-bit bidirectional General Purpose I/O port
P1.0	P14	I/O	GPIO only
P1.1	R16	I/O	GPIO only
P1.2	P15	I/O	GPIO only
P1.3	P16	I/O	GPIO only
P1.4	N14	I/O	GPIO only
P1.5	N15	I/O	GPIO only
P1.6	N16	I/O	GPIO only
P1.7	M13	I/O	GPIO only
P2			**Port 2** Port 2 is a 16-bit bidirectional general purpose I/O port and input/output for serial interfaces (IIC, ASC0, SSC)
P2.0	A16	I/O	RXDCAN0 CAN 0 receiver input
P2.1	G13	I/O	TXDCAN0 CAN 0 transmitter output
P2.2	G14	I/O	RXDCAN1 CAN 1 receiver input
P2.3	A15	I/O	TXDCAN1 CAN 1 transmitter output
P2.4	F15	I/O	GPIO only
P2.5	B15	I/O	GPIO only
P2.6	E15	I/O	SCL IIC Serial Port Clock
P2.7	C15	I/O	SDA IIC Serial Port Data
P2.8	F13	I/O	Open Drain GPIO
P2.9	F14	I/O	Open Drain GPIO
P2.10	D15	I/O	RXD0 ASC0 receiver input/output
P2.11	E14	I/O	TXD0 ASC0 transmitter output
P2.12	D14	I/O	SCLK SSC clock line
P2.13	E13	I/O	MRST SSC master receive / slave transmit
P2.14	C14	I/O	MTSR SSC master transmit / slave receive
P2.15	B14	I/O	EXI4IN External Interrupt Input 5 PLL_CLC.LOCK Monitoring of PLL_CLC.LOCK

PRELIMINARY

Table 1 Pin Definitions and Functions

Symbol	BGA BALL	In/ Out[1)]	Functions
P3			**Port 3** Port 3 is a 16-bit bidirectional general purpose I/O port which is also used as input/output for serial interfaces (ASC1) and timer (GPTU)
P3.0	J13	I/O	GPTU.0 GPTU I/O line 0
P3.1	K16	I/O	GPTU.1 GPTU I/O line 1
P3.2	K15	I/O	GPTU.2 GPTU I/O line 2
P3.3	J16	I/O	GPTU.3 GPTU I/O line 3
P3.4	H13	I/O	GPTU.4 GPTU I/O line 4
P3.5	H14	I/O	GPTU.5 GPTU I/O line 5
P3.6	J15	I/O	GPTU.6 GPTU I/O line 6
P3.7	H15	I/O	GPTU.7 GPTU I/O line 7
P3.8	H16	I/O	RXD1 ASC1 receiver input/output
P3.9	D16	I/O	TXD1 ASC1 transmitter output
P3.10	G16	I/O	RXD2 ASC2 receiver input/output
P3.11	E16	I/O	TXD2 ASC2 transmitter output OSCBYP Latch-In Input Pin
P3.12	F16	I/O	EXI5IN External Interrupt Input 5 HWCFG0 Latch-In
P3.13	G15	I/O	EXI6IN External Interrupt Input 6 HWCFG1 Latch-In
P3.14	C16	I/O	EXI7IN External Interrupt Input 7 HWCFG2 Latch-In
P3.15	B16	I/O	GPIO only
CODEC			**CODEC**
AI0+	D9	I	CODEC 0 Non-Inverting Input
AI0-	B9	I	CODEC 0 Inverting Input
AO0+	C11	O	CODEC 0 Non-Inverting Output
AO0-	B12	O	CODEC 0 Inverting Output
AI1+	C10	I	CODEC 1 Non-Inverting Input
AI1-	B10	I	CODEC 1 Inverting Input
AO1+	B11	O	CODEC 1 Non-Inverting Output
AO1-	D11	O	CODEC 1 Inverting Output
CEXT	D12	I	CODEC External Clock Input
CODEC_DIS	C12	I	CODEC Disable (power saving)

PRELIMINARY

Table 1 Pin Definitions and Functions

Symbol	BGA BALL	In/ Out[1)]	Functions
DEBUG			**DEBUG (OCDS/JTAG Control)**
$\overline{\text{TRST}}$	T16	I,d	Reset/module enable
TCK	R15	I,u	JTAG clock input
TDI	T15	I,u	Serial data input
TDO	R14	O	Serial data output
TMS	P13	I,u	State machine control signal
$\overline{\text{OCDSE}}$	T14	I,u	OCDS enable input
$\overline{\text{BRKIN}}$	R13	I,u	OCDS break input
$\overline{\text{BRKOUT}}$	P12	O	OCDS break output
Test			**Test Pins**
SCAN_MODE	J14	I	Scan Mode
PLLCTRL_AO	D8	I	Control current of different analog stages
TM_CTRL0	C7	I	Test Mode Control 0
TM_CTRL1	C5	I	Test Mode Control 1
Reserved Pins			**Reserved Internal Test and Heat Sink Pins.** Must be routed as isolated pads on the PCB.
HS0	N12	IO	Heat Sink 0
HS1	T13	IO	Heat Sink 1
HS2	R12	IO	Heat Sink 2
HS3	T12	IO	Heat Sink 3
HS4	J10	IO	Heat Sink 4
HS5	H10	IO	Heat Sink 5
HS6	P11	IO	Heat Sink 6
HS7	N11	IO	Heat Sink 7
HS8	R11	IO	Heat Sink 8
HS9	T11	IO	Heat Sink 9
HS10	P10	IO	Heat Sink 10
HS11	N10	IO	Heat Sink 11
HS12	T10	IO	Heat Sink 12
HS13	K9	IO	Heat Sink 13
HS14	K8	IO	Heat Sink 14
HS15	J7	IO	Heat Sink 15
BYPASS	A12	I,d	PLL Bypass Control Input
$\overline{\text{NMI}}$	A13	I,u	Non-Maskable Interrupt Input
$\overline{\text{HRST}}$	B13	I/O,u	Bidirectional Hardware Reset

PRELIMINARY

Table 1 Pin Definitions and Functions

Symbol	BGA BALL	In/ Out[1)]	Functions
$\overline{\text{PORST}}$	C13	I,u	Power-on Reset Input (must be active during power up)
CLKOUT	A14	O	CPU Clock Output
XTAL1 XTAL2	A6 A7	I O	PLL/Oscillator Input/Output
XTAL3 XTAL4	D5 C6	I O	Real Time Clock Oscillator input/output (32 KHz)
V_{AREF_COD}	D10	-	Codec 0,1 Reference Voltage
V_{AGND_COD}	C9	-	Codec 0,1 Reference Ground
$V_{DD\_COD0/1}$	A10	-	Codec Pad and Analog Power Supply (3.3V)
$V_{SSA\_COD0/1}$	A11	-	Codec Pad and Analog Ground
V_{DD_GUARD}	B8	-	Guard Ring Supply (1.8V)
V_{SS_GUARD}	C8	-	Guard Ring Ground (1.8V)
V_{DD_OSCI}	D7	-	Main Oscilator Power Supply (1.8V)
V_{DD_RTC}	A5	-	RTC Oscilator Core Supply (1.8V)
V_{SSA_32K}	B5	-	RTC and Main Osc. Core Ground (1.8V)
V_{DDP_PLL}	B6	-	RTC and Main Osc. Supply (3.3V)
V_{SSP_PLL}	B7	-	RTC and Main Osc. Ground (3.3V)
V_{DDPLL}	A9	-	PLL Supply (1.8V)
V_{SSPLL}	A8	-	PLL Ground (1.8V)
V_{DDR}	D6	-	SRAM Power Supply (1.8V)
V_{DDSB}	L13	-	SRAM Stand-By Power Supply (1.8V)
V_{DD_PWR}	D4 D13 H7 N4 N13	- - - - -	3.3V Power Supply
V_{DD_PWR2}	G7 G10 K7 K10	- - - -	1.8V Power Supply

PRELIMINARY

Table 1 Pin Definitions and Functions

Symbol	BGA BALL	In/ Out[1)]	Functions
V_{SS_GND}	G8 G9 H8 H9 J8 J9	- - - - - -	Digital Power Ground

1) The notification ',u' after the input/output type defines an internal pull-up resistor. An internal pull-down resistor is indicated by ',d'. For the lines AD[31:0] and A[23:0], the type of the pull device can be selected 's'.

PRELIMINARY

System Architecture and Control

32-Bit TriCore CPU

- 32-bit architecture with 4-GByte unified data, program and input/output address space
- Fast automatic context-switch
- Dual 16 x 16 Multiply-accumulate (MAC) unit
- Saturating integer arithmetic
- Register based design with multiple variable register banks
- Bit handling
- Packed data operations
- Zero overhead loop
- Precise exceptions
- Flexible power management

Instruction Set with High Efficiency:

- 16/32-bit instructions for reduced code size
- Little endian byte ordering with support for big and little endian byte ordering at bus interface
- Boolean, array of bits, character, signed and unsigned integer, integer with saturation, signed fraction, double word integers and IEEE-754 single precision floating-point data types
- Bit, 8-bit byte, 16-bit half word, 32-bit word and 64-bit double word data formats
- Powerful instruction set
- Flexible and efficient addressing mode for high code density

PRELIMINARY

On-chip Code Memories

Local Memory Bus Memory (LMBRAM):

Address range of the 64 KByte Local Memory Bus Memory:

- C000 0000_H - C000 $FFFF_H$ (in segment 12 for cached operation)
- E800 0000_H - E800 $FFFF_H$ (in segment 14 for non-cached operation)

PMU Scratch-Pad SRAM (CSRAM):

The Program Memory Unit (PMU) memory consists of 24-KByte Code Scratchpad RAM (CSRAM) and 8-KByte Instruction Cache (ICACHE).

Address range of the CSRAM:

- D400 0000_H - D400 $5FFF_H$

On-chip Data Memories

DMU Scratch-Pad SRAM (DSRAM):

The Data Memory Unit (DMU) memory consists of 24-KByte Data Scratchpad RAM (DSRAM) and 8-KByte Data Cache (DCACHE).

Address range of the DSRAM:

- D000 0000_H - D000 $5FFF_H$

FPI-Bus Data Memory (FPIDRAM):

The FPI-Bus Data Memory (FPIDRAM) is a 16-KByte static RAM located on the FPI-Bus. It contains two parts: FPIDRAM0 and FPIDRAM1. One half of it (FPIDRAM1) can be used for standby power operation.

Address range of the FPI Data Memory:

- 9FFF 8000_H - 9FFF $BFFF_H$ (in segment 9 for cached operation)
- BFFF 8000_H - BFFF $BFFF_H$ (in segment 11 for non-cached operation)

PRELIMINARY

System Control Unit (SCU)

The System Control Unit of the TC1912 basically handles all system control tasks. All these system functions are tightly coupled and therefore they are handled physically by one unit, the SCU. The system tasks of the SCU are:

- Clock Generation and Control
- Reset control
- Power Management control and wake-up
- Watchdog timer
- Device identification
- Standby SRAM control
- External interrupt capability (8 sources)

System timer (STM)

The System Timer is designed for global system timing applications requiring both high precision and long range. It is used by the CPU for software operating system issues.

Features:

- Free-running 56-bit counter
- All 56 bits can be read synchronously
- Different 32-bit portions of the 56-bit counter can be read synchronously
- Driven by clock, f_{STM} (normally identical with the system clock).
- Counting begins at power-on reset
- Continuous operation is not affected by any reset condition except power-on reset

External Bus Interface (EBU_LMB)

EBU_LMB is connected to the Local Memory Bus (LMB) of the TC1912 and also to the FPI Bus. EBU_LMB is always a slave on the LMB and a master/slave on the FPI bus.

Any LMB masters thus can access external memories or devices through EBU_LMB. Currently the maximum length of the bursts are according to the size of program and data cache lines, i.e. 8 x 32-bit words. Single transfers (non-burst) are supported for 8-bit, 16-bit and 32-bit wide access.

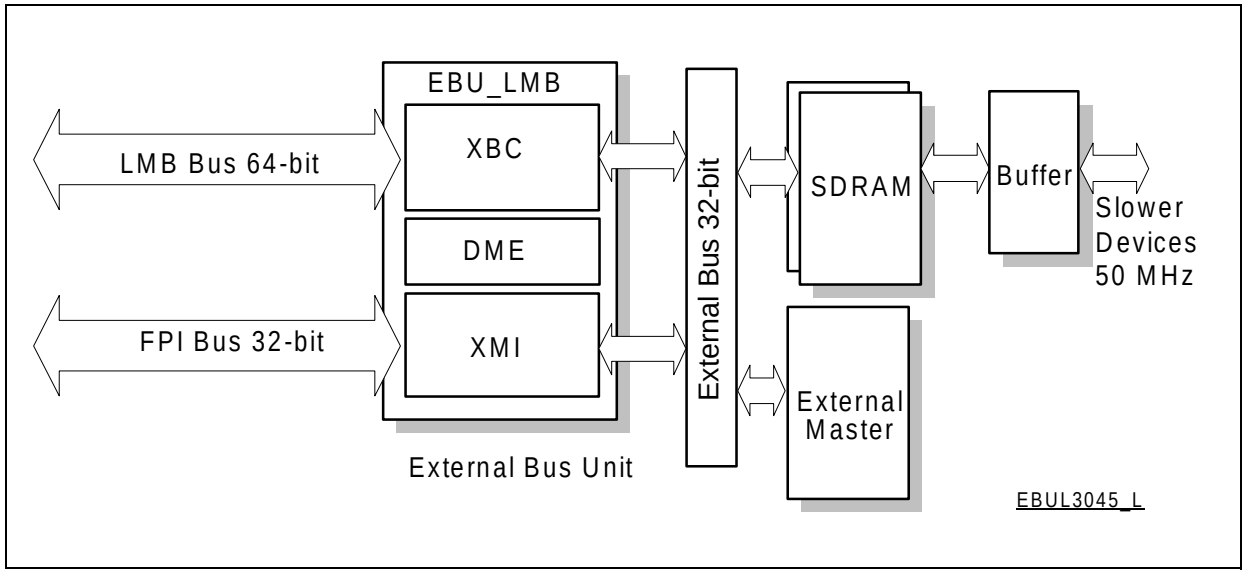


Figure 4 EBU_LMB block diagram

Features supported in EBU_LMB:

- Local Memory Bus (LMB 64-bit) support.
- External bus frequency: LMB frequency = 1:1 or 1:2 or 1:4.
- Highly programmable access parameters.
- Intel-style and Motorola-style peripheral/device support.
- SDRAM support (burst access, multibanking, precharge, refresh).
- 16- and 32-bit SDRAM data bus and support of 64, 128 and 256MBit devices.
- Burst flash support.
- Multiplexed access (address & data on the same bus) when DRAM is not present on the External Bus.
- Data Buffering: Code Prefetch Buffer, Read/Write Buffer.
- External master arbitration (compatible to C166 and other TriCore devices).
- 8 programmable address regions (1 dedicated for emulator).
- Little-Endian and Big-Endian support.
- $\overline{\text{CS}}$glb signal, dedicated pin, bit programmable to combine one or more $\overline{\text{CS}}$ lines, for buffer control.
- $\overline{\text{RMW}}$ signal reflecting a read-modify-write action.
- Signal for controlling data flow of slow-memory buffer.
- Slave unit for external (off-chip) master to access devices on the FPI bus.
- Master unit for FPI master to access external (off-chip) devices.
- Data Mover Engine.

PRELIMINARY

Interrupt System

- Flexible interrupt prioritizing scheme with 256 interrupt priority levels
- Fast interrupt response

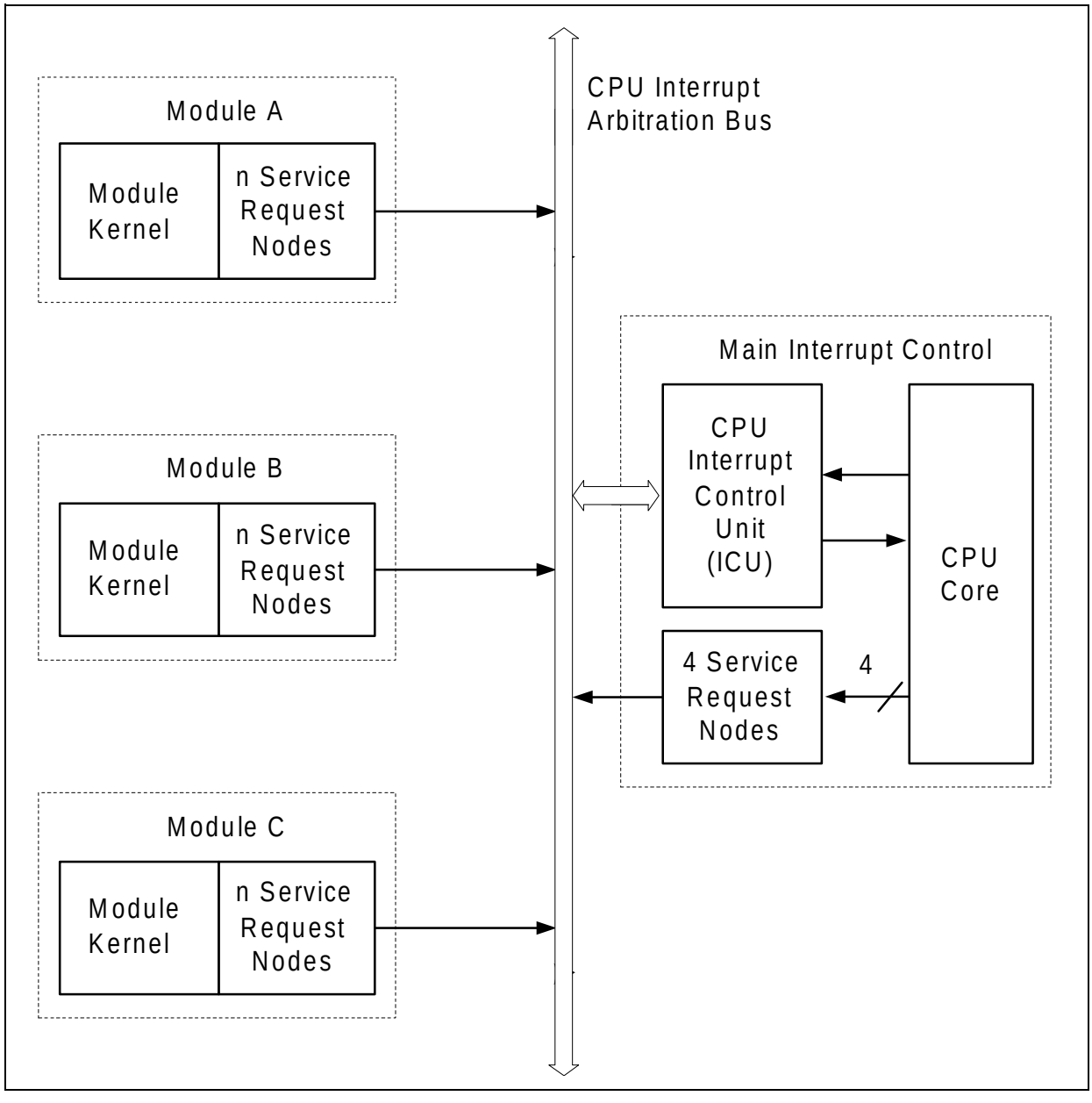


Figure 5 Block Diagram Interrupt System

PRELIMINARY

FPI-Bus

The Flexible Peripheral Interconnect Bus is designed with the requirements of high-performance Systems-on-Chip in mind.

Key Features:

- Core independent
- Multi-master capability
- Demultiplexed operation
- Clock synchronous
- Peak transfer rate of up to 200 MBytes/s (@ 50 MHz bus clock)
- Address and data bus scalable (32 bit address bus, 32 bit data bus)
- 8-/16- and 32 bit data transfers
- Broad range of transfer types from single to multiple data transfers
- Burst transfer capability
- EMI and power consumption minimized

LMB-Bus

The Local Memory Bus is a synchronous, pipelined, split bus with variable block size transfer support. All signals relate to the positive clock edge.

The protocol supports 8,16,32 & 64 bits single beat transactions and variable length 64 bits block transfers.

Key Features:

The LMB provides the following features:

- Optimized for high speed and high performance
- 32 bit address, 64 bit data busses
- Central simple per cycle arbitration
- Slave controlled wait state insertion
- Address pipelining (max depth - 2)
- Split transactions
- Variable block length - 2, 4 or 8 beats of 64 bit data

PRELIMINARY

On-Chip Debug System (OCDS)

The TC1912 architecture is supporting OCDS Level 1. This means access to FPI Bus and the whole FPI address space via the JTAG interface pins.

On-Chip Peripheral Units

The TC1912 offers several on-chip peripheral units such as serial controllers, timer units, and Codec module. Within the TC1912 all these peripheral units are connected to the TriCore CPU/system via the FPI (Flexible Peripheral Interconnect) Bus. Several IO lines on the TC1912 ports are reserved for these peripheral units to communicate with the external world.

Peripheral Units of the TC1912:

- Three Asynchronous/Synchronous Serial Channels with baudrate generator, parity, framing and overrun error detection, IrDA mode, FIFO buffers.
- One High Speed Synchronous Serial Channels with programmable data length and shift direction
- TwinCAN Module with two interconnected CAN nodes for high efficiency data handling via FIFO buffering and gateway data transfer
- IIC module
- One multi-functional General Purpose Timer Units with three 32-bit timer/counter
- Dual channel Codec interface
- GPIO blocks

Table 2 Peripheral Modules

Module	Address Range	I/O Lines	Interrupt Nodes
Asynchronous Serial Channel 0 (ASC0)	$F000\ 0A00_H$ - $F000\ 0AFF_H$	RDX0, TDX0	ASC0_TSRC ASC0_RSRC ASC0_ESRC ASC0_TBSRC
Asynchronous Serial Channel 1 (ASC1)	$F000\ 0B00_H$ - $F000\ 0BFF_H$	RDX1, TDX1	ASC1_TSRC ASC1_RSRC ASC1_ESRC ASC1_TBSRC
Asynchronous Serial Channel 2 (ASC2)	$F000\ 0C00_H$ - $F000\ 0CFF_H$	RDX2, TDX2	ASC2_TSRC ASC2_RSRC ASC2_ESRC ASC2_TBSRC
Synchronous Serial Channel (SSC)	$F000\ 0800_H$ - $F000\ 08FF_H$	SCLK, MRST, MTSR	SSC_TSRC SSC_RSRC SSC_ESRC

PRELIMINARY

Table 2 Peripheral Modules (cont'd)

Module	Address Range	I/O Lines	Interrupt Nodes
Inter-IC Bus (IIC)	$F000\ 0500_H$ - $F000\ 05FF_H$	SCL, SDA	IIC_XP0SRC IIC_XP1SRC IIC_XP2SRC
Real Time Clock (RTC)	$F000\ 0100_H$ - $F000\ 01FF_H$	-	RTC_SRC
System Timer Unit (STM)	$F000\ 0300_H$ - $F000\ 03FF_H$	-	-
General Purpose Timer (GPTU)	$F000\ 0700_H$ - $F000\ 07FF_H$	GPTU	GPTU_SRC0..7
CAN (TwinCAN)	$F010\ 0000_H$ - $F010\ 0BFF_H$	RXDCAN[1:0], TXDCAN[1:0]	CAN_SRC0..7
Speech Interface (Codec)	$F000\ 2400_H$ - $F000\ 24FF_H$	2*2 analog IN, 2*2 analog OUT, CEXT, CODEC_DIS	CODEC_SRC0..5

PRELIMINARY

Asynchronous/Synchronous Serial Interfaces (ASC 0/1/2)

The Asynchronous/Synchronous Serial Interface ASC provides serial communication between the TriCore and other microcontrollers, microprocessors or external peripherals.

Features:

- Full duplex asynchronous operating modes
  - 8- or 9-bit data frames, LSB first
  - Parity bit generation/checking
  - One or two stop bits
  - Baudrate from 3.125 MBaud to 0.74 Baud (@ 50 MHz module clock)
  - Multiprocessor mode for automatic address/data byte detection
  - Loop-back capability
- Half-duplex 8-bit synchronous operating mode
  - Baudrate from 6.25 MBaud to 637 Baud (@ 50 MHz module clock)
- Double buffered transmitter/receiver
- Interrupt generation
  - on a transmitter buffer empty condition
  - on a transmit last bit of a frame condition
  - on a receiver buffer full condition
  - on an error condition (frame, parity, overrun error)
- Support for IrDA
- Automatic Baudrate Detection
- 8 Byte FIFO

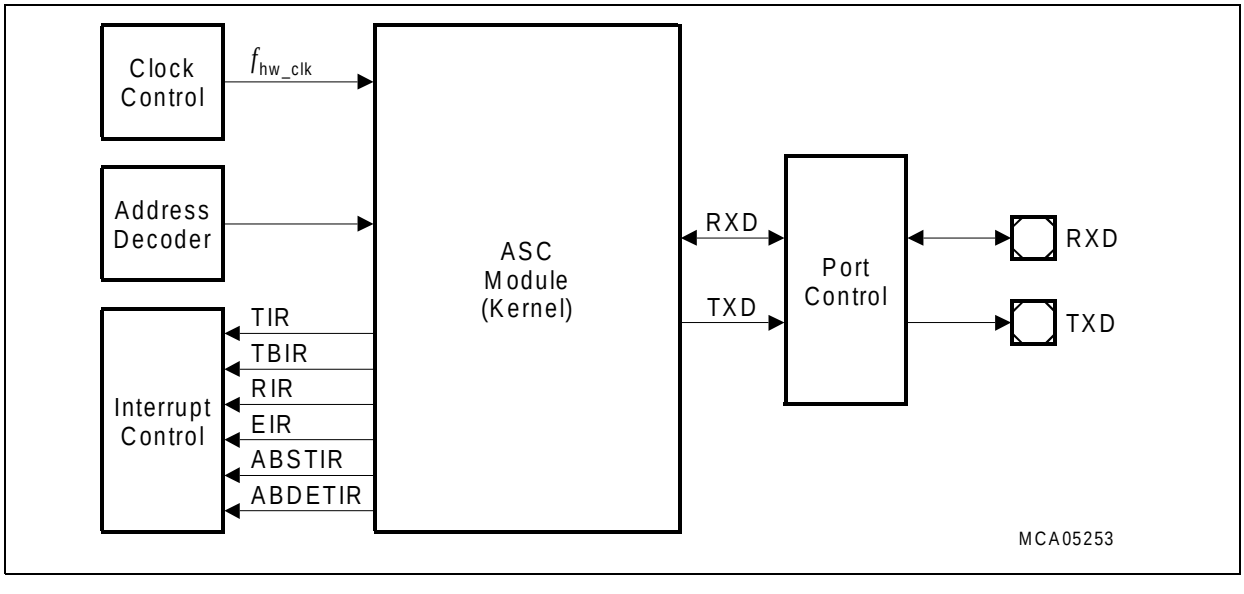


Figure 6 General Block Diagram of the ASC Interface

PRELIMINARY

High-Speed Synchronous Serial Interface (SSC)

The High Speed Synchronous Serial Interface SSC provides serial communication between microcontrollers, microprocessors or external peripherals. The SSC supports full-duplex and half-duplex synchronous communication up to 25 MBaud (@ 50 MHz module clock). The serial clock signal can be generated by the SSC itself (master mode) or be received from an external master (slave mode). Data width, shift direction, clock polarity and phase are programmable. This allows communication with SPI-compatible devices. Transmission and reception of data are double-buffered. A 16-bit baud rate generator provides the SSC with a separate serial clock signal.

Features:

- Master and slave mode operation
  - Full-duplex or half-duplex operation
- Flexible data format
  - Programmable number of data bits : 2 to 16 bit
  - Programmable shift direction : LSB or MSB shift first
  - Programmable clock polarity : idle low or high state for the shift clock
  - Programmable clock/data phase : data shift with leading or trailing edge of SCLK
- Maximum baudrate: 25 MBaud in Master, 12.5 in Slave mode (@ 50 MHz module clock)

Interrupt generation
  - on a transmitter empty condition
  - on a receiver full condition
  - on an error condition (receive, phase, baudrate, transmit error)
- Three pin interface

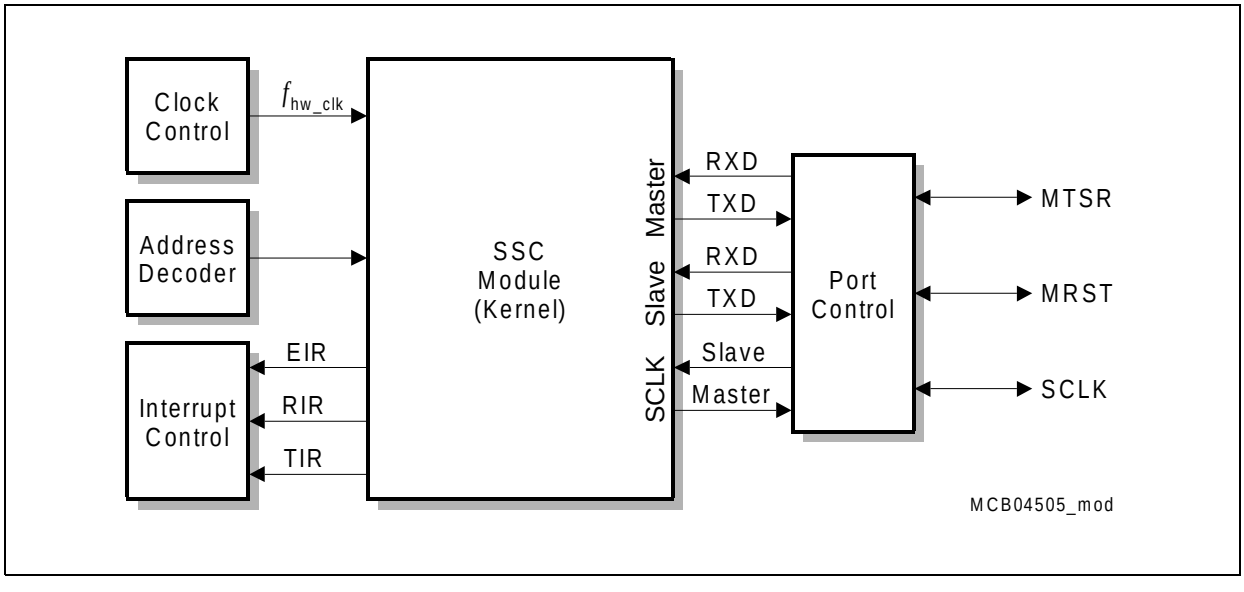


Figure 7 General Block Diagram of the SSC Interface

PRELIMINARY

Inter-IC Interface (IIC)

IIC supports a certain protocol to allow devices to communicate directly with each other via two wires. One line is responsible for clock transfer and synchronization (SCL), the other is responsible for the data transfer (SDA).

The on-chip IIC Bus module connects the platform buses to other external controllers and/or peripherals via the two-line serial IIC interface. The IIC Bus module provides communication at data rates of up to 400 kBit/s and features 7-bit addressing as well as 10-bit addressing. This module is fully compatible to the IIC bus protocol.

The module can operate in three different modes:

Master mode, where the IIC controls the bus transactions and provides the clock signal.

Slave mode, where an external master controls the bus transactions and provides the clock signal.

Multimaster mode, where several masters can be connected to the bus, i.e. the IIC can be master or slave.

The on-chip IIC bus module allows efficient communication via the common IIC bus. The module unloads the CPU of low level tasks like:

- (De)Serialization of bus data.
- Generation of start and stop conditions.
- Monitoring the bus lines in slave mode.
- Evaluation of the device address in slave mode.
- Bus access arbitration in multimaster mode.

IIC Features:

- Extended buffer allows up to 4 send/receive data bytes to be stored.
- Selectable baud rate generation.
- Support of standard 100 kBaud and extended 400 kBaud data rates.
- Operation in 7-bit addressing mode or 10-bit addressing mode.
- Flexible control via interrupt service routines or by polling.

PRELIMINARY

CAN Interface (TwinCAN)

Figure 8 shows a global view of the functional blocks of the TwinCAN module.

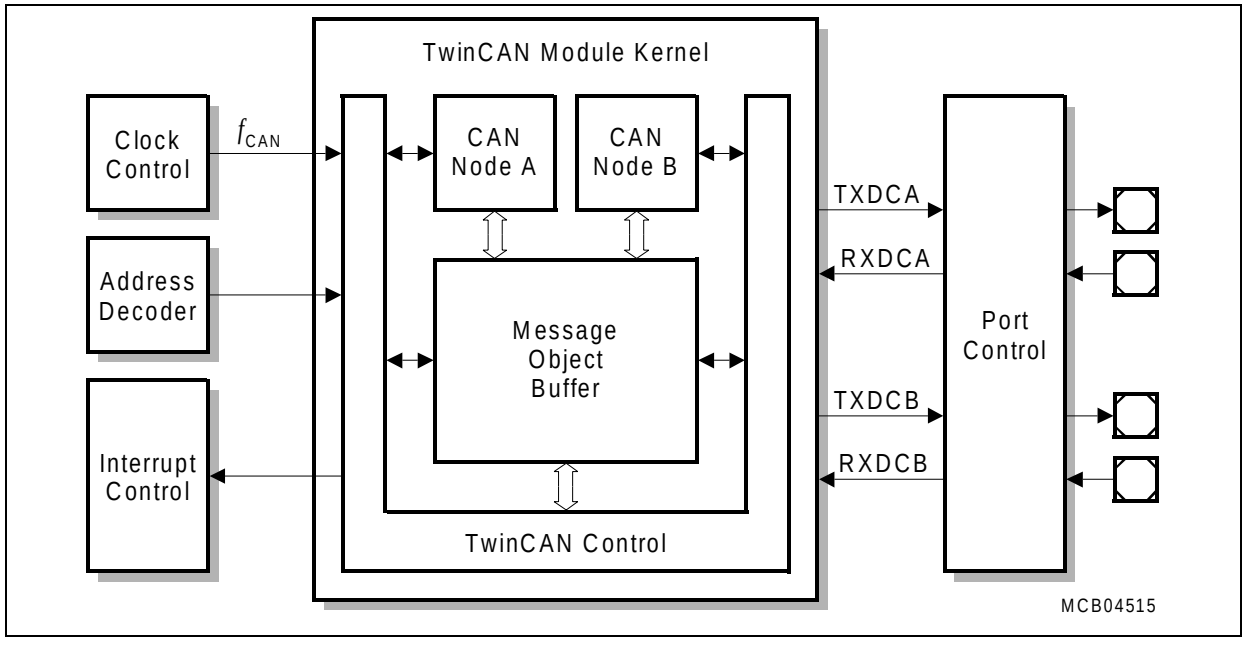


Figure 8 General Block Diagram of the TwinCAN Interfaces

TwinCAN Features:

- CAN functionality according to CAN specification V2.0 B active.
- Dedicated control registers are provided for each CAN node.
- A data transfer rate up to 1MBaud is supported.
- Flexible and powerful message transfer control and error handling capabilities are implemented.
- Full-CAN functionality: 32 message objects can be individually
  - assigned to one of the two CAN nodes,
  - configured as transmit or receive object,
  - participate in a 2,4,8,16 or 32 message buffer with FIFO algorithm,
  - setup to handle frames with 11 bit or 29 bit identifiers,
  - provided with programmable acceptance mask register for filtering,
  - monitored via a frame counter,
  - configured to Remote Monitoring Mode.
- Up to eight individually programmable interrupt nodes can be used.
- CAN Analyzer Mode for bus monitoring is implemented.

The TwinCAN module has four IO lines. The TwinCAN module is further supplied by a clock control, interrupt control, address decoding, and port control logic.

PRELIMINARY

The CAN module contains two Full-CAN nodes operating independently or exchanging data and remote frames via a gateway function. Transmission and reception of CAN frames is handled in accordance to CAN specification V2.0 part B (active). Each of the two Full-CAN nodes can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

Both CAN nodes share the TwinCAN module's resources in order to optimize the CAN bus traffic handling and to minimize the CPU load. The flexible combination of Full-functionality and FIFO architecture reduces the efforts to fulfill the real-time requirements of complex embedded control applications. Improved CAN bus monitoring functionality as well as the increased number of message objects permit precise and comfortable CAN bus traffic handling.

Depending on the application, each of the 32 message objects can be individually assigned to one of the two CAN nodes. Gateway functionality allows automatic data exchange between two separate CAN bus systems, which reduces CPU load and improves the real time behavior of the entire system.

The bit timings for both CAN nodes are derived from the peripheral clock (f_{CAN}) and are programmable up to a data rate of 1 MBaud. A pair of receive and transmit pins connect each CAN node to a bus transceiver.

PRELIMINARY

Timer Unit (GPTU)

Figure 9 shows a global view of all functional blocks of the GPTU module.

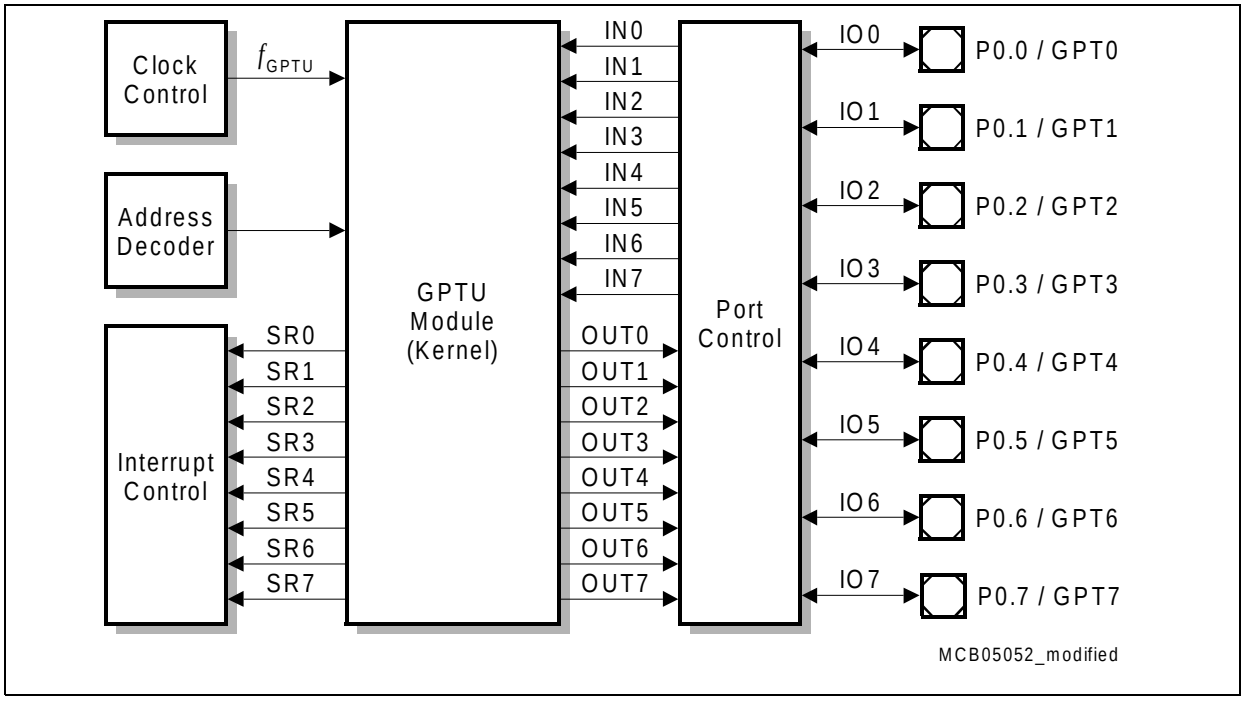


Figure 9 General Block Diagram of the GPTU Interface

The GPTU consists of three 32-bit timers designed to solve such application tasks as event timing, event counting, and event recording. The GPTU communicates with the external world via eight inputs and eight outputs.

The three timers of the GPTU module T0, T1, and T2, can operate independently from each other, or can be combined:

General Features:

- All timers are 32-bit precision timers with a maximum input frequency of $f_{GPTU}/2$.
- Events generated in T0 or T1 can be used to trigger actions in T2
- Timer overflow or underflow in T2 can be used to clock either T0 or T1
- T0 and T1 can be concatenated to form one 64-bit timer

Features of T0 and T1:

- Each timer has a dedicated 32-bit reload register with automatic reload on overflow
- Timers can be split into individual 8-, 16-, or 24-bit timers with individual reload registers
- Overflow signals can be selected to generate service requests, pin output signals, and T2 trigger events
- Two input pins can determine a count option

PRELIMINARY

Features of T2:

- Optionally count up or down
- Operating modes:
  - Timer
  - Counter
  - Incremental Interface Mode
- Options:
  - External start/stop, one-shot operation, timer clear on external event
  - Count direction control through software or an external event
  - Two 32-bit reload/capture registers
- Reload modes:
  - Reload on overflow or underflow
  - Reload on external event: positive transition, negative transition, or both transitions
- Capture modes:
  - Capture on external event: positive transition, negative transition, or both transitions
  - Capture and clear timer on external event: positive transition, negative transition, or both transitions
- Can be split into two 16-bit counter/timers
- Timer count, reload, capture, and trigger functions can be assigned to input pins. T0 and T1 overflow events can also be assigned to these functions.
- Overflow and underflow signals can be used to trigger T0 and/or T1 and to toggle output pins
- T2 events are freely assignable to the service request nodes.

Real Time Clock Unit RTC

The Real Time Clock (RTC) module is basically an independent timer chain and counts clock ticks. The base frequency of the RTC can be programmed via a reload counter. The RTC can work fully asynchronous to the system frequency and is optimized on low power consumption.

Features:

The RTC serves different purposes:

- Absolute system clock to determine the current time and date
- Cyclic time based interrupt
- Alarm interrupt for wake up on a defined time
- 48-bit timer for long term measurements

PRELIMINARY

Codec Interface

The speech A/D and D/A converters (called codec) is designed for telephone and speech recognition quality. They can be used for microphone / earpiece applications. The TC1912 configuration implements a dual channel speech codec connected to the FPI bus.

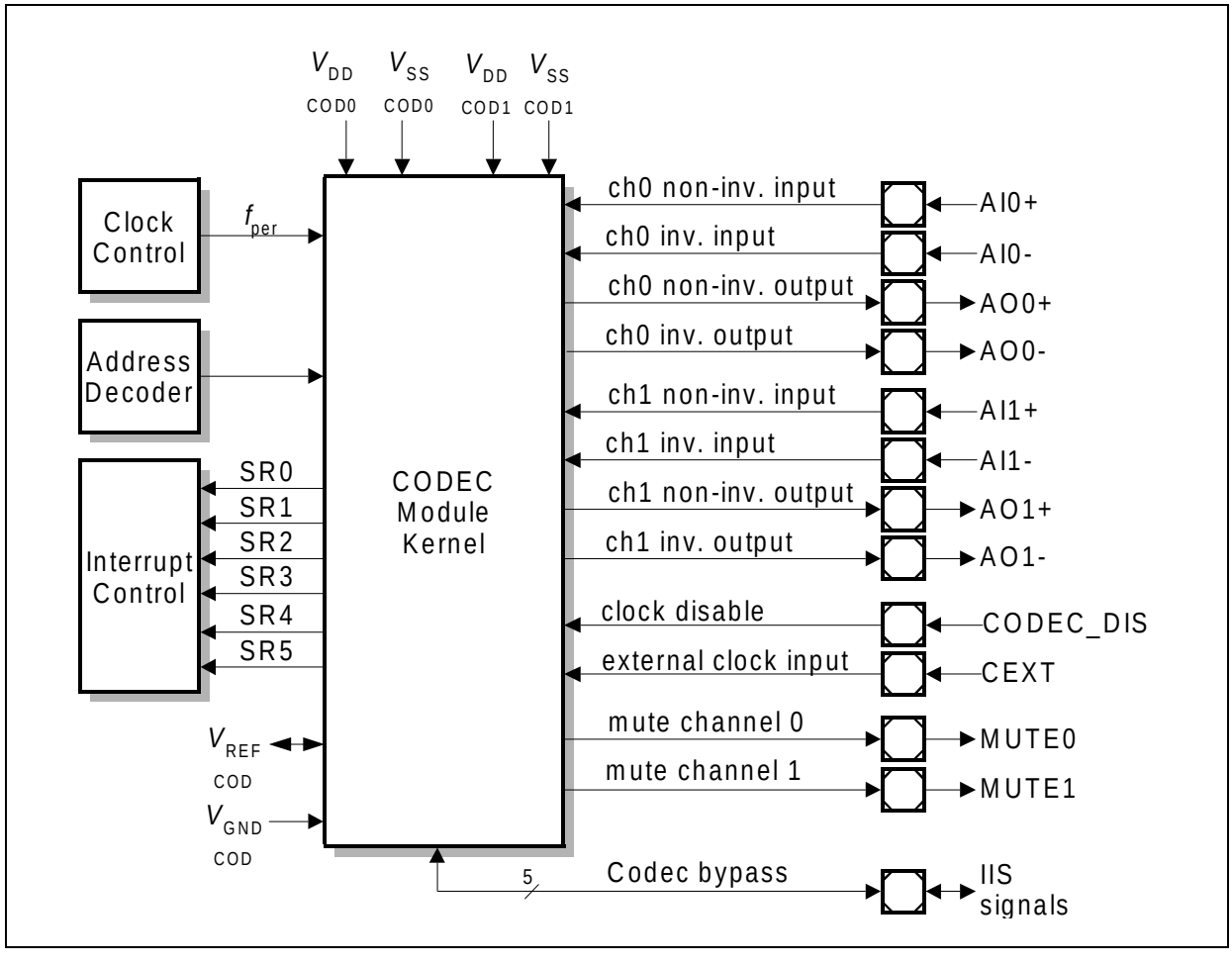


Figure 10 General Codec Overview

General Purpose I/Os (GPIO)

- Push/pull output drivers
- 3.3 Volt operation for GPIO
- Programmable pull-up/-down devices at all pins
- Optional Open Drain Output Mode

PRELIMINARY

ID Register Table

Table 3 List of TC1912 ID registers

Short Name	Description	Address	Reset Value
SCU_ID	SCU Identification Register	F000 0008$_H$	0019 C002$_H$
MANID	Manufacturer Identification Register	F000 0070$_H$	0000 1820$_H$
CHIPID	Chip Identification Register	F000 0074$_H$	0000 8902$_H$
RTID	Redesign Tracing Identification Register	F000 0078$_H$	0000 0000$_H$
RTC_ID	RTC Module Identification Register	F000 0108$_H$	0000 5A04$_H$
BCU_ID	BCU Identification Register	F000 0208$_H$	0000 6A06$_H$
STM_ID	System Timer Module Identification Register	F000 0308$_H$	0000 C002$_H$
JDP_ID	JTAG/OCDS Module Identification Register	F000 0408$_H$	0000 6305$_H$
IIC_ID	IIC Module Identification Register	F000 0508$_H$	0000 4604$_H$
GPTU_ID	GPTU Module Identification Register	F000 0708$_H$	0001 C002$_H$
SSC_ID	SSC Module Identification Register	F000 0808$_H$	0000 4503$_H$
ASC0_ID	ASC Module Identification Register	F000 0A08$_H$	0000 44E1$_H$
ASC1_ID	ASC Module Identification Register	F000 0B08$_H$	0000 44E1$_H$
ASC2_ID	ASC Module Identification Register	F000 0C08$_H$	0000 44E1$_H$
CODEC_ID	Codec Identification Register	F000 2408$_H$	001C C002$_H$
CAN_ID	CAN Module Identification Register	F010 0008$_H$	0000 4110$_H$
CPS_ID	CPU Module Identification Register	F7E0 FF08$_H$	0015 C004$_H$
CPU_ID	CPU Identification Register	F7E1 FE18$_H$	000A C003$_H$
EBU_ID	EBU_LMB Module Identification Register	F800 0008$_H$	0014 C003$_H$
DMU_ID	DMU Identification Register	F87F FC08$_H$	0008 C002$_H$
PMU_ID	PMU Module Identification Register	F87F FD08$_H$	000B C002$_H$
LCU_ID	LCU Identification Register	F87F FE08$_H$	000F C003$_H$
LFI_ID	LFI Identification Register	F87F FF08$_H$	000C C003$_H$

PRELIMINARY

Power Supply

Figure 11 shows the TC1912 power supply concept, where certain logic modules are individually supplied with power. In this way, the noise margin is improved in the especially sensitive modules, like the A/D converter and the CODEC.

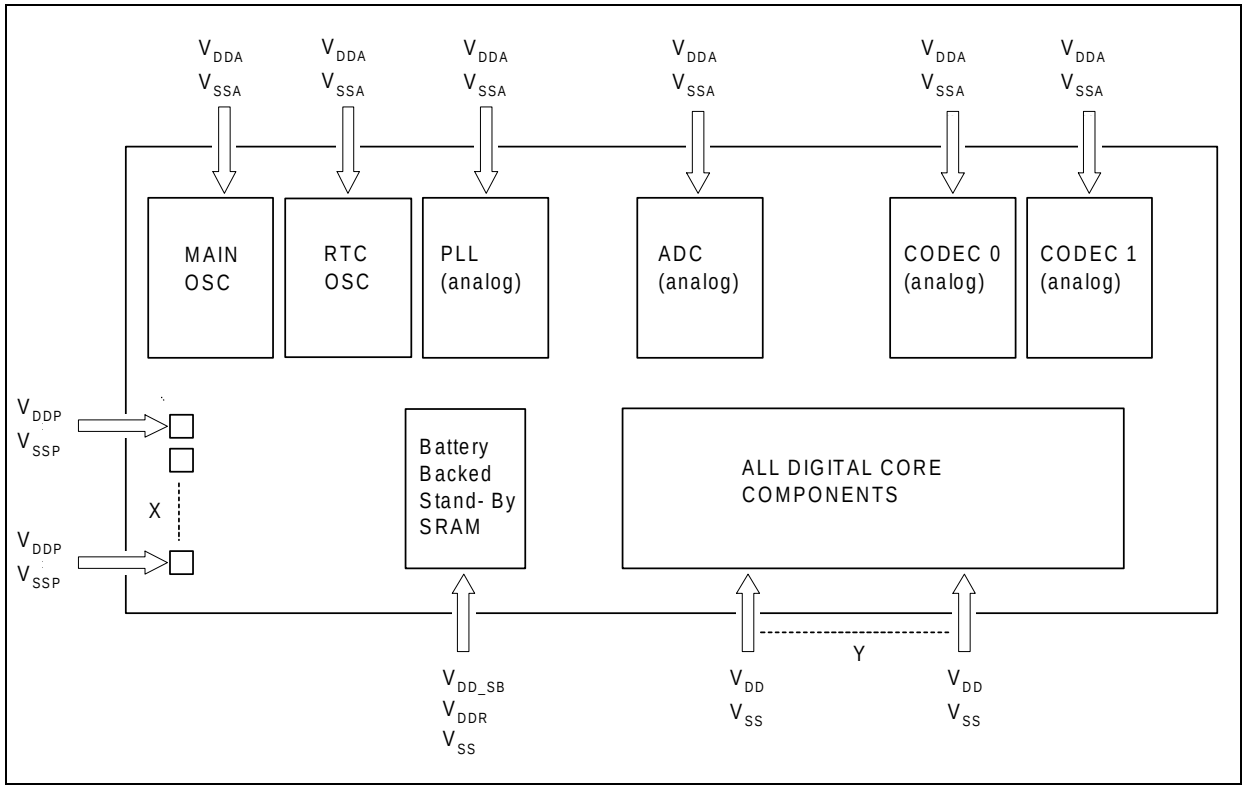


Figure 11 TC1912 Power Supply Concept

PRELIMINARY

Power-Up Sequence

During Power-Up reset pin $\overline{\text{PORST}}$ has to be held active until both power supply voltages have reached at least their minimum values.

During the Power-Up time (rising of the supply voltages from 0 to their regular operating values) it has to be ensured, that the core V_{DD} power supply reaches its operating value first, and then the GPIO V_{DDP} power supply. During the rising time of the core voltage it must be ensured that $0 < V_{DD}-V_{DDP} < 0.5$ V.

During power-down, the core and GPIO power supplies V_{DD} and V_{DDP} respectively, have to be switched off until all capacitances are discharged to zero, before the next power-up.

Note: The states of the pins are undefined when only the port voltage V_{DDP} is on.

PRELIMINARY

Electrical characteristics

Parameter Interpretation

The parameters listed in the following partly represent the characteristics of the TC1912 and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column “Symbol”:

CC (**C**ontroller **C**haracteristics):
The logic of the TC1912 will provide signals with the respective characteristics.

SR (**S**ystem **R**equirement):
The external system must provide signals with the respective characteristics to the TC1912.

PRELIMINARY

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Ambient temperature	T_A	-40	85	°C	under bias
Storage temperature	T_{ST}	-65	150	°C	
Junction temperature	T_J	–	125	°C	under bias
Voltage on I/O Supply pins with respect to ground (V_{SS})	V_{DDP}	-0.5	4.2	V	
Voltage on Core Supply pins with respect to ground (V_{SS})	V_{DD}	-0.3	2.1	V	
Voltage on PLL Supply pins with respect to ground (V_{SS})	V_{DDPLL}	-0.3	2.1	V	PLL
Voltage between Oscillator Supply Pins and ground (V_{SS}).	V_{DDOSC}	-0.3	2.1	V	
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	-0.5	4.2	V	
Input current on any pin during overload condition	I_{OV}	-10	10	mA	
Absolute sum of all input currents at overload condition	ΣI_{OV}	–	|100|	mA	
Power dissipation	P_{DISS}	–	1.0	W	

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
During absolute maximum rating overload conditions (V_{IN}>V_{DD} or V_{IN}<V_{SS}) the voltage on V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

PRELIMINARY

Package Parameters (P-LBGA-208)

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Power dissipation	P_{DISS}	–	1.0	W	–
Thermal resistance	R_{THA}	–	30	K/W	Chip to ambient

Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the TC1912. All parameters specified in the following sections refer to these operating conditions, unless otherwise noted.

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Supply voltage	V_{DDP}	3.0	3.6[1)]	V	I/O supply
	V_{DD}	1.71	1.89[2)]	V	Core supply
	V_{DDPLL}	1.71	1.89	V	PLL supply
	V_{DDOSC}	1.71	1.89	V	Oscillator supply
Ground voltage	V_{SS}	0		V	
Input current on any pin during overload condition	I_{OV}	-5	5	mA	$V_{OV} > V_{DDP}$ + 0.3V $V_{OV} < V_{SS}$ - 0.3V
Absolute sum of all input currents at overload condition	$\Sigma\lvert I_{OV}\rvert$	–	|50|	mA	
Ambient temperature under bias	T_A	-40	85	°C	
CPU clock	f_{CPU}	–	66	MHz	
External Load Capacitance	C_L	–	50	pF	

1) Voltage overshoot to 4 V is permissible, provided the pulse duration is less than 100 µs and the cumulated summary of the pulses does not exceed 1 h

2) Voltage overshoot to 2 V is permissible, provided the pulse duration is less than 100 µs and the cumulated summary of the pulses does not exceed 1 h

PRELIMINARY

DC Characteristics

GPIO pins

Parameter	Symbol	Limit values		Unit	Test Conditions
		min.	max.		
Output low voltage (strong driver)	V_{OL}	-	1 0.4	V	I_{OL} = 10 mA I_{OL} = 2.5 mA
Output high voltage (strong driver)	V_{OH}	2.4	-	V	I_{OH} = - 2.5 mA
Output low voltage (medium driver)[1]	V_{OL}	-	0.4	V	I_{OL} = 1 mA
Output high voltage (medium driver)[1]	V_{OH}	2.4	-	V	I_{OH} = - 1 mA
Output low voltage (weak driver)[1]	V_{OL}	-	0.4	V	I_{OL} = 100 µA
Output high voltage (weak driver)[1]	V_{OH}	2.4	-	V	I_{OH} = - 100 µA
Input low voltage	V_{IL}	-0.3	0.8	V	LVTTL
Input high voltage	V_{IH}	2.0	V_{DDP}+0.3 or 3.7V	V	whatever is lower
Input leakage current	I_{OZ1}	-	±500	nA	0V< V_{in} < V_{DDP}
Pull-up current [2]	$\|I_{PUH}\|$	-	1	µA	V_{OUT} = 2.0V
Pull-up current [3]	$\|I_{PUL}\|$	20	-	µA	V_{OUT} = 0.8V
Pull-down current	$\|I_{PDL}\|$	-	0.8	µA	V_{OUT} = 0.8V
Pull-down current	$\|I_{PDH}\|$	20	-	µA	V_{OUT} = 2.0V
Pin capacitance[1]	C_{IO}	-	10	pF	f = 1MHz @ T_A = 25°C

1) Not subject to production test, verified by design/characterization.

2) The maximum current that may be drawn while the respective signal line remains inactive.

3) The minimum current that must be drawn in order to drive the respective signal line active.

PRELIMINARY

NMI Pin

NMI Pin is an input pin with different Pull-Up characteristics than other pins. The related characteristics are given in the following table

Parameter	Symbol	Limit values		Unit	Test Conditions
		min.	max.		
Max. current allowed through the Pull-Up device while pin (input) voltage remains still at the high level	$\|I_{PUH}\|$	-	4	uA	V_{OUT}=2.0V
Min. current needed through the Pull-Up device so that pin voltage is driven to the low level.	$\|I_{PUL}\|$	100	-	uA	V_{OUT}=0.8V

Note: NMI Pin does not have a Pull-Down device.

Oscillator Pins

Parameter	Symbol	Limit values		Unit	Test Conditions
		min.	max.		
Input leakage current (analog input) at XTAL1[1]	I_{OZ1} CC	-	±200	nA	0V< V_{in} < V_{DDP}
Input low voltage XTAL1	V_{ILX} SR	-	0.3	V	-
Input high voltage XTAL1[2]	V_{IHX} SR	0.8	V_{DD}-0.3 V_{DD}-0.35 V_{DD}-0.4 V_{DD}-0.43	V	f_{OSC}=4MHz f_{OSC}=8MHz f_{OSC}=12MHz f_{OSC}=16MHz
XTAL1 input current	I_{IX1} CC	-	±20	µA	0V < V_{IN} < V_{DD}
XTAL3 input current[2]	I_{IX3} CC	-	±0.5	µA	0V < V_{IN} < V_{DD}

1) Only applicable in deep sleep mode

2) Not subject to production test, verified by design/characterization.

PRELIMINARY

IIC Pins

Each IIC Pin is an open drain output pin with different characteristics than other pins. The related characteristics are given in the following table

Parameter	Symbol	Limit values		Unit	Test Conditions
		min.	max.		
Output low voltage	V_{OL} CC	-	0.4 0.6	V	3 mA 6 mA
Input high voltage[1)]	V_{IH} SR	$0.7V_{DDP}$	3.6	V	-
Input low voltage[1)]	V_{IL} SR	-0.3	$0.3V_{DDP}$	V	-
Input leakage current	I_{OZ2} CC	-	+ - 500	nA	
Pin capacitance[1)]	C_{IO} CC	-	10	pF	f=1MHz@ T_A=25°C

1) Not subject to production test, verified by design/characterization.

Note: No 5 V IIC interface is supported with these pads. Only voltages lower than 3.60 V must be applied to these pads.

Note: IIC pins have no Pull-Up and Pull-Down devices.

PRELIMINARY

Codec Electrical Characteristics

Parameter	Symbol	Limit values			Unit	Test Conditions
		min.	typ.	max.		
Digital supply voltage	V_{DD}	1.71	1.8	1.89	V	
Analog supply voltage	V_{DDA}	3.0	3.3	3.6	V	
Analog supply ground	V_{SSA}	-0.1	0.0	+0.1	V	
External reference voltage	V_{AREF} [1]	1.14	1.2	+1.26 [2]	V	
Analog reference ground	V_{AGND}	V_{SSA}- 0.05	V_{SSA}	V_{SSA}+ 0.05	V	
Analog input voltage (RMS)	V_{AIN}			0.775	V_{rms}	[3]
Analog output voltage (RMS)	V_{AOUT}			0.775	V_{rms}	
Input Resistace of the Analog Inputs [4]	Rain	-	30	-	kOhm	differential input, gain: -12,-6, 0 dB
		-	15	-	kOhm	single-ended input, gain: -12,-6, 0 dB
		-	60	-	kOhm	differential input, gain: 6 to 30 dB
		-	30	-	kOhm	single-ended input, gain: 6 to 30 dB
Internal Reference Voltage Vref (Bandgap Voltage) [5]	V_{BGP}	1.1	1.2	1.3	V	AGCCR. BGPSEL[1,0] =00

1) Reference voltage outside the nominal range causes reduced dynamic range, decreased distortion/clipping margins, increased/decreased gain.

2) $V_{SSA}=V_{AGND}=0V$

3) Please take the gain settings of the analog preamplifier into account, therefore $V_{imaxreal}=V_{imax}$/gain

4) Simulation value.

5) For external usage, Bandgap reference voltage is strongly dependent on the external load (<500 MOhm). In this case, high impedance buffer must be used.

PRELIMINARY

Codec ADC and DAC path characteristics

Parameters	min.	typ.	max.	Unit	Test conditions[1]
Attenuation distortion (ref. freq. 1014 Hz) (ref. level 0dBm0)[2]	0 -0.25 -0.25 -0.25 0		 0.25 0.45	dB dB dB dB dB	< 0.025 0.025-0.0375 0.0375-0.3 0.3-0.425 > 0.425
Signal to total distor-tion		-55	-45	dB	at 0dBm0
Gain tracking (ref. freq. 1014 Hz) (ref. level 0dBm0)[2]	-0.3 -0.6 -1.6		0.3 0.6 1.6	dB dB dB	+3 to -40 dBm0 -40 to -50 dBm0 -50 to -55 dBm0
Idle channel noise		-80	-75	dBm 0	receive &transmit
Cross talk		-80	-75	dB	
Harmonic distortion		-60	-50	dB	at 0dBm0
Gain (ref. freq. 1014 Hz) (ref. level 0dBm0)[2]	-0.8	0	0.8	dB	receive &transmit
Power supply rejection ratio (PSRR)	-	-60 -40	-35 -35	dB dB	Receive (0.0375-0.425)[3] Transmit(0.0375-0.425)[3]

1) Values given in this table are valid for all sampling frequencies.

2) 0dBm0 is equivalent to -12dBm is equal to 194.7 mV_{RMS}.

3) Supply ripple 70 mV.

Note: Numbers without units in the test conditions column are relative frequency values to the chosen sampling frequency. e.g. 0.425 equals 3.4 kHz @ 8 kHz sampling frequency.

PRELIMINARY

Power Supply Current

Parameter	Symbol	Limit values		Unit	Test Conditions
		typ. [1]	max.		
Active mode supply current	I_{DD}	180	–	mA	Sum of all I_{DD}.
Idle mode supply current	I_{ID}	90	–	mA	at 1.8V Core Supply
Deep sleep mode supply current	I_{DS}	0.25	–	mA	at 1.8V Core Supply

1) Typical values are measured at 25°C, CPU clock at 66 MHz and nominal supply voltage, i.e.. 3.3V for V_{DDP} and 1.8V for V_{DD}, V_{DDPLL}, V_{DDOSC}

Note: The Power Supply Current values refer to the total current at 1.8V power supply, at LMB/FPI bus frequency ratio of 2:1, while running an average application. These numbers are estimation based on average device measurements.

PRELIMINARY

AC Characteristics

Operating Conditions apply.

Output Rise/Fall Times

GPIO pins

Rise/fall time measurements are made between 10% and 90%.

The following table is valid for the GPIO pins pad drivers. Output pad characteristics are controllable via DRVCTRx registers.

Pad Modus rise / fall time	Symbol	Limit values		Temp Comp	Unit	Test Conditions
		min.	max.			
Strong driver						
• sharp edge	SF	-	3	yes	ns	@50pF
• medium edge[1)]	SM	-	6	yes	ns	@50pF
• soft edge[1)]	SS	-	12	yes	ns	@50pF

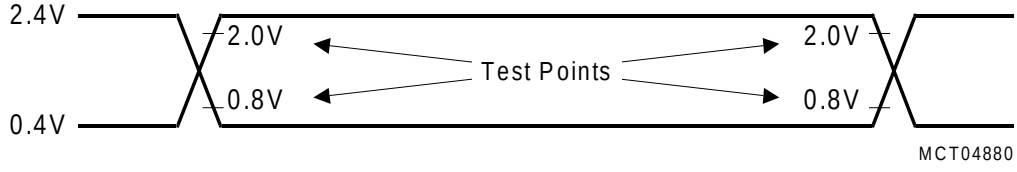
1) Not subject to production test, verified by design/characterization.

PRELIMINARY

Timing Characteristics

(Operating Conditions apply)

Note: Timing parameters are not subject to production test, they are verified by design/characterization.



AC inputs during testing are driven at 2.4V for a logic “1” and 0.4V for a logic “0”. Timing measurements are made at V_{IHmin} for a logic “1” and V_{ILmax} for a logic “0”.

Figure 12 Input/Output Waveforms for AC Tests - for GPIO, Dedicated and EBU pins

PRELIMINARY

External Oscillator at XTAL1 Timing Requirements

(Operating Conditions apply)

Parameter		Symbol	Limits		Unit
			min.	max.	
Main Oscillator XTAL frequency[1]	with/without PLL	f_{OSC} SR	4	16	MHz
Frequency of an external oscillator driving at XTAL1[2]	with PLL[3] without PLL[4]	f_{OSCDD} SR	4 -	25 25	MHz
Input Clock high time		t_1 SR	16	–	ns
Input Clock low time		t_2 SR	16	–	ns
Input Clock rise time		t_3 SR	–	7	ns
Input Clock fall time		t_4 SR	–	7	ns

1) Oscillator Bypass Pin P3.11 latch-in value high. Internal oscillator provides the input clock signal.

2) Oscillator Bypass Pin P3.11 latch-in value low. Internal oscillator disabled. External oscillator provides the input clock signal.

3) Internal PLL provides the system clock. BYPASS pin latch-in value low. PLL prescaler value P=1.

4) Internal PLL bypassed. BYPASS pin latch-in value high. External oscillator provides the system clock directly. When CODEC modules is active its frequency limitations must be taken into consideration. Otherwise, minimum frequency in this mode can go as low as zero.

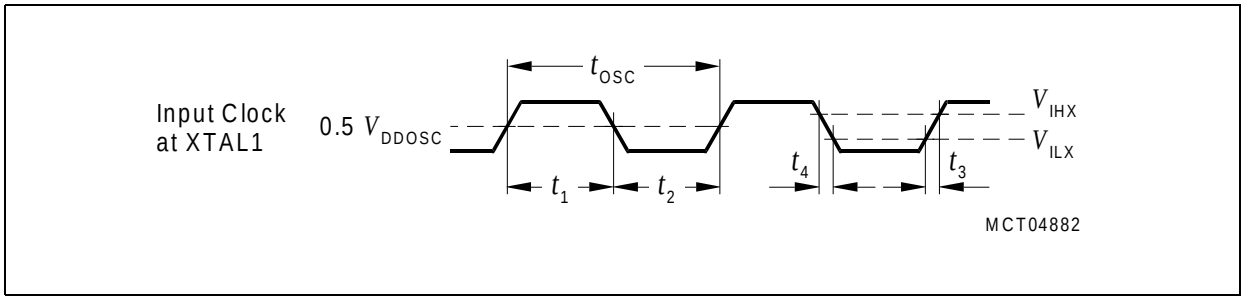


Figure 13 External Clock at XTAL1 Requirements

Note: V_{DDOSC}, V_{IHX} and V_{IHL} are defined in the Oscillator Pins DC Characteristics Chapter.

Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal supplier.

PRELIMINARY

CPU Clock Timing

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol	Limits		Unit
		min.	max.	
CLKOUT period	t_{CLKOUT} CC	15	–	ns
CLKOUT high time	t_1 CC	6	–	ns
CLKOUT low time	t_2 CC	6	–	ns
CLKOUT rise time	t_3 CC	–	3	ns
CLKOUT fall time	t_4 CC	–	3	ns

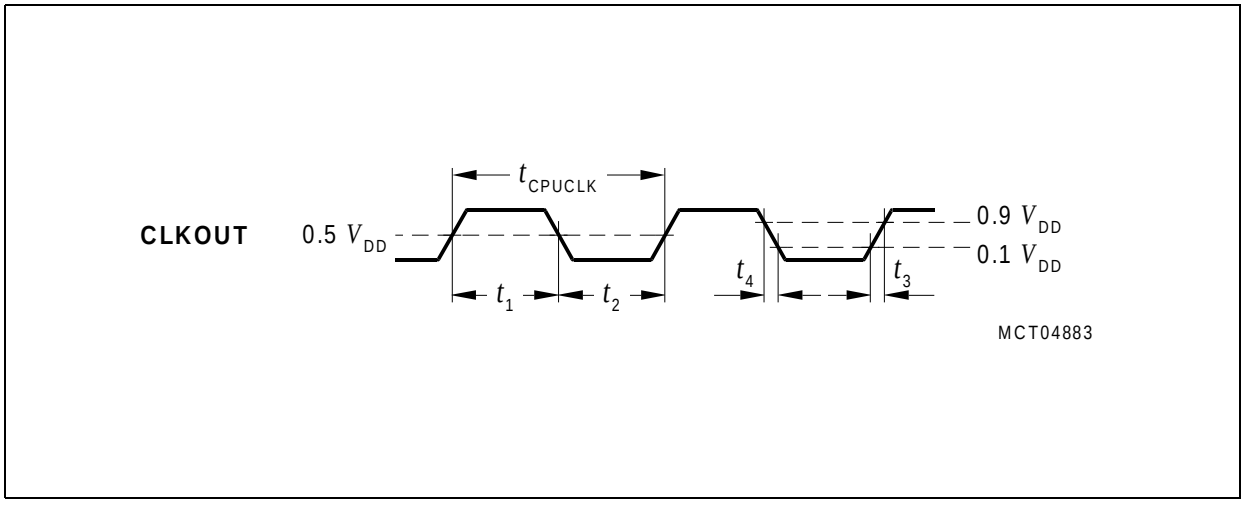


Figure 14 CLKOUT Timing

PRELIMINARY

PLL Parameters

Parameter	Symbol	Limit Values[1]		Unit
		min.	max.	
Accumulated jitter	D_N	see Figure 15		–
VCO frequency range	f_{VCO}	100	150[2]	MHz
		150	200[3]	MHz
		200	250[4]	MHz
		250	300[5]	MHz
PLL base frequency	$f_{PLLBASE}$	20	80[2]	MHz
		20	130[3]	MHz
		20	180[4]	MHz
		20	230[5]	MHz
PLL lock-in time	t_L	–	200	µs

1) Not subject to production test, verified by design/characterization.

2) @ vcosel = ’00’

3) @ vcosel = ’01’

4) @ vcosel = ’10’

5) @ vcosel = ’11’

Note: When TC1912 starts-up with the PLL not bypassed, first user instructions are executed with the frequency defined by the VCO free-running frequency ($f_{PLLBASE}$) and by the reset value of the PLL_CLC register (the K-divider and VCOSEL bitfields). It is software responsibility to initialize its own appropriate values in the bitfields in this register, before giving the command for the VCO to lock to the input frequency. For more information, see the Users Manual, System Units, System Control Unit chapter.

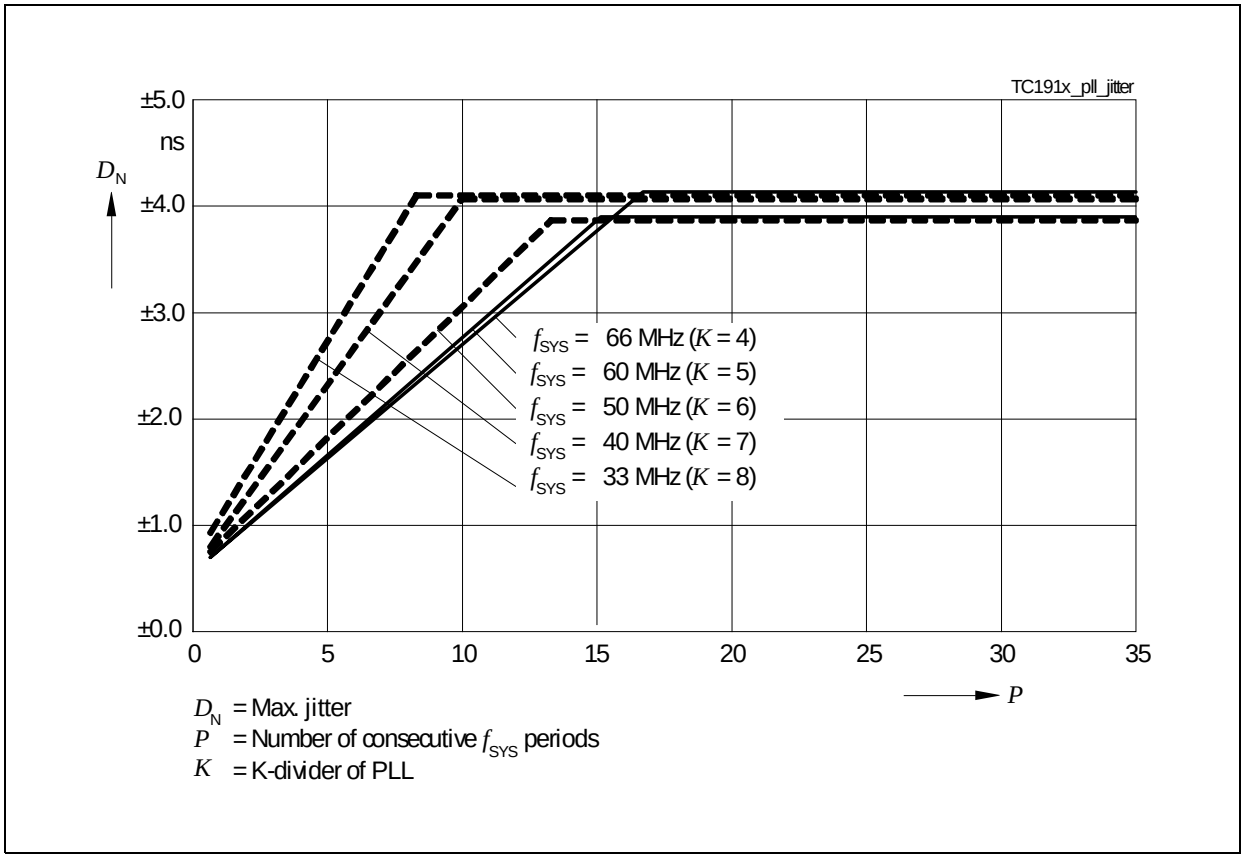


Figure 15 Approximated Maximum Accumulated PLL Jitter

The following two formulas define the (absolute) approximate maximum value of jitter D_N in [ns] dependent on the K-factor, the system clock frequency f_{SYS} in [MHz], and the number P of consecutive f_{SYS} periods.

$$\text{for } P < 0.25 \times f_{SYS} \quad D_N\,[\text{ns}] = \pm\left[\left(\frac{735}{f_{SYS} \times K} + 0.9\right) \times \frac{P}{f_{SYS} \times 0.25} + 0.5\right] \quad [1]$$

$$\text{for } P \geq 0.25 \times f_{SYS} \quad D_N\,[\text{ns}] = \pm\left[\frac{735}{f_{SYS} \times K} + 1.4\right] \quad [2]$$

With rising number P of clock cycles the maximum jitter increases linearly up to a specific value of P. Beyond this value of P the maximum accumulated jitter remains at a constant value.

PRELIMINARY

Timing for EBU_LMB Clock Outputs

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limits		Unit
			min.	max.	
EBUCLK period	t_1	CC	15	–	ns
EBUCLK high time	t_2	CC	6	–	ns
EBUCLK low time	t_3	CC	6	–	ns
EBUCLK rise time	t_4	CC	–	2.5	ns
EBUCLK fall time	t_5	CC	–	2.5	ns
BFCLK0 period	t_6	CC	20	–	ns
BFCLK0 high time	t_7	CC	9	–	ns
BFCLK0 low time	t_8	CC	9	–	ns
BFCLK0 rise time	t_9	CC	–	3.5	ns
BFCLK0 fall time	t_{10}	CC	–	2.5	ns

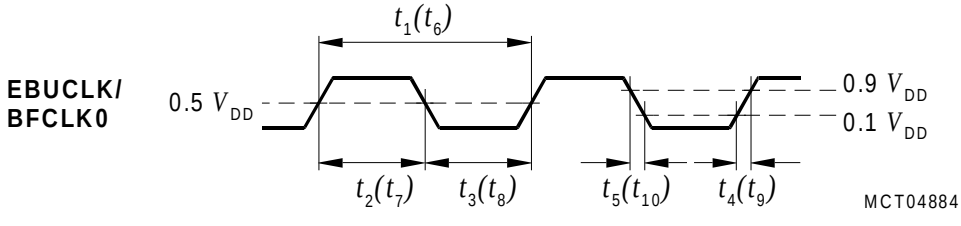


Figure 16 EBU_LMB Clock Output Timing

PRELIMINARY

Timing for SDRAM Access Signals

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limits		Unit
			min.	max.	
CKE high from EBUCLK ↑	t_1	CC	-	7.0	ns
CKE low from EBUCLK ↑	t_2	CC	2.0	-	ns
A(23:0) output valid from EBUCLK ↑	t_3	CC	-	7.0	ns
A(23:0) output hold from EBUCLK ↑	t_4	CC	2.0	-	ns
$\overline{\text{CS}}$(6:0) low from EBUCLK ↑	t_5	CC	-	7.0	ns
$\overline{\text{CS}}$(6:0) high from EBUCLK ↑	t_6	CC	2.0	-	ns
$\overline{\text{RAS}}$ low from EBUCLK ↑	t_7	CC	-	7.0	ns
$\overline{\text{RAS}}$ high from EBUCLK ↑	t_8	CC	2.0	-	ns
$\overline{\text{CAS}}$ low from EBUCLK ↑	t_9	CC	-	7.0	ns
$\overline{\text{CAS}}$ high from EBUCLK ↑	t_{10}	CC	2.0	-	ns
RD/$\overline{\text{WR}}$ low from EBUCLK ↑	t_{11}	CC	-	7.0	ns
RD/$\overline{\text{WR}}$ high from EBUCLK ↑	t_{12}	CC	2.0	-	ns
$\overline{\text{BC}}$(3:0) low from EBUCLK ↑	t_{13}	CC	-	7.0	ns
$\overline{\text{BC}}$(3:0) high from EBUCLK ↑	t_{14}	CC	2.0	-	ns
AD(31:0) output valid from EBUCLK ↑	t_{15}	CC	-	7.7	ns
AD(31:0) output hold from EBUCLK ↑	t_{16}	CC	2.0	-	ns
AD(31:0) input setup to EBUCLK ↑	t_{17}	SR	2.0	-	ns
AD(31:0) input hold from EBUCLK ↑	t_{18}	SR	4.0	-	ns

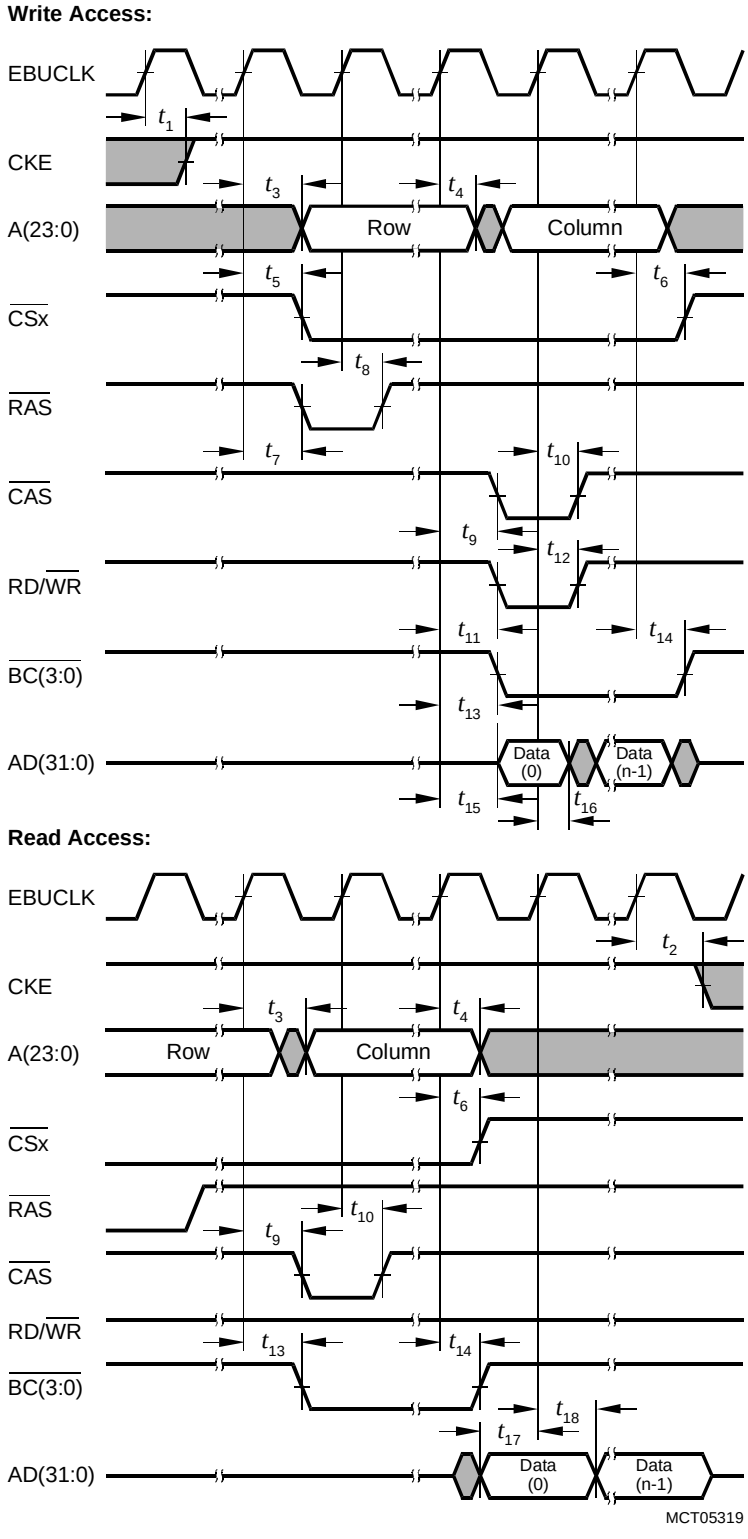


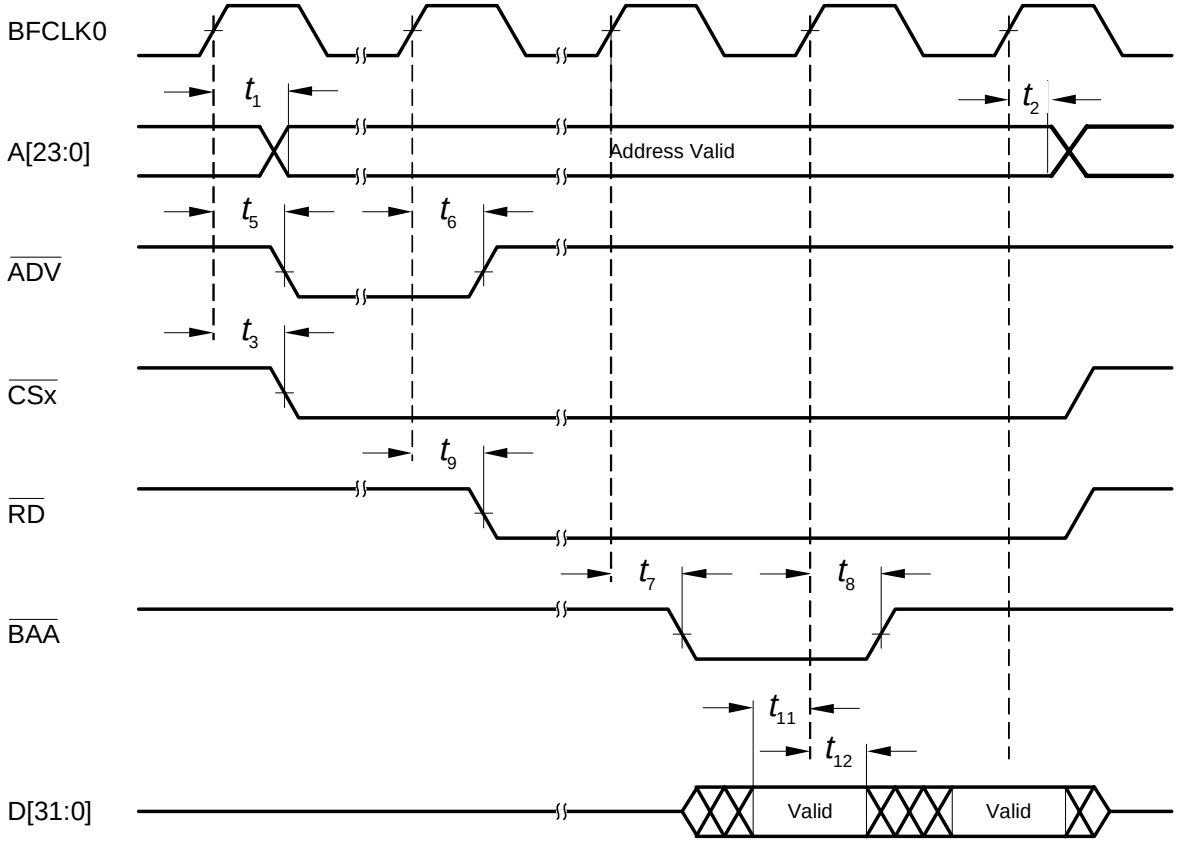
Figure 17 SDRAM Access Timing

PRELIMINARY

Timing for Burst Flash Access Signals

Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limits		Unit
			min.	max.	
A(23:0) output valid from BFCLK0 ↓	t_1	CC	–	11.0	ns
A(23:0) output hold from BFCLK0 ↓	t_2	CC	0.0	–	ns
$\overline{\text{CS}}$(6:0) low from BFCLK0 ↓	t_3	CC	–	9.0	ns
$\overline{\text{ADV}}$ low from BFCLK0 ↓	t_5	CC	–	10.0	ns
$\overline{\text{ADV}}$ high from BFCLK0 ↓	t_6	CC	3.0	–	ns
$\overline{\text{BAA}}$ low from BFCLK0 ↓	t_7	CC	–	10.0	ns
$\overline{\text{BAA}}$ high from BFCLK0 ↓	t_8	CC	3.0	–	ns
$\overline{\text{RD}}$ low from BFCLK0 ↓	t_9	CC	–	10.0	ns
AD(31:0) input setup to BFCLK0 ↓	t_{11}	SR	6.0	–	ns
AD(31:0) input hold from BFCLK0 ↓	t_{12}	SR	3.0	–	ns



Note: Between the end of the Address Phase ($\overline{ADV}$ goes high) and the beginning of the Command Phase ($\overline{RD}$ goes low) several cycles of Command Delay Phase can be inserted.

mct04889_mod_la

Figure 18 Burst Flash Access Timing (Instruction Read)

PRELIMINARY

Timing for Demultiplexed Access Signals[1)]

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limits		Unit
			min.	max.	
ALE low from EBUCLK ↓	t_1	CC	–	8.0	ns
ALE high from EBUCLK ↓	t_2	CC	2.0	–	ns
A(23:0) output valid from EBUCLK ↓	t_3	CC	–	8.0	ns
A(23:0) output hold from EBUCLK ↓	t_4	CC	2.0	–	ns
$\overline{\text{CS}}$(6:0) low from EBUCLK ↓	t_5	CC	–	8.0	ns
$\overline{\text{CS}}$(6:0) high from EBUCLK ↓	t_6	CC	2.0	–	ns
MR/$\overline{\text{W}}$ low from EBUCLK ↓	t_7	CC	–	8.0	ns
MR/$\overline{\text{W}}$ high from EBUCLK ↓	t_8	CC	2.0	–	ns
$\overline{\text{RMW}}$ low from EBUCLK ↓	t_9	CC	–	8.0	ns
$\overline{\text{RMW}}$ high from EBUCLK ↓	t_{10}	CC	1.0	–	ns
$\overline{\text{RD}}$ low from EBUCLK ↓	t_{11}	CC	–	8.0	ns
$\overline{\text{RD}}$ high from EBUCLK ↓	t_{12}	CC	0.0	–	ns
RD/$\overline{\text{WR}}$ low from EBUCLK ↓	t_{13}	CC	–	8.0	ns
RD/$\overline{\text{WR}}$ high from EBUCLK ↓	t_{14}	CC	2.0		ns
$\overline{\text{CMDELAY}}$ input setup to EBUCLK ↓	t_{15}	SR	4.0	–	ns
$\overline{\text{CMDELAY}}$ hold from EBUCLK ↓	t_{16}	SR	3.0	–	ns
$\overline{\text{WAIT}}$ input setup to EBUCLK ↓	t_{17}	SR	4.0	–	ns
$\overline{\text{WAIT}}$ hold from EBUCLK ↓	t_{18}	SR	3.0	–	ns
$\overline{\text{BC}}$(3:0) low from EBUCLK ↓	t_{19}	CC	–	8.0	ns
$\overline{\text{BC}}$(3:0) high from EBUCLK ↓	t_{20}	CC	2.0	–	ns
AD(31:0) output valid from EBUCLK ↓	t_{21}	CC	–	8.0	ns
AD(31:0) output hold from EBUCLK ↓	t_{22}	CC	0.0	–	ns
AD(31:0) input setup to EBUCLK ↓	t_{23}	SR	4.0	–	ns
AD(31:0) input hold from EBUCLK ↓	t_{24}	SR	4.0	–	ns

1) It is user responsibility to program an appropriate whole number of clock cycles to generate the correct phase length according to the particular asynchronous memory/peripheral device specification.

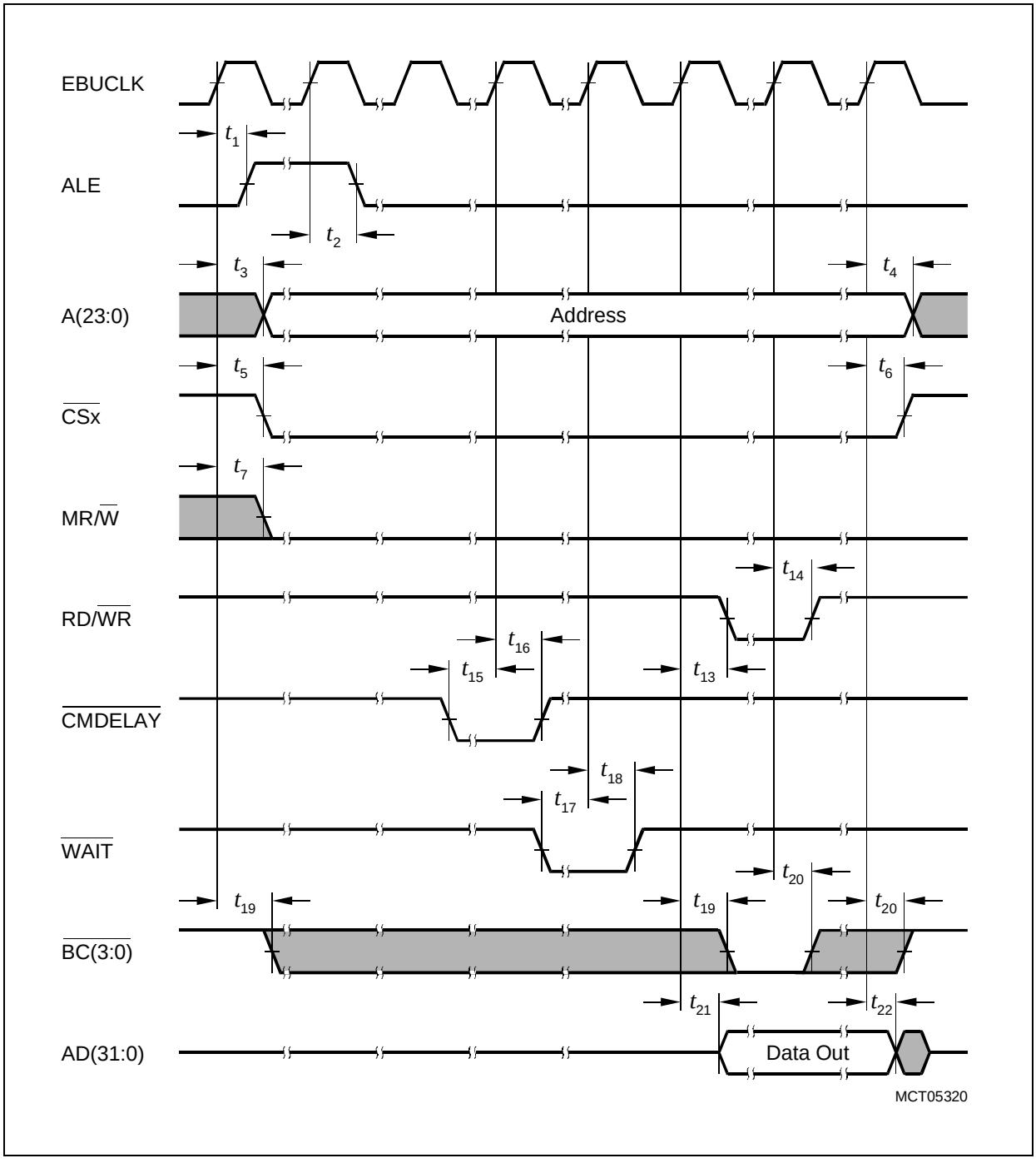


Figure 19 Demultiplexed Write Access

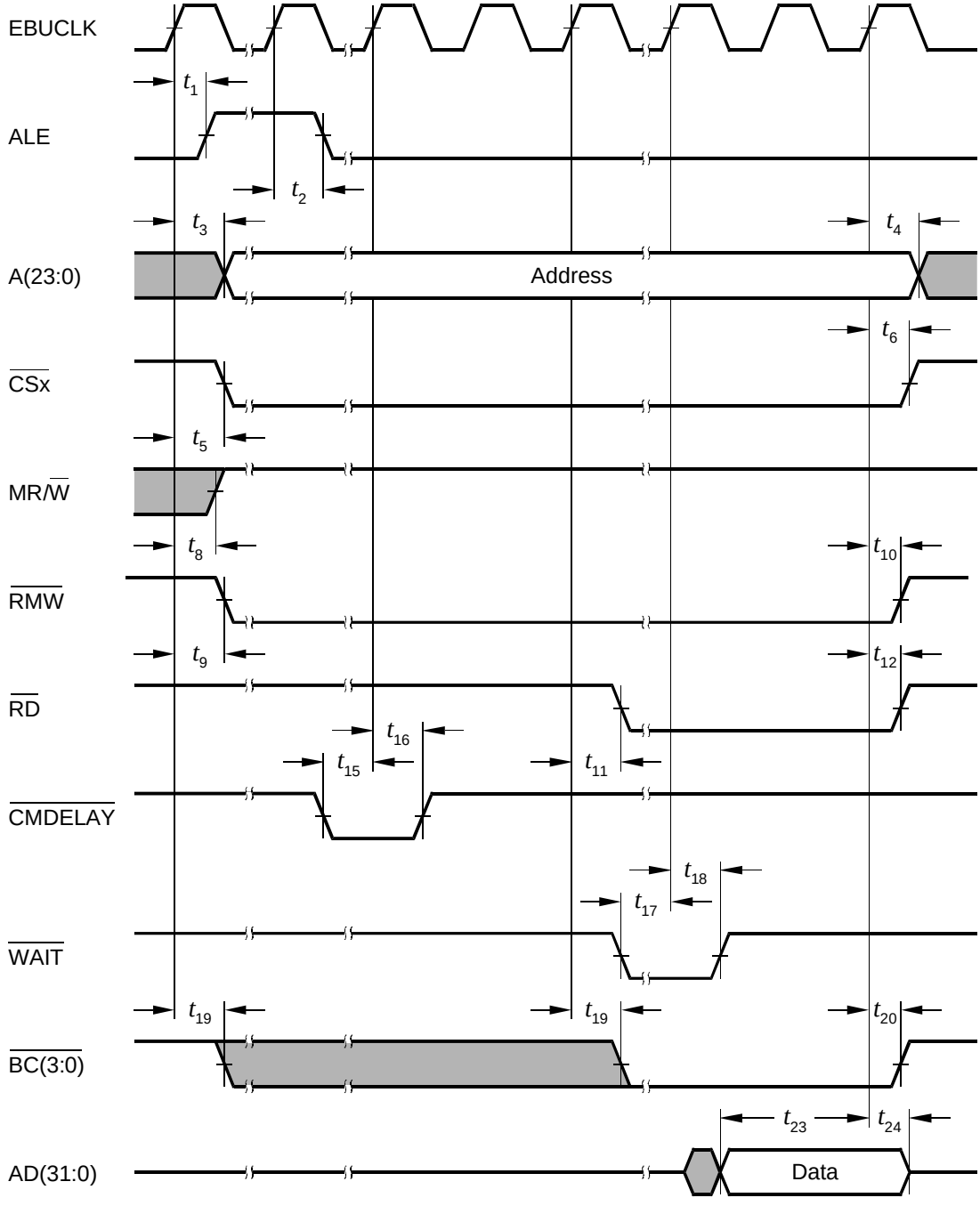


Figure 20 Demultiplexed Read Access

PRELIMINARY

Timing for Multiplexed Access Signals[1)]

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limits		Unit
			min.	max.	
ALE high from EBUCLK ↑	t_1	CC	–	8.0	ns
ALE low from EBUCLK ↑	t_2	CC	2.0	–	ns
AD(31:0) output valid from EBUCLK ↑	t_3	CC	–	8.0	ns
AD(31:0) output hold from EBUCLK ↑	t_4	CC	0.0	–	ns
AD(31:0) input setup to EBUCLK ↑	t_5	SR	4.0	–	ns
AD(31:0) input hold from EBUCLK ↑	t_6	SR	4.0	–	ns
$\overline{\text{CS}}$(6:0) low from EBUCLK ↑	t_7	CC	–	8.0	ns
$\overline{\text{CS}}$(6:0) high from EBUCLK ↑	t_8	CC	1.0	–	ns
MR/$\overline{\text{W}}$ low from EBUCLK ↑	t_9	CC	–	8.0	ns
MR/$\overline{\text{W}}$ high from EBUCLK ↑	t_{10}	CC	2.0	–	ns
$\overline{\text{RMW}}$ low from EBUCLK ↑	t_{11}	CC	–	8.0	ns
$\overline{\text{RMW}}$ high from EBUCLK ↑	t_{12}	CC	1.0	–	ns
RD/$\overline{\text{WR}}$ low from EBUCLK ↑	t_{13}	CC	–	8.0	ns
RD/$\overline{\text{WR}}$ high from EBUCLK ↑	t_{14}	CC	2.0	–	ns
$\overline{\text{RD}}$ low from EBUCLK ↑	t_{15}	CC	–	8.0	ns
$\overline{\text{RD}}$ high from EBUCLK ↑	t_{16}	CC	0.0	–	ns
$\overline{\text{CMDELAY}}$ input setup to EBUCLK ↑	t_{17}	SR	4.0	–	ns
$\overline{\text{CMDELAY}}$ hold from EBUCLK ↑	t_{18}	SR	3.0	–	ns
$\overline{\text{WAIT}}$ input setup to EBUCLK ↑	t_{19}	SR	4.0	–	ns
$\overline{\text{WAIT}}$ hold from EBUCLK ↑	t_{20}	SR	3.0	–	ns
$\overline{\text{BC}}$(3:0) low from EBUCLK ↑	t_{21}	CC	–	8.0	ns
$\overline{\text{BC}}$(3:0) high from EBUCLK ↑	t_{22}	CC	2.0	–	ns

1) It is user responsibility to program an appropriate whole number of clock cycles to generate the correct phase length according to the particular asynchronous memory/peripheral device specification.

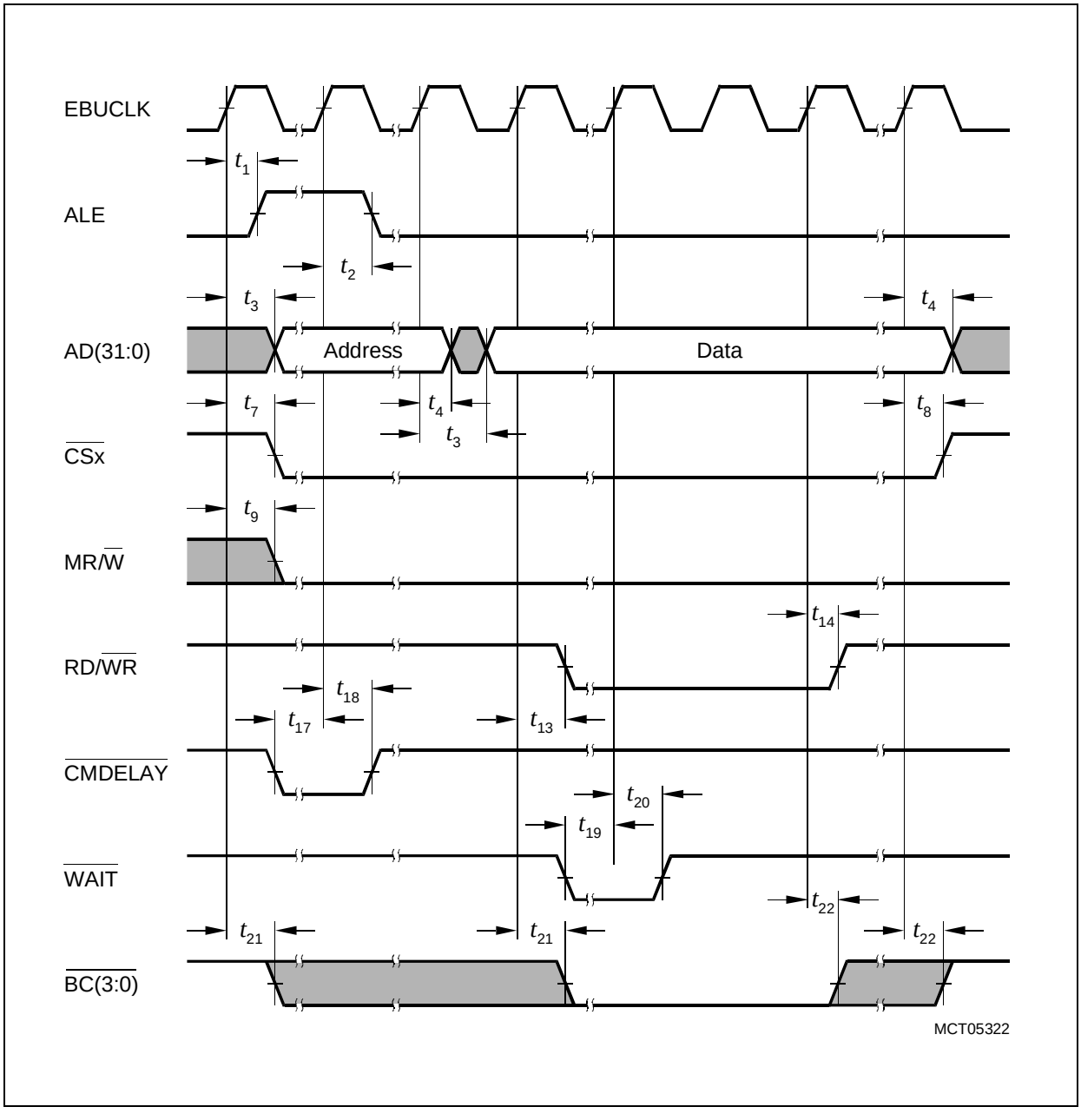
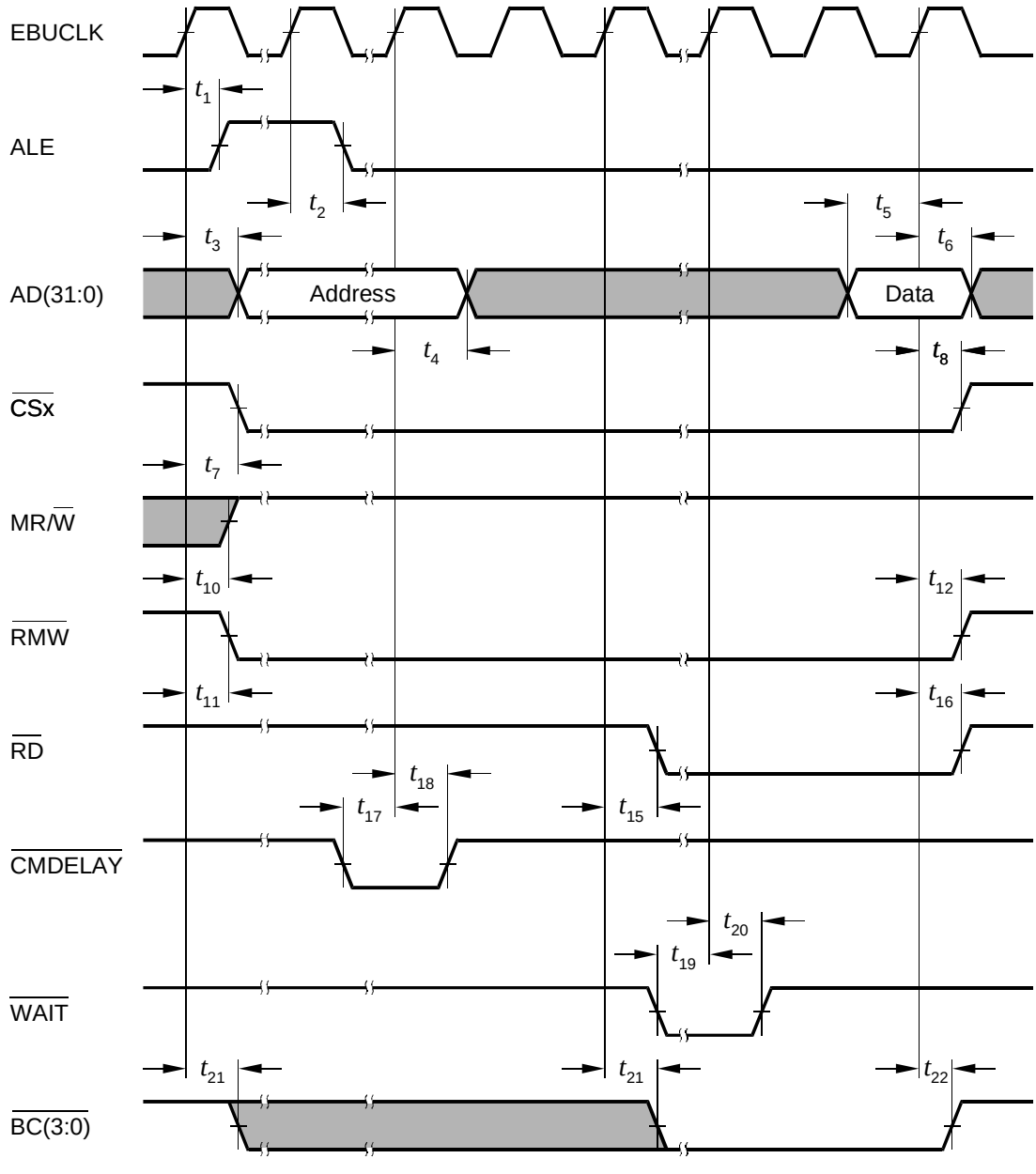


Figure 21 Multiplexed Write Access



Note: RMW signal is only available during Read-Modify-Write Access.

Figure 22 Multiplexed Read Access

PRELIMINARY

Timing for External Bus Arbitration Signals

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limits		Unit
			min.	max.	
$\overline{\text{HOLD}}$ input setup to EBUCLK ↓	t_1	SR	6.0	–	ns
$\overline{\text{HOLD}}$ input hold from EBUCLK ↓	t_2	SR	8.0	–	ns
$\overline{\text{HLDA}}$ low from EBUCLK ↓	t_3	CC	–	10.0	ns
$\overline{\text{HLDA}}$ high from EBUCLK ↓	t_4	CC	–	9.0	ns
$\overline{\text{HLDA}}$ input setup to EBUCLK ↓	t_5	SR	8.0	–	ns
$\overline{\text{HLDA}}$ input hold from EBUCLK ↓	t_6	SR	8.0	–	ns
$\overline{\text{BREQ}}$ low from EBUCLK ↓	t_7	CC	–	10.0	ns
$\overline{\text{BREQ}}$ high from EBUCLK ↓	t_8	CC	–	9.0	ns

Note: The signals $\overline{\text{HOLD}}$, $\overline{\text{HLDA}}$ and $\overline{\text{BREQ}}$ are alternate function of the $\overline{\text{CS5}}$, $\overline{\text{CS6}}$ and $\overline{\text{CSOVL}}$ Pins.

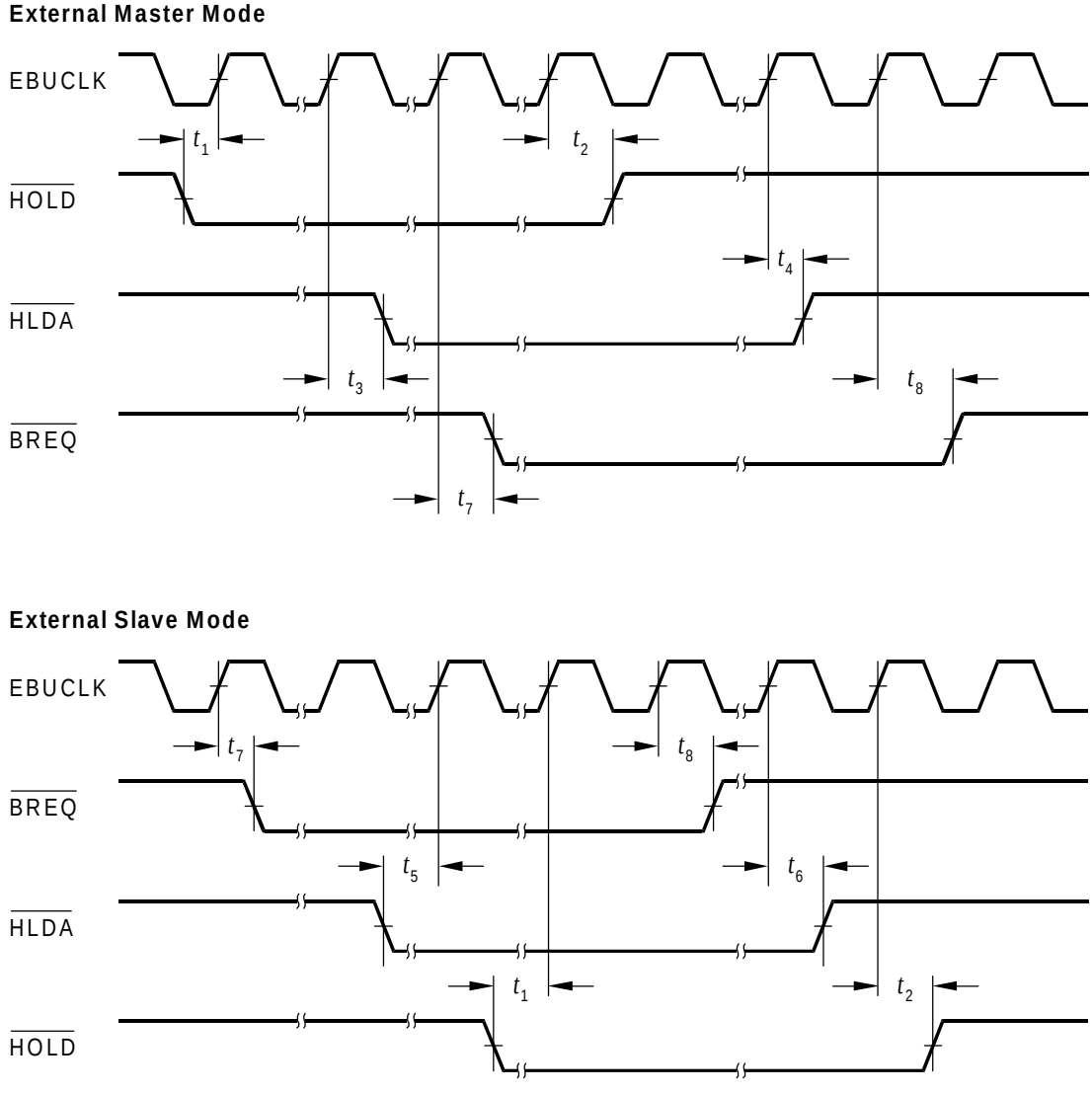


Figure 23 External Bus Arbitration Timing

PRELIMINARY

SSC Master Mode Timing

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limit Values		Unit
			min.	max.	
SCLK period	t_{SCLK}	CC	40		ns
MTSR low/high from SCLK edge	t_5	CC	-	2.0	ns
MRST setup to SCLK edge	t_6	SR	15	-	ns
MRST hold from SCLK edge	t_7	SR	15	-	ns

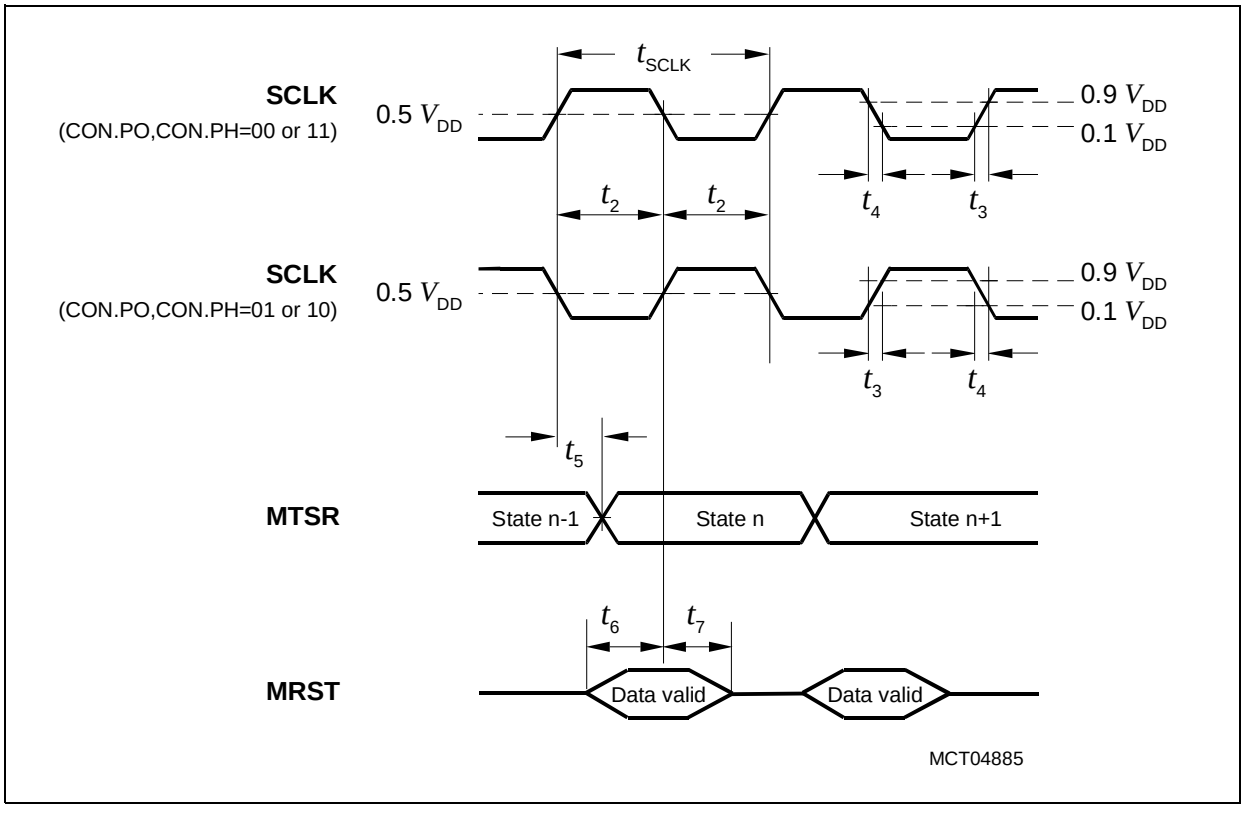


Figure 24 SSC Master Mode Timing

PRELIMINARY

Package Outlines

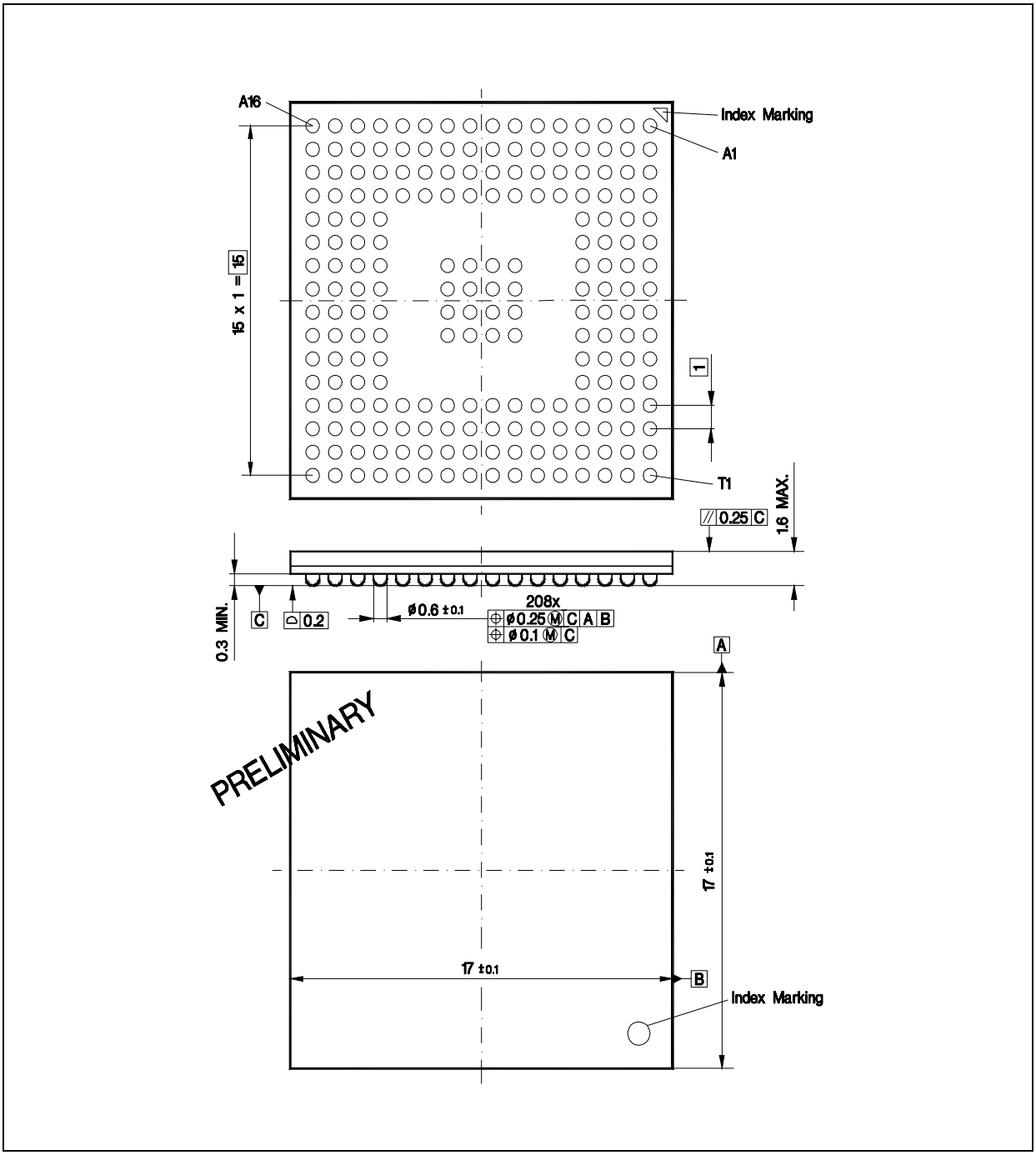


Figure 25 P-LBGA-208 Package

You can find all of our packages, sorts of packing and other in our Infineon Internet Page “Products”: http://www.infineon.com/products

PRELIMINARY

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