National Semiconductor Corporation

PRELIMINARY

microCMOS

TP3330 Monolithic Full Duplex 1200/600/300 BPS Bell 212A/V.22 Modem

General Description

The TP3330 is a single chip full duplex 1200/600/300 BPS voiceband modem that operates over two wire voice-grade phone lines. It is compatible with Bell 212A, Bell 103/113 (1200/300 BPS) and CCITT V.22 A,B (1200/600 BPS) modem standards. All modulation, demodulation and filtering functions are performed on-chip.

The TP3330 contains an on-chip USART that performs serial-to-parallel and parallel-to-serial conversions on data characters. It can be connected directly to the host processor or controller through a standard microprocessor bus. The device provides status information on error conditions (parity, overrun, framing and break detect) as well as modem status conditions to the CPU. Also included on-chip is a full prioritized interrupt system which reduces software overhead in the CPU. When operating in asynchronous mode, it is functionally equivalent to the INS8250A UART.

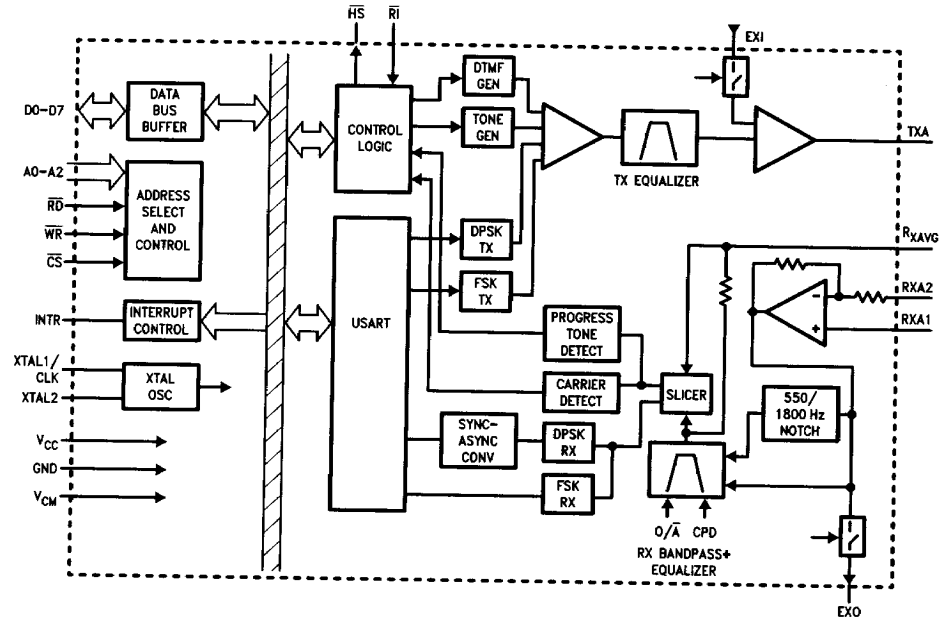
Additional functions on the device are an on-chip DTMF generator and call progress tone detector to facilitate auto-dialing. Hook-switch control output and an interrupt input for Ring Detect are provided to facilitate auto-answering. Interfacing to the phone line is simplified by the on-chip hybrid circuit.

The TP3330 is implemented with National's advanced dual-metal silicon gate microCMOS process. The device operates from a single +5V supply, and is ideal for portable or battery operated systems.

Features

- Bell 212A and Bell 103/113 compatible
- CCITT V.22 A,B compatible
- On-chip USART with full prioritized interrupt system
- Synchronous transmission: 1200/600 BPS
- Asynchronous transmission: 1200/600/300 BPS
- Hybrid and line driver with switched audio access
- DTMF generator
- Call progress tone detection
- Loopback test modes
- +5V only single supply operation
- LSTTL and CMOS compatible logic

Block Diagram



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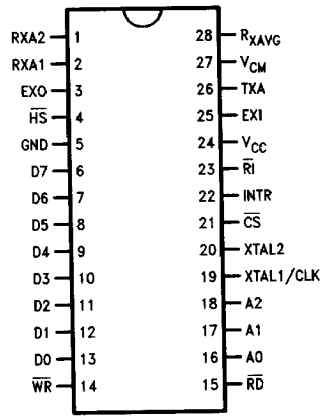
Connection Diagrams

Dual-In-Line Package



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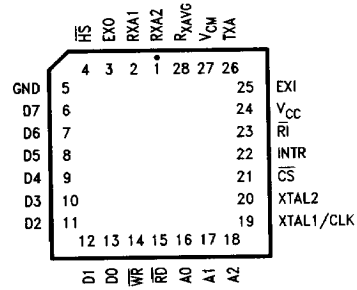
Top View

Order Number TP3330N
See NS Package Number N28B
Plastic Chip Carrier (PCC)



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Top View

Order Number TP3330V
See NS Package Number V28A

Pin Descriptions

Pin Number	Name	Function
21	$\overline{CS}$	**Chip Select:** When $\overline{CS}$ is low, the device is selected, enabling communication between the TP3330 and the CPU. When $\overline{CS}$ is high, the Data Bus is in TRI-STATE, $\overline{RD}$ and $\overline{WR}$ will have no effect on the device.
15	$\overline{RD}$	**Read Strobe:** With $\overline{CS}$ low, a logic low at $\overline{RD}$ input allows the CPU to read data or status information from the TP3330.
14	$\overline{WR}$	**Write Strobe:** With $\overline{CS}$ low, a logic low at $\overline{WR}$ input allows the CPU to write data or control words into the TP3330.
16–18	A0, A1, A2	**Register Select:** These 3 inputs are the address selects to a particular internal register of the TP3330 to read from or write to during a read or write operation. A0 is the LSB.
6–13	D7–D0	**Data Bus:** This data bus is comprised of 8 TRI-STATE input/output lines. The bus provides bidirectional communications between the CPU and the TP3330. Data, control words and status information are transferred via this bus. D0 is the LSB and D7 is the MSB. Serial data on the line is LSB first.
22	INTR	**Interrupt Output:** This line goes high whenever any one of the interrupt types has an active high condition and is enabled via the Interrupt Enable Register. The INTR output is TRI-STATE when Bit 3 of MCR2 is set to logic 0.
19	XTAL1/ CLK	This is the input of the on-chip oscillator circuit which requires an external 4.91520 MHz crystal. It can also be used as the input for an external 4.91520 MHz clock signal.
20	XTAL2	This is the output of the on-chip oscillator high gain inverter.
24	V_{CC}	Positive power supply pin. The supply voltage is $+5V \pm 5\%$ referenced to GND. A 0.1 μF bypass capacitor is required to be connected from V_{CC} to GND.
5	GND	**Ground:** All digital signals are referenced to this pin.
27	V_{CM}	**Analog Common Mode:** This pin is biased to $\frac{1}{2}$ V_{CC} by an internal resistor divider and must be AC bypassed by an external 100 μF electrolytic and a 0.1 μF ceramic capacitor. All analog signals are referenced to this pin.
26	TXA	Transmit analog output of the line driver amplifier.
2, 1	RXA1, RXA2	**Receive Analog Inputs:** RXA1 and RXA2 are analog high impedance inputs to the receiver buffer amplifier. When connected as recommended, they produce a 600Ω hybrid circuit.

Pin Descriptions (Continued)

Pin Number	Name	Function
25	EXI	**External Audio Input:** This is a high impedance input to the line driver amplifier which can be used to transmit an externally generated tone or voice. The EXI input is switched on or off by Bit 5 of the Handshaking Control Register. The input signal from EXI is not filtered by the Transmit filter, and should be less than 1 Vp-p in order to prevent output clipping. When not used, it should be connected to V_{CM}.
3	EXO	**External Audio Output:** This is a buffered audio output of the receiver, capable of driving a 10 kΩ load. The EXO output is switched on or off by Bit 4 of the Handshaking Control Register.
28	R_{XAVG}	This is the comparator input of the internal slicer circuit. An external 0.01 μF capacitor must be connected from this pin to V_{CM}.
4	$\overline{HS}$	**Hook Switch Output:** This logical latched output may be used to drive an external relay driver for hook-switch control. It is programmed by Bit 7 of the Dialing Control Register. A logic high at Bit 7 will set the $\overline{HS}$ output to logic low level.
23	$\overline{RI}$	**Ring Indicator:** A logical low at this input indicates the presence of ringing signal received by an external ring detector. The CPU can monitor the $\overline{RI}$ input by reading Bit 6 of the Modem Status Register 2. Whenever the $\overline{RI}$ input changes from a low to high state, an interrupt is generated if the Modem Status Interrupt is enabled.

Functional Description

POWER-UP INITIALIZATION

When power is first applied, the internal power-on reset circuitry initializes the TP3330. Internal registers (except the Receive Buffer, Transmitter Holding and Sync-character Registers) are reset to their initial conditions. The state of the output signals are also set to their inactive conditions. (Refer to Table I.) A Master Reset can be generated by setting Bit 2 of the Modem Control Register 2.

TRANSMITTER

The transmitter section consists of a digital modulator and spectrum controller, a switched capacitor transmit equalizer, a post filter, and a line driver amplifier. At 1200/600 BPS, the modulator is a DPSK (Differential Phase Shift-Keyed) modulator with a scrambler circuit that prevents loss of synchronization. At 300 BPS, the modulator is a phase-coherent FSK (Frequency Shift-Keyed) modulator. Data information from the CPU is converted into a phase modulated or a frequency modulated sine wave that can be transmitted over the switched telephone network.

Half-channel fixed compromised equalization is provided by the transmit equalizer, which also attenuates any unwanted frequency components, so that the out-of-band emission is within the limits of FCC and CCITT specifications. *Figure 1* shows the out-of-band energy relative to the transmit carrier.

The line driver is a low distortion power amplifier that outputs the transmit carrier or the DTMF signal and is able to drive a −9 dBm signal into a 600Ω line. When the modem is not transmitting data or DTMF signals, externally generated tones or voice can be transmitted to the line from the EXI input. It is enabled by setting Bit 5 of the Handshaking Control Register. When not used, this input should be connected to V_{CM}.

Table II shows the frequency assignments of the Transmit Carrier.

TABLE I. Reset Functions

Register/Signals	Reset State
Interrupt Enable Register	All Bits Low
Interrupt Identification Register	Bit 0 is High, Bits 1–7 are Low
Line Control Register 1	All Bits Low
Modem Control Register 2	All Bits Low
Line Status Register	All Bits Low, Except Bits 5 & 6 which are High
Modem Status Register 2	All Bits Low, Except Bit 6 which is an input
Line Control Register 2	All Bits Low
Modem Control Register 1	All Bits Low
Dialing Control Register	All Bits Low
Handshaking Control Register	All Bits Low
Modem Status Register 1	All Bits Low
Test Mode Register	All Bits Low
INTR	Low
$\overline{HS}$	High

Functional Description (Continued)

TABLE II. Transmit Carrier Frequency Assignment

Standard	Data Rate		Nominal Carrier Frequency (Hz)	Actual Carrier Frequency (Hz)	% Deviation from Nominal
Bell 212A	300 BPS Originating	Mark	1270	1265.625	−0.34
		Space	1070	1068.750	−0.12
	300 BPS Answering	Mark	2225	2221.875	−0.14
		Space	2025	2025	0
	1200 BPS Low Band		1200	1200	0
	1200 BPS High Band		2400	2400	0
	Answer Tone		2225	2221.875	−0.14
CCITT V.22	600/1200 BPS Low Band		1200	1200	0
	600/1200 BPS High Band		2400	2400	0
	Answer Tone		2100	2100	0
	Guard Tone		550	553.125	+0.57
			1800	1800	0

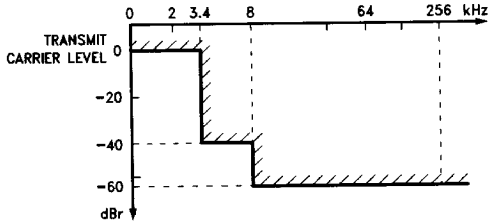

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FIGURE 1. Out-of-Band Energy Relative to Transmit Carrier

RECEIVER

The receiver consists of a 2-to-4 wire hybrid amplifier, an anti-alias filter, a switched capacitor receive bandpass filter and a low distortion digital demodulator. When connected as recommended, the input buffer amplifier performs as a 2-to-4 wire converter, canceling the transmitted signal from the incoming received signal.

An audio output is provided at EXO for audio monitoring of the received signals from the line. It can be used to drive an external power amplifier, such as the LM386, for audio monitoring of call progress. It is enabled by setting Bit 4 of the Handshaking Control Register.

The receive filter is a 22-pole switched capacitor bandpass filter which can be programmed to operate in the low band or high band channel. It rejects out-of-band transmission, noise components and the undesirable adjacent channel echo signals which can be fed from the transmitter section to the receiver section over the 2-wire phone line. For CCITT V.22 operation, a programmable 550 Hz or 1800 Hz notch filter is also included to reject the guard tone that is transmitted along with the high band carrier. A half channel amplitude and group delay equalizer is also included to ensure low bit error rate and low bit length distortion when connected to any voice grade phone line.

At 1200/600 BPS, the demodulator is a DPSK demodulator with a phase-locked loop clock recovery circuit. The received data is descrambled using the inverse of the transmit scrambler polynomial. In the asynchronous mode, the sync-to-async converter re-inserts the stop bit deleted by the transmitting modem. At 300 BPS, the demodulator is a FSK demodulator.

CARRIER DETECTOR

The carrier detector monitors the level of the receive signal. To prevent transmission of erroneous data to the CPU, the receive data output from the demodulator is clamped to logic high when the carrier falls below the receive threshold level for a time greater than $t_{CD\ OFF}$. Whenever the receive signal is above the threshold level for a time greater than $t_{CD\ ON}$, Bit 7 in the Modem Status Register 2 (CD) is set to logic 1, indicating the presence of valid carrier, and the demodulator output is enabled.

When the Call Progress Tone Detector is enabled, the sampling clock frequency of the receive bandpass filter is scaled down by 2.5 times, so that it covers the passband (350 Hz to 620 Hz) of the precise call progress tones. CD ON indicates the presence of tones, while CD OFF indicates the absence of tones. Such a cadence is easily monitored by the CPU, which can discriminate between the types of call progress tones as shown in the following table:

Dial Tone	350 Hz + 440 Hz	Continuous
Busy Tone	480 Hz + 620 Hz	0.5s ON /0.5s OFF
Re-Order Tone	480 Hz + 620 Hz	0.25s ON /0.25s OFF
Ringback Tone from Central Office:	440 Hz + 480 Hz	2s ON /4s OFF
from PBX:	440 Hz + 480 Hz	1s ON /3s OFF

The Modem Answer Tone is detected by the Answer Tone Detector, which is reflected by Bit 1 of the Modem Status Register 2.

DTMF GENERATOR

An on-chip DTMF generator facilitates auto-dialing. It accepts BCD input from the CPU, and is able to generate all 16 standard DTMF tone pairs. With DTMF ENABLE (Bit 4 of the Dialing Control Register) set to logic high, a 4-bit binary number previously loaded into locations Bits 0–3 is decoded and sets the high group and low group programmable counters to the appropriate divider ratios. The output voltage at TXA is the sum of the high and low group sine waves superimposed on a DC level of approximately ½ V_{CC}. The modulator and EXI are disabled, and the gain of the receive buffer amplifier is reduced by 20 dB in order to prevent overloading the receive filter section.

Table III shows the output tone frequencies, and Table IV is the functional truth table.

Functional Description (Continued)

TABLE III. DTMF Output Frequency Accuracy

Tone Group	Standard DTMF Frequency (Hz)	Tone Output Frequency (Hz)	% Deviation
Low Group f_L	697	693.750	−0.47
	770	768.750	−0.16
	852	853.125	+0.13
	941	937.500	−0.37
High Group f_H	1209	1209.375	+0.03
	1336	1340.625	+0.35
	1477	1481.250	+0.29
	1633	1631.250	−0.11

TABLE IV. Functional Truth Table for DTMF Dialing

Keyboard Equivalence	BCD Inputs				DTMF Enable Bit 4	DTMF Output	
	Bit 3	Bit 2	Bit 1	Bit 0		f_L(Hz)	f_H(Hz)
x	x	x	x	x	0	0	0
1	0	0	0	1	1	697	1209
2	0	0	1	0	1	697	1336
3	0	0	1	1	1	697	1477
4	0	1	0	0	1	770	1209
5	0	1	0	1	1	770	1336
6	0	1	1	0	1	770	1477
7	0	1	1	1	1	852	1209
8	1	0	0	0	1	852	1336
9	1	0	0	1	1	852	1477
0	1	0	1	0	1	941	1336
*	1	0	1	1	1	941	1209
#	1	1	0	0	1	941	1477
A	1	1	0	1	1	697	1633
B	1	1	1	0	1	770	1633
C	1	1	1	1	1	852	1633
D	0	0	0	0	1	941	1633

TEST MODES

The TP3330 provides several test modes to allow the user or the CPU to verify that the modem is operating properly.

Analog Loopback

In the Analog Loopback mode, the receive bandpass filter and demodulator are configured to process the same channel as the transmitter. The transmitted carrier output is looped back to the receiver input via an internal attenuator, while still maintaining the modulated carrier to the output pin TXA.

Digital Loopback

When the Digital Loopback mode is enabled, the digital output of the demodulator is looped back to the digital input of the modulator. At 1200/600 BPS, the recovered clock of the receiver is also looped back internally to the transmit clock. The serial data input to the receive shift register of the USART is clamped to logic high, and the transmit data from the USART is ignored.

Remote Digital Loopback

The TP3330 supports Remote Digital Loopback by providing the Dotting Pattern detector for the originator. A Dotting Pattern Generator and an unscramble mark detector are provided for the remote modem for the handshaking process.

USART Digital Loopback

This test mode allows the user to test the USART's functions and interrupt system independently of the rest of the circuit. In this test mode, the serial data output from the transmit shift register is looped internally to the serial data input of the receive shift register. The data input from the demodulator is ignored. The four modem control bits (RTS, DTR, OUT1 and OUT2) are internally connected to the four modem status bits (CTS, DSR, RI and CD).

Functional Description (Continued)

USART

The on-chip USART performs serial-to-parallel conversion on data characters received from the line and parallel-to-serial conversion on data characters received from the CPU. Status information on error conditions (parity, overrun, framing or break interrupt) is provided to the CPU at any time during the functional operation. In asynchronous transmission, the USART is functionally equivalent to National's INS8250A UART, providing start-stop framing to the data. In synchronous transmission, the programmable synchronous characters are transmitted at the beginning or during data transmission in order to achieve synchronization.

ACCESSIBLE REGISTERS

The operation of TP3330 is programmable via the internal accessible registers. Table V summarizes those registers which are used to control and monitor the modem's operation. The registers listed in Table VI are used to control the USART's operations in data transfer and monitor the error conditions.

Modem Control Register 1

This register specifies the general operating conditions for the TP3330.

Bit 0: In combination with Bit 1, this bit selects the data rate of transmission.

Bit 1	Bit 0	Data Rate
0	0	1200 BPS DPSK
0	1	300 BPS FSK
1	0	1200 BPS DPSK
1	1	600 BPS DPSK

Bit 1: A logic low selects the Bell 212A and logic high selects the CCITT V.22 modem standard. The answer tone is automatically set to 2225 Hz for Bell 212A, and 2100 Hz for V.22.

Bits 2, 3: These 2 bits specify the threshold level for the carrier detector and call progress tone detector.

Bit 3	Bit 2	Carrier ON Threshold (dBm)	Carrier OFF Threshold (dBm)
0	0	−43	−46
0	1	−38	−41
1	0	−33	−36
1	1	−33	−36

Bits 4, 5: These 2 bits specify the nominal transmit carrier amplitude and DTMF levels at the TXA output.

Bit 5	Bit 4	Carrier (mVrms)	DTMF V_L/V_H (mVrms)
0	0	550	615/775
0	1	435	490/615
1	0	345	390/490
1	1	275	310/390

Bit 6: This bit selects the guard tone frequency to be transmitted along with the DPSK high band carrier when TP3330 is operating at V.22 mode. A logic low selects 1800 Hz, and a logic high selects 550 Hz.

Bit 7: A logic 0 for this bit selects the Asynchronous transmission with start-stop bits. A logic 1 selects the Synchronous transmission mode. At 300 BPS, this bit is ignored and transmission is always in Asynchronous mode only.

Dialing Control Register

This register controls the operation of TP3330 in the DTMF dialing mode.

Bits 0–3: These bits specify a 4 bit BCD digit defined in Table IV. The di it is decoded to generate the corresponding DTMF tone pair.

TABLE V. Summary of Modem Registers

AL3	1	1	1	1	1
A0–A2	0	1	2	2	3
	Modem Control Register 1	Dialing Control Register	Handshake Control Register (Write Only)	Modem Status Register 1 (Read Only)	Test Mode Register
Bit	MCR1	DCR	HCR	MSR1	TMR
0	LOW/$\overline{\text{HIGH}}$ Speed	DTMF No Bit 0	Transmit Output Enable	Receive Speed Indicator $\overline{1200}$/300 BPS	Power Up Enable
1	$\overline{\text{Bell 212A}}$/ V.22	DTMF No Bit 1	Transmit Scrambler Enable	2225 Hz/High Band Unscrambled Mark Detect	ALB Enable
2	Carrier Threshold Select	DTMF No Bit 2	Guard Tone Enable	Scrambled Mark Detect	DLB Enable
3	Carrier Threshold Select	DTMF No Bit 3	Answer Tone Enable	Low Band Unscrambled Mark Detect	0
4	Level Adjust	DTMF Enable	EXO Enable	Dotting Pattern Detect	0
5	Level Adjust	Enable Call Progress Tone Detect	EXI Enable	0	0
6	Guard Tone Select	Receive Mute Enable	ORIG/$\overline{\text{ANS}}$ Mode Select	0	0
7	$\overline{\text{ASYNC}}$/ SYNC Select	Hook Switch Control	Dotting Pattern Enable	0	0

TABLE VI. Summary of USART Registers

AL3	0	0	0	0	0	X	0	0	0	1	1	1
A0–2	0 DLAB = 0	0 DLAB = 0	1 DLAB = 0	2	3	4	5	6	7	5	6	7
	Receive Buffer Register (Read Only)	Transmit Holding Register (Write Only)	Interrupt Enable Register	Interrupt Identification Register (Read Only)	Line Control Register 1	Modem Control Register 2	Line Status Register	Modem Status Register 2	Scratch Pad Register	Line Control Register 2	Sync Character Register 1	Sync Character Register 2
Bit	RBR	THR	IER	IIR	LCR 1	MCR2	LSR	MSR2	SCR	LCR2	SYNC1	SYNC2
0	Data Bit 0	Data Bit 0	Enable Receive Data Ready Interrupt	0 If Interrupt Pending	Word Length Bit 0	Data Terminal Ready (DTR)	Receive Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Transmit Enable	Bit 0	Bit 0
1	Data Bit 1	Data Bit 1	Enable Transmit Holding Register Empty Interrupt	Interrupt ID Bit 0	Word Length Bit 1	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Receive Enable	Bit 1	Bit 1
2	Data Bit 2	Data Bit 2	Enable Line Status Interrupt	Interrupt ID Bit 1	Stop Bit Select (ASYNC Mode)	OUT 1 (Reset)	Parity Error (PE)	Trailing Edge of Ring Indicator (TERI)	Bit 2	Sync Character Select	Bit 2	Bit 2
3	Data Bit 3	Data Bit 3	Enable Modem Status Interrupt	Interrupt ID Bit 2	Parity Enable	OUT 2 (INTR Output Enable)	Framing Error (FE)	Delta Carrier Detect (DCD)	Bit 3	Int/Ext Syndet Select	Bit 3	Bit 3
4	Data Bit 4	Data Bit 4	0	0	Even Parity	Loop	Break Interrupt (ASYNC)/ SYNDET (SYNC)	Clear to Send (CTS)	Bit 4	Ext Syndet Input	Bit 4	Bit 4
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	THRE Empty	Data Set Ready (DSR)	Bit 5	Enter Hunt	Bit 5	Bit 5
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	TEMT	Ring Indicator (RI)	Bit 6	Slave Timing Enable	Bit 6	Bit 6
7	Data Bit 7	Data Bit 7	0	0	DLAB	AL3	0	Carrier Detect (CD)	Bit 7	0	Bit 7	Bit 7

Note: Bit 0 is the least significant bit.

It is the first bit serially transmitted or received.

Functional Description (Continued)

Bit 4: When this bit is set to logic 1, the DTMF generator is enabled.

Bit 5: When set to logic 1, the Call Progress Tone Detector is enabled. Bit 7 (CD) of Modem Status Register 2 indicates the presence (logic 1) or absence (logic 0) of call progress tones within the passband of 350 Hz to 620 Hz. After ringback tone is detected by the CPU, Bit 5 should be reset to logic 0, putting the TP3330 in normal data mode.

Bit 6: A logic high for this bit mutes the receiver buffer amplifier. Muting is useful during pulse dialing to prevent transient overloading of the receiver.

Bit 7: This bit controls the $\overline{HS}$ output signal for hookswitch control, and can be used for pulse dialthrough by setting and resetting this bit with the right timing. The following table shows the timing requirement for pulse dialing in North America.

Pulsing Rate	8 to 11	pps
Percentage Break	58 to 64	%
Inter-Digital Pause	0.6 to 1	Sec

Handshaking Control Register

This register controls the handshaking process of the TP3330.

Bit 0: A logic high enables the transmission of carrier or DTMF signals at the TXA output. A logic low will set TXA at the V_{CM} voltage.

Bit 1: When this bit is set to logic 1, it enables the scrambler circuit inserted in the data path for the DPSK modulator. Setting this bit low bypasses the scrambler.

Bit 2: A logic high enables the transmission of the guard tone frequency selected by Bit 6 of the Modem Control Register 1. The carrier amplitude is automatically reduced by about 1 dB in order to maintain the same total transmitted power output.

Bit 3: A logic high enables the transmission of the modem answer tone, which is 2225 Hz for Bell 212A, or 2100 Hz for V.22.

Bit 4: A logic high enables the receiver audio output at EXO. When disabled by a logic low, the EXO output is set to V_{CM} voltage.

Bit 5: A logic high enables the external audio input at EXI to the line driver amplifier.

Bit 6: A logic high selects the originating mode. The TP3330 transmits at the low band and receives at the high band frequency. A logic low selects the answer mode, transmitting at the high band and receiving at the low band frequency.

Bit 7: A logic high enables the transmission of the Dotting Pattern (scrambled alternating one's and zero's) for the handshaking process required to initialize a Remote Digital Loopback for 600 BPS or 1200 BPS. Bit 1 must also be set to logic 1 to enable the transmitter's scrambler.

Modem Status Register 1

This register provides status information regarding the incoming received signal from the phone line. When the Modem Status Interrupt is enabled, the low to high transition of the status bits in this register will generate an interrupt output at INTR. It is reset by a read operation on the Modem Status Register 1.

Bit 0: This status bit is the received data speed indicator for the Bell 212A answering mode only. A logic low indicates receiving at 1200 BPS, while a logic high indicates receiving at 300 BPS. Bit 0 is reset to logic 0 whenever CD (Bit 7 of MSR2) changes from logic 1 to logic 0.

Bit 1: This bit is the answer tone indicator. It goes high whenever a 2225 Hz answer tone or high band unscrambled mark has been received for more than 160 ms during handshaking.

Bit 2: This bit is the DPSK scrambled mark indicator. It goes high whenever a scrambled mark is received for 267 ms. (t_{SM})

Bit 3: This bit is the Low band DPSK unscrambled mark indicator. It goes high when an unscrambled mark is detected for more than 160 ms.

Bit 4: This bit is the Dotting Pattern indicator. It goes high whenever a pattern of DPSK scrambled alternating 1's and 0's are received for 267 ms, indicating that a Remote Digital Loopback is being acknowledged by the far end modem.

Bits 5,6,7: These bits are not used.

Note: Bits 1 to 4 are reset to logic 0 whenever the CPU reads the content of the Modem Status Register 1.

Test Mode Register

This register programs the modes of operation of the TP3330.

Bit 0: When this bit is programmed to logic low, the TP3330 is put in the power-down mode, minimizing current consumption. All non-essential circuits are de-activated, analog outputs TXA and EXO are TRI-STATE and the digital output $\overline{HS}$ is at inactive state. The internal registers are unaffected, and the $\overline{RI}$ input and its associate interrupt function as normal. When power is first applied to TP3330, the user should program a logic high in Bit 0 to set the device in the power-up mode.

Bit 1: A logic high enables the Analog Loopback test mode.

Bit 2: A logic high enables the Digital Loopback test mode.

Bits 3–7: These bits are not used, and should be set to logic 0.

Functional Description (Continued)

Line Control Register 1

The Line Control Register 1 specifies the format of asynchronous data communication. The programmer may retrieve the contents of both Line Control Registers for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory.

Bits 0,1: These 2 bits specify the number of data bits in each transmitted or received serial character. In the asynchronous mode for 1200 BPS/600 BPS, the sync-to-async converter allows 8, 9, 10, or 11 character length (start bit + data bits + parity bit + stop bits), the selections for word length, parity bit and stop bits must be matched to these requirements. Table VII shows the valid combinations for character lengths.

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of stop bits in each transmitted character for asynchronous communication. If Bit 2 is a logic 0, one stop bit is generated in the transmitted data. If Bit 2 is a logic 1 when a 5-bit word length is selected via Bits 0 and 1, one and a half stop bits are generated. If Bit 2 is a logic 1 when either a 6-, 7- or 8-bit word length is selected, two stop bits are generated. The receiver checks the first stop bit only, regardless of the number of stop bits selected.

Bit 3: This is the Parity Enable bit. When Bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and stop bit of the serial data.

Bit 4: This is the Even Parity Select bit. When Parity is enabled via Bit 3, a logic 0 at Bit 4 selects the Odd Parity and a logic 1 selects the Even Parity.

Bit 5: This is the Stick Parity select bit. When Parity is enabled via Bit 3, a logic 1 at Bit 5 enables the Stick Parity. If Bit 4 is a logic 1, the Parity bit is transmitted and checked by the receiver as a logic 0. If Bit 4 is a logic 0, then the Parity bit is transmitted as a logic 1.

Bit 6: This is the Break Control bit. When it is set to a logic 1, the serial output of the USART is forced to the Spacing (logic 0) state. The break is disabled by resetting bit 6 to a logic 0.

Note: To prevent any erroneous characters being transmitted because of the break, the following sequence is recommended:

1. Load an all 0's pad character in response to THRE.
2. Set break after the next THRE.
3. Wait for the transmitter to be idle (TEMT = 1) and clear break when normal transmission has been restored.

Bit 7: This bit is the Access Bit (DLAB). It must be set to logic 0 to access the Receiver Buffer Register, the Transmitter Holding Register, or the Interrupt Enable Register.

Line Control Register 2

The Line Control Register 2 specifies the format of Synchronous transmission.

Bit 0: A logic 1 enables the transmitter of the USART. Data begins to shift serially into the modulator circuit. A logic 0 disables the transmitter of the USART, and the serial data input to the modulator is clamped at logic high. When disabled while the modem is in operation, all the data that was previously loaded into the USART will be transmitted before the USART is shut down.

Bit 1: A logic high enables the receiver of the USART.

Bit 2: A logic low at this input selects double synchronization characters to be transmitted or received. A logic high selects single synchronization character.

Bit 3: A logic high at this input selects the external sync-detect mode. A logic low selects the internal sync-detect mode.

Bit 4: This bit is the External Sync-detect Input. When external sync-detect mode is selected via Bit 3, synchronization is achieved by applying a logic high at Bit 4, which forces the USART to exit the Hunt mode and start assembling serial data into the parallel format.

Bit 5: When Bit 5 is set to logic high, the Hunt mode is enabled. If internal sync-detect mode is programmed by Bit 3, the received data in the buffer register is compared at each bit boundary with the first sync character until a match is found. If the USART is programmed for double sync characters, the subsequent character is also compared. If both sync characters are detected, the USART exits the Hunt mode and is in synchronization.

Bit 6: A logic high selects the Slave Timing mode for Synchronous Transmission. The transmit clock is phase-locked to the recovery clock of the DPSK demodulator.

Bit 7: This bit is always at logic 0.

Sync-Character Registers 1,2

Bits 0–7: These registers are used to store the programmable synchronization characters for insertion at the beginning of, or during the transmission of synchronous messages. If the CPU does not respond to the TEMT and the USART is programmed for single sync-character, the content of Sync-Character Register 1 will be transmitted before the normal data transmission resumes. If dual sync-characters are being programmed, the contents of both Sync-Character Registers 1 and 2 will be transmitted.

Functional Description (Continued)

TABLE VII. Asynchronous Character Formats for 600/1200 BPS

Bit 2	Bit 3	Bit 1	Bit 0	Character Length (Bits)								
				Start	+	Data	+	Parity	+	Stop		
0	0	0	1	1	+	6	+	0	+	1	=	8
0	0	1	0	1	+	7	+	0	+	1	=	9
0	0	1	1	1	+	8	+	0	+	1	=	10
0	1	0	0	1	+	5	+	1	+	1	=	8
0	1	0	1	1	+	6	+	1	+	1	=	9
0	1	1	0	1	+	7	+	1	+	1	=	10
0	1	1	1	1	+	8	+	1	+	1	=	11
1	0	0	1	1	+	6	+	0	+	2	=	9
1	0	1	0	1	+	7	+	0	+	2	=	10
1	0	1	1	1	+	8	+	0	+	2	=	11
1	1	0	1	1	+	6	+	1	+	2	=	10
1	1	1	0	1	+	7	+	1	+	2	=	11

Line Status Register

The Line Status Register provides status information to the CPU concerning the data transfer. It is intended for read operation only, writing to this register is not recommended.

Bit 0: This is the Receive Data Ready (DR) indicator. It is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receive Buffer Register. Bit 0 is reset to a logic 0 by reading the data in the Receive Buffer Register.

Bit 1: This is the Overrun Error (OE) indicator. A logic 1 at Bit 1 indicates that data in the Receive Buffer Register was not read by the CPU before the next character was transferred into the Receive Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This is the Parity Error (PE) indicator. Bit 2 is set to a logic 1 whenever the received data character does not have the correct even or odd parity, as selected by the parity select bit. It is reset to logic 0 whenever the CPU reads the contents of the Line Status Register.

Bit 3: This is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid stop bit. It is set to a logic 1 whenever the stop bit following the last data bit or parity bit is at the spacing level. Bit 3 is reset whenever the CPU reads the contents of the Line Status Register.

Bit 4: When asynchronous transmission is selected, this bit is the Break Interrupt (BI) indicator. It is set to a logic 1 whenever the received data input is held in the spacing (logic 0) state for longer than a full word transmission time (that is, the total time of start bit + data bits + parity + stop bits). When Synchronous transmission is selected, this bit is the sync-detect indicator. It is set to logic 1 whenever the USART detects a valid sync-character (or two consecutive sync-characters when in dual sync mode). Bit 4 is reset whenever the CPU reads the contents of the Line Status Register.

Note: Bits 1 through 4 are the error conditions that produce a receiver Line Status Interrupt whenever any of the corresponding conditions is detected.

Bit 5: This is the Transmitter Holding Register Empty (THRE) indicator. It is set to logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register, indicating that the USART is ready to accept a new character for transmission. It also issues an interrupt to the CPU if the Transmitter Holding Register Empty Interrupt is enabled. Bit 5 is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

Bit 6: This is the Transmitter Empty (TEMT) indicator. It is set to a logic 1 whenever the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. It is reset to logic 0 whenever either the THR or TSR contains a data character.

Bit 7: This bit is permanently set to logic 0.

Interrupt Enable Register

This register enables the 4 types of interrupts to separately activate the Interrupt (INTR) output signal. The interrupt system can be totally disabled by resetting bits 0 through 3 of the Interrupt Enable Register. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTR output from the device. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers. The interrupt output signal can be put into TRI-STATE by resetting Bit 3 of the Modem Control Register 2 to logic 0.

Bit 0: A logic 1 enables the Received Data Available Interrupt.

Bit 1: A logic 1 enables the Transmitter Holding Register Empty Interrupt.

Bit 2: A logic 1 enables the Line Status Interrupt.

Bit 3: A logic 1 enables the Modem Status Interrupt (Interrupt sourced from either Modem Status Register 1 or 2).

Bits 4–7: These four bits are always at logic 0.

Interrupt Identification Register

Information indicating that a prioritized interrupt is pending and the type of that interrupt is stored in the Interrupt Identification Register (IIR). In order to provide minimum software

Functional Description (Continued)

overhead during data transfer, the TP3330 prioritizes interrupts into five levels. When addressed during chip-select time, the IIR freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When Bit 0 is a logic 0, an interrupt is pending and the IIR content may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending.

Bits 1–3: These 3 bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table VIII.

Bits 4–7: These 4 bits of the IIR are always at logic 0.

Modem Control Register 2

This register controls the modem interface with the TP3330.

Bit 0: This bit is the Data Terminal Ready indicator. A logic high indicates that the CPU is ready for data transfer. When Bit 0 is reset from a high to low state for more than 50 ms, a loss of DTR disconnect sequence is generated.

Bit 1: This bit is the Request to Send indicator. It is not used by the TP3330.

Bit 2: This bit is the Output 1 (OUT1) signal. It is internally connected to generate a Master Reset to the TP3330 when this bit is set to a logic 1. During normal operation, this bit must be kept at logic low.

Bit 3: This bit is the Output 2 (OUT2) signal. When Bit 3 is set to logic 0, it is internally connected to disable the interrupt (INTR) output signal, and INTR is in TRI-STATE. Bit 3 should be set to logic 1 to enable the Interrupt output line.

TABLE VIII. Interrupt Control Functions

Interrupt Identification Register					Interrupt Set and Reset Functions		
Bit 3	Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	0	0	1	—	None	None	—
0	1	1	0	Highest	Receiver Line Status	Overrun, or Parity, or Framing Error, or Break Interrupt, or Sync-Detect	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register, (If Source of Interrupt) or Writing into the Transmitter Holding Register
0	0	0	0	Fourth	Modem Status	Clear to Send, Data Set Ready, Ring Indicator, Carrier Detect, Call Progress Tone Detect	Reading the Modem Status Register 2
1	0	0	0	Fifth	Modem Status	2225 Hz Answer Tone, Scrambled 1, Unscrambled 1, Receive Speed, Dotting Pattern Detected	Reading the Modem Status Register 1

Functional Description (Continued)

Bit 4: A logic 1 enables the USART Digital Loopback test mode. It should be reset to logic 0 for normal data transfer.

Bits 5,6: These bits are permanently set to logic 0.

Bit 7: This is the Address Select Bit for the internal registers of TP3330. (Refer to Tables V and VI.)

Modem Status Register 2

This register provides information on the current state of the interface control signals from the modem to the CPU.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. A logic 1 indicates that the Clear to Send (CTS) status bit has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the Data Set Ready status bit has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the device has changed from a low to a high state.

Bit 3: This bit is the Delta Carrier Detect (DCD) indicator. Bit 3 indicates that the Carrier Detect or Call Progress Tone Detect (CD) indicator has changed state.

Bit 4: This bit is the Clear to Send Indicator. It goes to a logic 1 when the TP3330 completes the modem handshaking process, and is ready for data transfer. When Bit 4 (Loop) of the MCR2 is set to a logic 1, this bit is equivalent to RTS in the MCR2.

Bit 5: This bit is the Data Set Ready indicator. Bit 4 indicates to the CPU that the TP3330 is ready. It is set to logic 1 when the TP3330 is in power up mode, and reset to logic 0 when the device is powered down. When Bit 4 of the MCR2 is set to a logic 1, this bit is equivalent to DTR of the MCR2.

Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If Bit 4 of the MCR2 is set to a logic 1, this bit is equivalent to OUT1 in the MCR2.

Bit 7: This bit is the Carrier Detect (CD) indicator. A logic 1 indicates that a valid carrier signal exceeding the pre-selected threshold level is received for a period exceeding t_{CDON}. When the Call Progress Tone Detector is enabled by setting Bit 5 of the Dialing Control Register, Bit 7 indicates the presence of the call progress tones within the passband of 350–620 Hz. When Bit 4 of the MCR is set to a logic 1, this bit is equivalent to OUT2 of the MCR2.

Scratchpad Register

This 8-bit Read/Write register is intended as a scratchpad register to be used by the programmer to hold data temporarily. It does not control the device's function in any way.

Typical Application

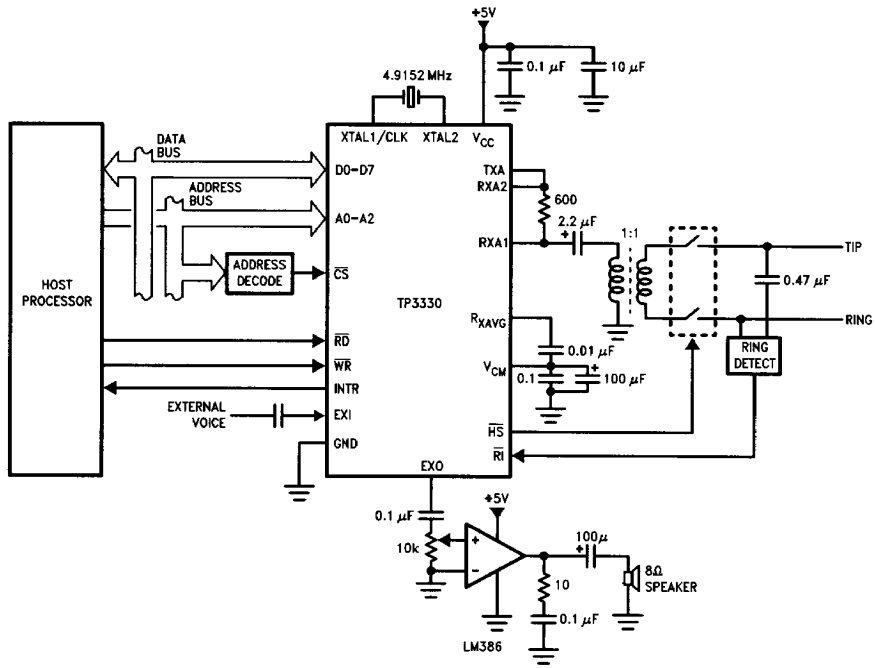

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FIGURE 2. Typical Application for an Integral Modem

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Operating Temperature Range	−25°C to +80°C
Storage Temperature Range	−65°C to +150°C
V_{CC} with Respect to GND	+7V
Voltage at Any Input	V_{CC} + 0.3V to GND − 0.3V
Voltage at Any Output	V_{CC} + 0.3V to GND − 0.3V
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

ESD Rating is to be determined

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Voltage				0.7	V
V_{IH}	Input High Voltage		2.0			V
V_{OL}	Output Low Voltage	I_{OL} = +1.0 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −0.1 mA	2.4			V
I_{IL}	Input Low Current All Digital Inputs	GND < V_{IN} < V_{IL}	−10		10	μA
I_{IH}	Input High Current All Digital Inputs	V_{IH} < V_{IN} < V_{CC}	−10		10	μA
I_{OZ}	TRI-STATE® Output Leakage Current	D0–D7, INTR, GND < V_O < V_{CC}	−20		20	μA
$I_{CC}0$	Power-Down Current	Outputs Open		0.4		mA
$I_{CC}1$	Power-Up Current	Outputs Open		30		mA

AC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TRANSMITTER						
V_{OXA}	Output Level at TXA	V_{CC} = 5.0V, R_{LXA} = 1.2 kΩ Bit 4, 5 of MCR1 = 0 High Band Carrier 2100/2225 Hz Answer Tone 550/1800 Hz Guard Tone DTMF, High Group DTMF, Low Group		 550 550 275 775 615		 mVrms mVrms mVrms mVrms mVrms
P_E	DTMF High Group Pre-Emphasis		1.0	2.0	3.0	dB
V_{OS}	Mean Output DC Offset Voltage at TXA	V_{CC} = 5.0V		2.5		V
E_{OX}	Out-of-Band Spectral Density Reference to Carrier	3.4 kHz < f < 8 kHz 8 kHz < f < 256 kHz		−45 −65		dB dB
THD	DTMF Distortion	V_{CC} = 5.0V, R_{LXA} = 1.2 kΩ, 300 Hz–3.4 kHz	−20			dB
G_{XI}	Voltage Gain from EXI to TXA	Input = 100 mVrms, f = 1 kHz Bit 5 of HCR = 1	dB	9.5		
R_{OXA}	Output Dynamic Resistance		Ω	1		
R_{LXA}	Load Resistance		1	1.2		kΩ
C_{LXA}	Load Capacitance				100	pF

Note 1: Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = 5.0V ±5%, GND = 0V, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical values are measured at V_{CC} = 5.0V, T_A = 25°C.

Note 2: All tests on AC parameters of Transmitter and Receiver are based on test circuit shown in *Figure 3.*

Note 3: 0 dBm into 600Ω = 0.775 Vrms.

Note 4: Crystal specification: Parallel Resonant 4.9152 MHz, R_S < 150Ω, L = 67.6 MH, C_M = 0.015 pF, C_H = 5 pF.

AC Electrical Characteristics (Note 1) (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVER						
R_{RIN}	Input Resistance	From RXA1 to GND		10		kΩ
		From RXA2 to GND		100		kΩ
S_R	Input Signal Level		−43		−12	dBm
TH_{CD}	Carrier Detect Threshold	Bits 3, 2 or MCR1 = 0, 0 ON		−43		dBm
		OFF		−46		dBm
		Bits 3, 2 of MCR1 = 0, 1 ON		−38		dBm
		OFF		−41		dBm
		Bits 3, 2 of MCR1 = 1, 0 ON		−33		dBm
		OFF		−36		dBm
H_{CD}	Carrier Detect Hysteresis	Measured from TH_{CD} ON to TH_{CD} OFF	2	3	5	dB
I_D	Peak Intersymbol Distortion (Isochronous ± Bias)	Back-to-Back, Received Level at −12 dBm, 300 BPS, 511-Bit Pattern		5		%
BER	Bit Error Rate	Back-to-Back, with Additive 300 Hz–3.4 kHz Flat Noise, Received Level at −12 dBm 511-Bit Pattern				
		300 BPS, S/N = 5 dB		10^{-5}		
		600 BPS, S/N = 10 dB		10^{-6}		
		1200 BPS, S/N = 12 dB		10^{-6}		
G_{RO}	Voltage Gain from RXA1 to EXO	Input = 200 mVrms, f = 1 kHz Bit 4 of HCR = 1		6		dB
R_{LEXO}	Load Resistance at EXO		10			kΩ
C_{LEXO}	Load Capacitance at EXO				100	pF
t_{CDON}	Carrier Detector Acquisition Time	300 BPS	100	160	200	ms
		600/1200 BPS				
		Originating Mode	230	267	310	ms
		Answering Mode	755	765	775	ms
t_{CDOFF}	Carrier Detector Release Time		10	17	24	ms
t_{PDON}	Call Progress Tone Detector Acquisition Time	350 Hz < f < 620 Hz		40		ms
t_{PDOFF}	Call Progress Tone Detector Release Time	350 Hz < f < 620 Hz		40		ms
t_{CTSON}	CTS ON Acquisition Time	300 BPS,				
		Originating Mode	755	765	775	ms
		Answering Mode	100	160	200	ms
		600 BPS/1200 BPS,				
		Originating/Answering Mode	755	765	775	ms
t_{DTRD}	Loss of DTR Disconnect Time	From DTR OFF to CD or CTS OFF	57	68	77	ms
t_{CDD}	Loss of Carrier Disconnect Time	From CD OFF to CTS OFF	405	415	425	ms

Note 1: Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, GND = 0V, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical values are measured at V_{CC} = 5.0V, T_A = 25°C.

AC Electrical Characteristics (Note 1) (Continued)

Symbol	Parameter	Conditions	Min	Max	Units
BUS TIMING READ CYCLE					
t_{SCR}	Chip Select Setup before $\overline{RD}$		50		ns
t_{HRC}	Chip Select Hold Time after $\overline{RD}$		20		ns
t_{SAR}	Address Setup before $\overline{RD}$		60		ns
t_{HRA}	Address Hold Time after $\overline{RD}$		20		ns
t_{WRD}	$\overline{RD}$ Pulse Width		125		ns
t_{DRD}	Data Delay from $\overline{RD}$	C_L = 100 pF		125	ns
t_{ZRD}	$\overline{RD}$ Invalid to Data Floating	C_L = 100 pF	0	100	ns
t_{RC}	Read Cycle Time		360		ns
WRITE CYCLE					
t_{SCW}	Chip Select Setup before $\overline{WR}$		50		ns
t_{HWC}	Chip Select Hold Time after $\overline{WR}$		20		ns
t_{SAW}	Address Setup before $\overline{WR}$		60		ns
t_{HWA}	Address Hold Time after $\overline{WR}$		20		ns
t_{WWR}	$\overline{WR}$ Pulse Width		100		ns
t_{SDW}	Data Set Up before $\overline{WR}$		40		ns
t_{HWD}	Data Hold Time after $\overline{WR}$		40		ns
t_{WC}	Write Cycle Time		360		ns

Note 1: Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = 5.0V ±5%, GND = 0V, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical values are measured at V_{CC} = 5.0V, T_A = 25°C.

Note 2: All tests on AC parameters of Transmitter and Receiver are based on test circuit shown in *Figure 3.*

Note 3: 0 dBm into 600Ω = 0.775 Vrms

Note 4: Crystal specification: Parallel Resonant 4.9152 MHz, R_S < 150Ω, L = 67.6 mH, C_M = 0.015 pF, C_H = 5 pF.

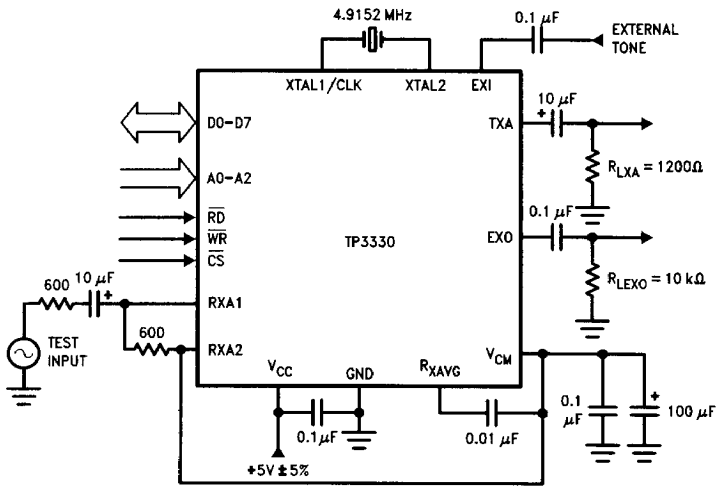

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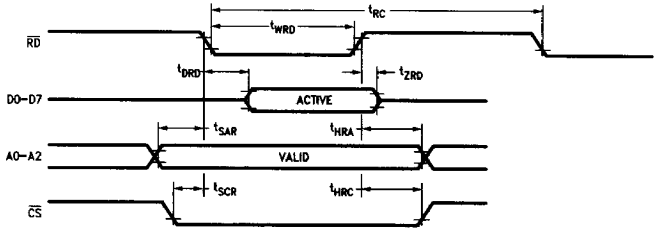
FIGURE 3. AC Test Circuit

Timing Waveforms

READ CYCLE



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WRITE CYCLE

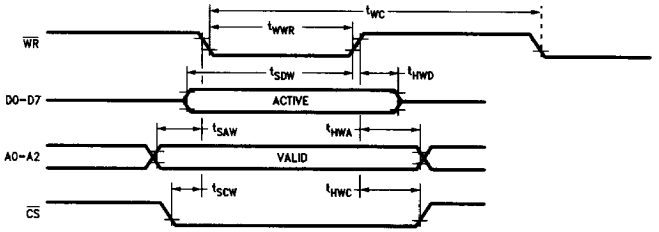

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FIGURE 4. Data Bus Timing Diagram

ORIGINATING MODEM

ANSWERING MODEM

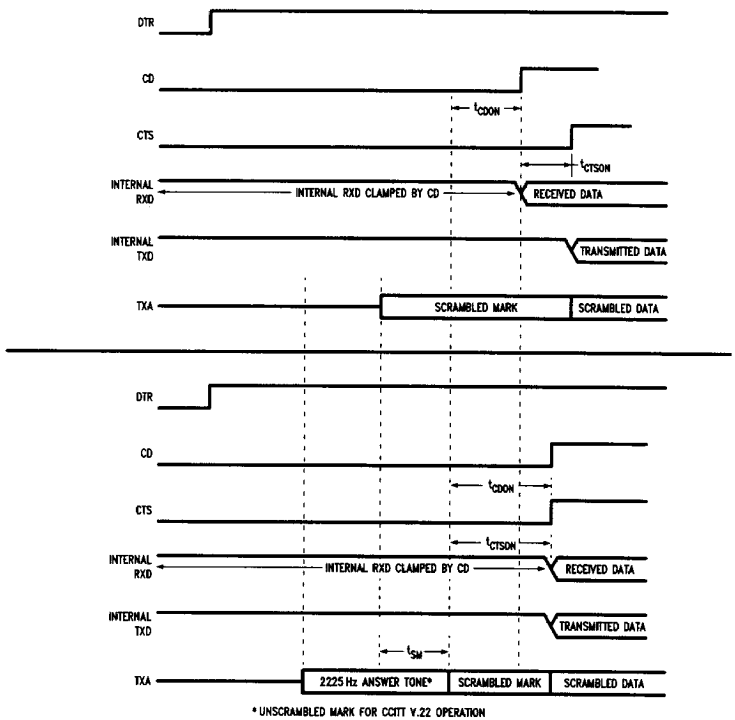

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FIGURE 5. TP3330 Configured in Bell 212A 1200 BPS Mode

Timing Waveforms (Continued)

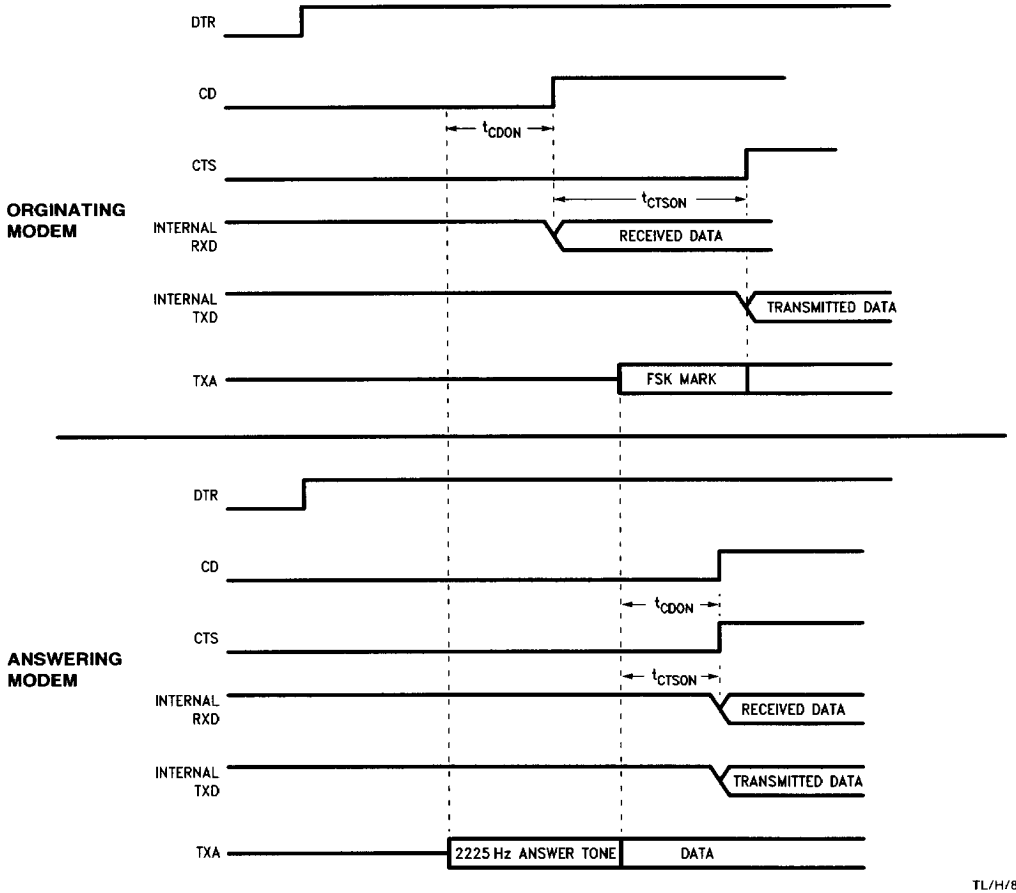

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FIGURE 6. TP3330 Configured in Bell 212A 300 BPS Mode

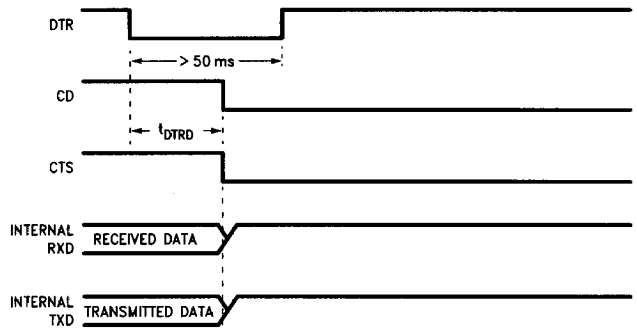

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FIGURE 7. Loss of DTR Disconnect Sequence

Timing Waveforms (Continued)

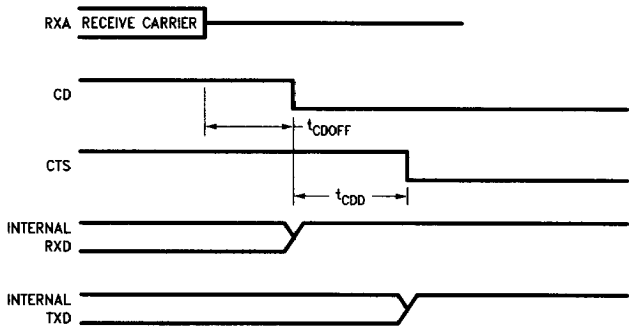

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FIGURE 8. Loss of Carrier Disconnect Sequence