

2048 x 8 BIT STATIC CMOS RAM

DESCRIPTION The μPD447 is a high speed, low power, 2048 word by 8 bit static CMOS RAM fabricated using an advanced silicon gate CMOS technology. A unique circuitry technique makes the μPD447 a very low operating power device which requires no clock or refreshing to operate.

Since the device has two chip enable inputs, it is suited for battery backup applications. Minimum standby power current is drawn by this device when $\overline{CE2}$ equals V_{CC} independently of the other input levels.

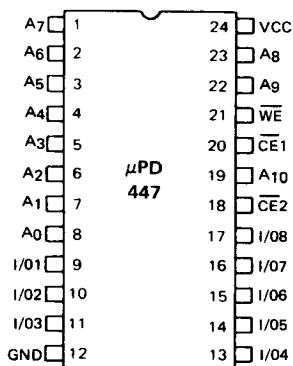
Data Retention is guaranteed at a power supply voltage as low as 2V.

The μPD447 is packaged in a standard 24-pin dual-in-line package and is plug-in compatible with 16K EPROMs.

FEATURES

- Single +5V Supply
- Fully Static Operation — No Clock or Refreshing required
- TTL Compatible — All Inputs and Outputs
- Common Data Input and Output Using Three-State Output
- Two Chip Enable Inputs for Battery Operation
- Max Access/Min Cycle Times Down to 120 ns
- Low Power Dissipation; 45 mA Max Active/100 μA Max Standby/10 μA Max Data Retention
- Data Retention Voltage — 2V Min
- Standard 24-Pin Plastic and Ceramic Packages
- Plug-in Compatible with 16K EPROMs

PIN CONFIGURATION



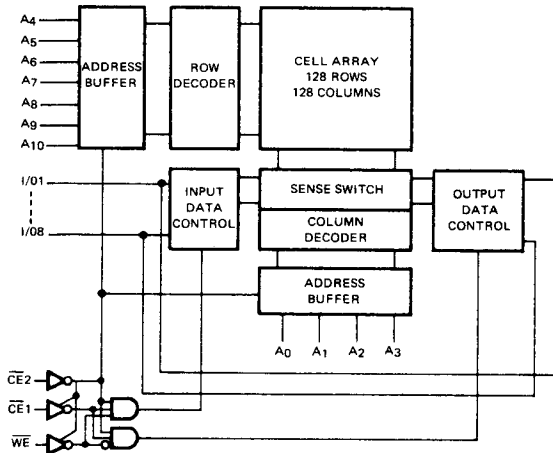
PIN NAMES

A0-A10	Address Inputs
WE	Write Enable
CE1-CE2	Chip Enable Inputs
I/O1-I/O8	Data Input/Output
VCC	Power (+5V)
GND	Ground

TRUTH TABLE

CE1	CE2	WE	MODE	I/O	ICC
X	H	X	NOT SELECTED	HZ	STANDBY
H	X	X	NOT SELECTED	HZ	ACTIVE
L	L	L	WRITE	D _{IN}	ACTIVE
L	L	H	READ	D _{OUT}	ACTIVE

μPD447



BLOCK DIAGRAM

Supply Voltage 7.0V
 Input or Output Voltage Supplied -0.3 to $V_{CC} + 0.3V$
 Storage Temperature Range -55°C to 125°C
 Operating Temperature Range 0°C to 70°C

ABSOLUTE MAXIMUM RATINGS*

COMMENT Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* $T_a = 25^\circ C$

$V_{CC} = 5V \pm 10\%$, $T_a = 0^\circ C$ to $70^\circ C$

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS									UNIT
			μPD447-2			μPD447-1			μPD447			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input High Voltage	V _{IH}		2.2		V _{CC} + 0.3	2.2		V _{CC} + 0.3	2.2		V _{CC} + 0.3	V
Input Low Voltage	V _{IL}		-0.3		0.8	-0.3		0.8	-0.3		0.8	V
Input Leakage Current	I _{LI}	V _{IN} = 0 ~ V _{CC}	-1.0		1.0	-1.0		1.0	-1.0		1.0	μA
I/O Leakage Current	I _{LO}	V _{CE2} = V _{IH} V _{I/O} = 0 ~ V _{CC}	-1.0		1.0	-1.0		1.0	-1.0		1.0	μA
Operating Supply Current	I _{CCA1}	V _{CE2} = V _{IL} I _{I/O} = 0 MIN TCYCLE		30	45		25	39		20	30	mA
	I _{CCA2}	V _{CE2} = V _{IL} I _{I/O} = 0 DC CURRENT		5	10		5	10		5	10	mA
Standby Current	I _{CCS}	V _{CE2} = V _{CC} V _{IN} = 0 ~ V _{CC}			100			100			100	μA
Output High Voltage	V _{OH}	I _{OH} = -1.0 mA	2.4			2.4			2.4			V
Output Low Voltage	V _{OL}	I _{OL} = 2.0 mA			0.4			0.4			0.4	V

DC CHARACTERISTICS

$T_a = 25^\circ C$, $f = 1.0$ MHz

PARAMETER	SYMBOL	LIMITS		UNIT	TEST CONDITIONS
		MIN	MAX		
Input Capacitance	C_{IN}		6	pF	$V_{IN} = 0V$
Input/Output Capacitance	$C_{I/O}$		8	pF	$V_{I/O} = 0V$

CAPACITANCE

Bob

μPD447

#345 CS access
time

AC CHARACTERISTICS

V_{CC} = 5.0

Read C
Access
Chip E
Chip F
Output
Chip I
Chip I
Chip
Chip

for μPD447-2

is it 120?

or is it 60?

Use CE1 to output valid.

447	
MAX	UNIT
	ns
200	ns
100	ns
200	ns
	ns
	ns
	ns
100	ns
100	ns

3

WRITE CYCLE

V_{CC} = 5.0V ± 10%, T_a = 0°C to 70°C

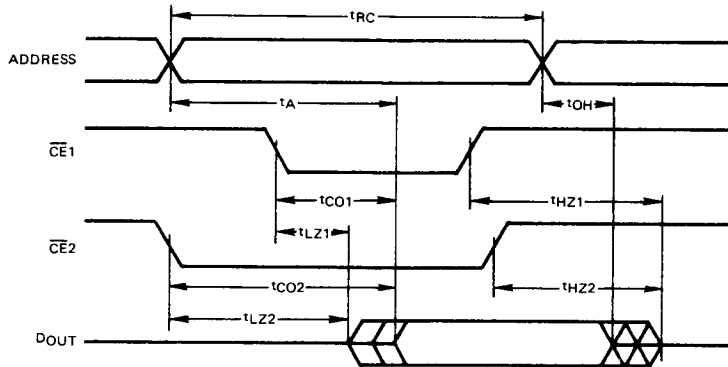
PARAMETER	SYMBOL	LIMITS						UNIT
		μPD447-2		μPD447-1		μPD447		
		MIN	MAX	MIN	MAX	MIN	MAX	
Write Cycle Time	tWC	120		150		200		ns
Chip Enable (CE1) to End of Write	tCW1	100		125		170		ns
Chip Enable (CE2) to End of Write	tCW2	100		125		170		ns
Address Setup Time	tAW	0		0		0		ns
Write Pulsewidth	tWP	100		125		170		ns
Write Recovery Time	tWR	0		0		0		ns
Write Enable to Output in HZ	tWZ		60		75		100	ns
Output Active from End of Write	tOW	20		20		20		ns
Data Valid to End of Write	tDW	60		75		100		ns
Data Hold Time	tDH	0		0		0		ns

T_a = 0°C to 70°C

LOW V_{CC} DATA RETENTION

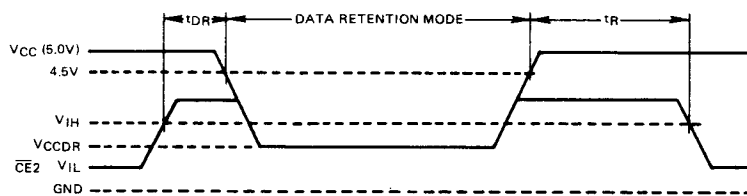
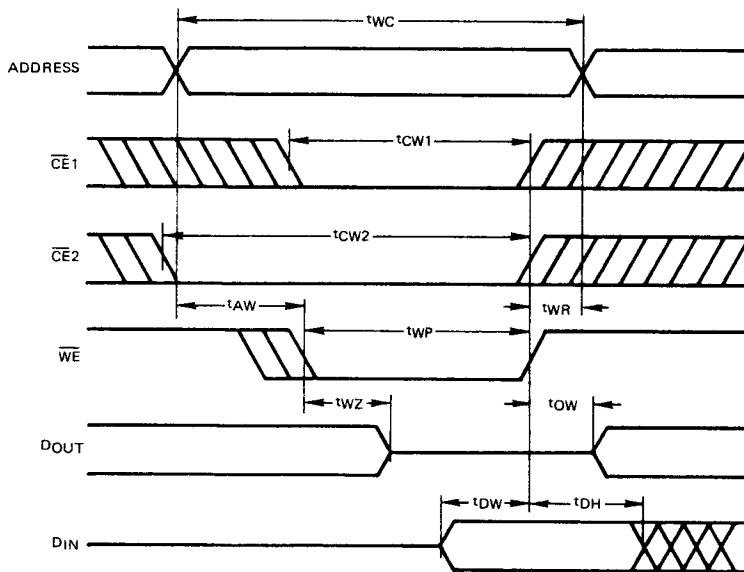
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V _{CC} for Data Retention	V _{CCDR}	V _{IN} = 0 ~ V _{CC} , V _{CE2} = V _{CC}	2.0			V
Data Retention Current	I _{CCDR}	V _{CC} = 3.0V, V _{IN} = 0 ~ V _{CC} V _{CE2} = V _{CC}		0.1	10	μA
Chip Disable to Data Retention Time	t _{CDR}		0			ns
Operation Recovery Time	t _R		t _{RC}			ns

READ CYCLE TIMING CHART



TIMING WAVEFORMS

WRITE CYCLE TIMING CHART

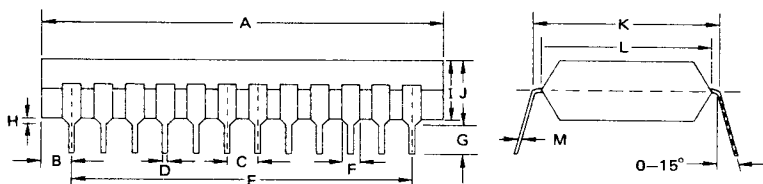


**LOW VCC
DATA RETENTION
TIMING CHART**

AC TEST CONDITIONS

Input Pulse Levels	0.8V to 2.2V
Input Rise and Fall Times	10 ns
Input and Output Timing Reference Levels	1.5V
Output Load	1 TTL + 100 pF

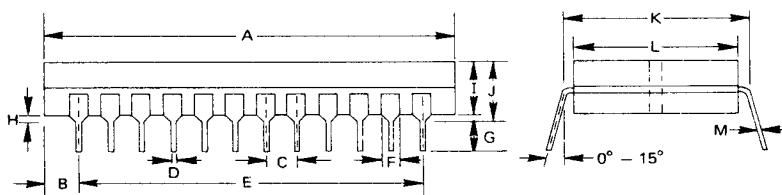
PACKAGE OUTLINE
μPD447C



(PLASTIC)

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	+0.10 -0.05	0.01 +0.004 -0.0019

μPD447D



(CERDIP)

ITEM	MILLIMETERS	INCHES
A	33.5 MAX.	1.32 MAX.
B	2.78	0.11
C	2.54	0.1
D	0.46	0.018
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN.	0.1 MIN.
H	0.5 MIN.	0.019 MIN.
I	4.58 MAX.	0.181 MAX.
J	5.08 MAX.	0.2 MAX.
K	15.24	0.6
L	13.5	0.53
M	+0.10 -0.05	0.01 +0.004 -0.002