XC3300 Family
HardWire™ Logic Cell Arrays

PRELIMINARY Product Specification

FEATURES

- Mask Programmed versions of Xilinx Programmable Logic Cell Arrays (LCA)
  - Cost reduction for high volume applications
  - Transparent conversion from Programmable LCA
  - On-chip scan path test latches
  - High Performance 1.2 μ CMOS process
  - 100 MHz flip-flop toggle rate
- Easy Conversion from Programmable LCA
  - Architecturally identical to Programmable LCA
  - Fully pin and performance compatible
  - Same specifications as Programmable LCA
  - Supports daisy-chained configuration modes
  - Test program automatically generated
  - Emulates Programmable Configuration Signals
- Advanced Second Generation Architecture
  - Compatible arrays up to 9000 gate complexity
  - Extensive register and I/O capabilities
  - Two global clocks (less than 1 ns skew)
  - Internal 3-state bus capabilities
  - On-chip oscillator

DESCRIPTION

The Xilinx Logic Cell Array (LCA) family provides a group of high-performance, high-density digital integrated circuits. Their regular, extendable, flexible architecture is composed of three types of configurable elements: a perimeter of IOBs, a core array of CLBs and circuitry for interconnection. The general structure of a LCA device is shown in Figure 4.

The Xilinx XC3300 family of HardWire devices are mask programmed versions of the Xilinx XC3000 Programmable Logic Cell Arrays. In high-volume applications where the design is stable, the programmable LCAs used for prototyping and initial production can be replaced by their HardWire equivalents. This offers a significant cost reduction with virtually no risk or engineering resources required.

In a Programmable LCA the logic functions and interconnections are determined by the configuration program data loaded and stored in internal static memory cells. The HardWire LCA has the identical architecture as the Programmable LCA it replaces. All CLBs, IOBs, interconnect topology, power distribution and so on are the same. In the HardWire LCA the memory cells and the logic they control are replaced by metal connections. Thus the HardWire LCA is a semicustom device manufactured to provide a customer specific function, yet is completely compatible with the Programmable LCA it replaces.

Xilinx manufactures the HardWire LCA using the information from the Programmable LCA design file. Since the HardWire device is both pinout and architecturally identical with the Programmable LCA it is easily created without the need for all the costly and time-consuming engineering activities which other semicustom solutions would require. No redesign time; no expensive and time consuming simulation runs; no place and route; no test vector generation. The combination of the Programmable and HardWire LCA products simply offer the fastest and easiest way to get your product to market, and ensures a subsequent low-cost, low-risk high-volume cost reduction path.

HardWire Device	Replacement for Pin Compatible Programmable Device	Total Available Gates	File Submitted to Xilinx	Maximum Flip-Flop Toggle Frequency	Packages						
					PLCC			PQFP		PPGA	
					Pins	68	84	100	160	132	175
XC3330	XC3020, XC3030	3000	3030.LCA	100 MHz	I/O	58	74	80	–	–	–
XC3342	XC3042	4200	3042.LCA	100 MHz	I/O	58	74	82	–	–	–
XC3390	XC3064, XC3090	9000	3090.LCA	100 MHz	I/O	–	70	–	144	110	144

HARDWIRE APPLICATION

HardWire products are designed to provide a simple, low-risk path for a customer to achieve significant cost-reductions on a high-volume design which initially used the Programmable LCA. In the prototype and early production stages, and for low to moderate volume applications, the Programmable LCA is the solution of choice. Later in the life cycle - if the design is stable and goes into high-volume production - the HardWire device can be used in place of the original Programmable device.

Figure 1 shows the typical life cycle of a high-volume product, and illustrates the optimal way for using the Programmable and HardWire LCAs. During the development and prototype stages the Programmable LCA is used.

Production is started using a Programmable device and the design includes a method for storing the configuration bitstream. Using a Programmable device at this stage reduces risk, allows a faster time to market, and permits design modifications to be made without obsoleting any LCA devices. After a few months of production with the Programmable device, the HardWire device can be substituted in the circuit. This may also permit removal of an EPROM used for bitstream storage.

Since the circuit board was designed initially for a Programmable device, production can be switched back if the situation warrants. For example, if demand for the product increases dramatically, production can be increased in days or weeks by using Programmable devices. A change can be quickly made to the product with a Programmable device. There is no manufacturing leadtime with off-the-shelf, standard product Programmable devices. As another example, production can be switched to Programmable devices as the product nears the end of the life cycle. This avoids end-of-life buys and the risk of obsolescence.

HardWire Design/Production Interface

Figure 2 shows how the design, development and production activities are sequenced for both the Programmable and HardWire products. Notice that no additional activity is needed for the HardWire device until the design is in volume production. At that time there is a simple design analysis (done by Xilinx) prior to generating the custom mask, and then the HardWire prototypes are manufactured. An in-system verification is performed by the customer, and the HardWire is released to full production. As the architectures of the Programmable and HardWire LCAs are identical, virtually no engineering resources are needed to move from one to the other. By comparison, a traditional masked gate array attempting to "assemble" these logic functions from NAND gates to emulate the LCA would require extensive design activity. A comparison of the activities required to convert to a HardWire LCA versus a gate array is shown in Figure 3.

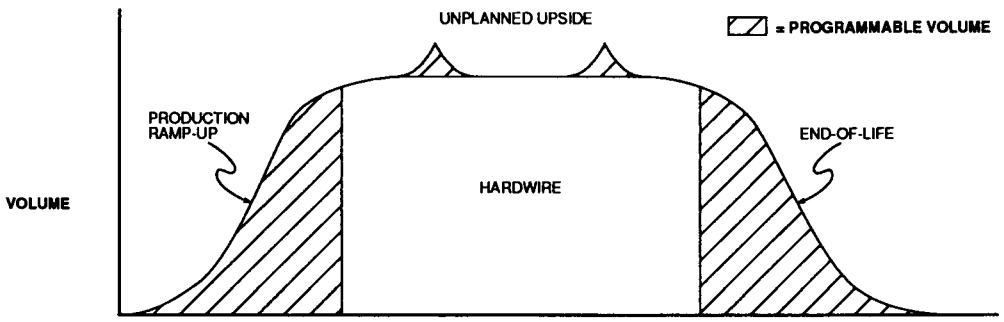


Figure 1. Typical High-Volume Product Life Cycle

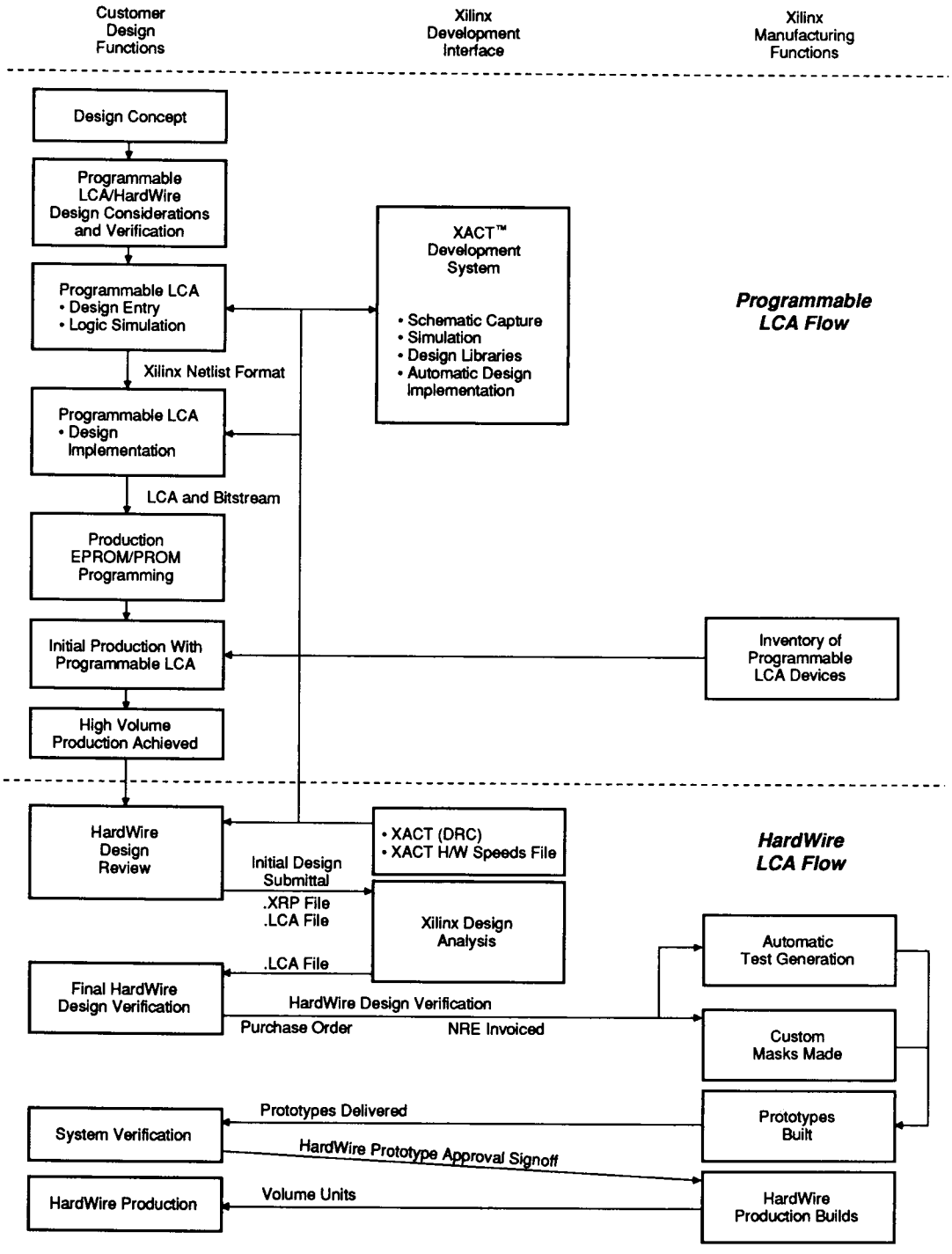


Figure 2. Programmable/HardWire Design/Production Interface. X1333

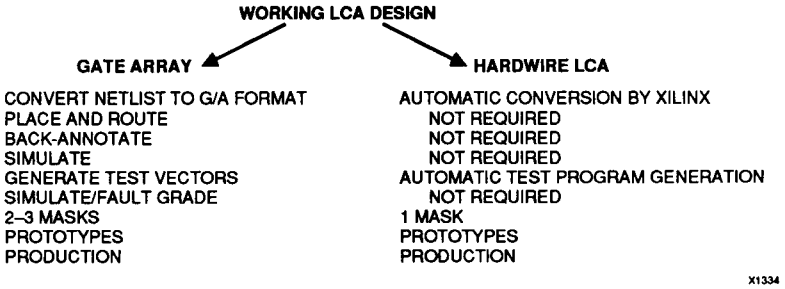


Figure 3. Design Flow Comparison: Gate Array versus Hardwire.

ARCHITECTURE

As shown in Figure 4, the HardWire LCA has the same architecture as the Programmable LCA it replaces. The perimeter of I/O Blocks (IOBs) provides an interface between the internal logic array and the device package pins. The array of Configurable Logic Blocks (CLBs) performs user-specified logic functions. The interconnect resources are programmed to form networks carrying logic signals among blocks, analogous to printed circuit board traces connecting SSI/MSI packages.

The logic functions of the blocks are implemented by look-up tables. Functional options are implemented by user-defined multiplexers. Interconnecting networks between blocks are implemented with user-defined fixed metal connections.

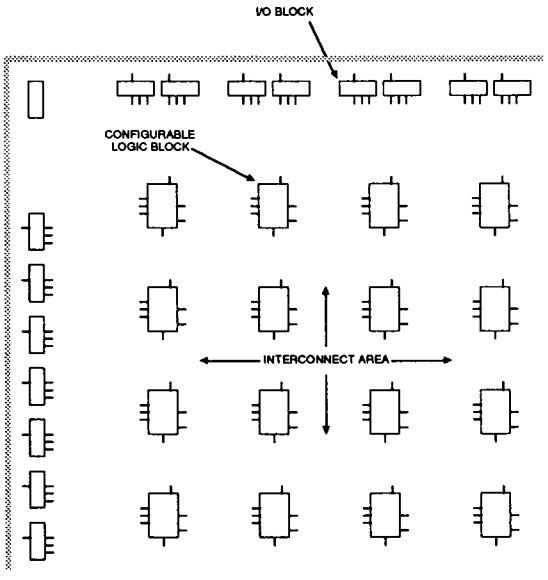


Figure 4. Logic Cell Array Structure

I/O Block

Each user-defined IOB (shown in Figure 5) provides an interface between the external package pin of the device and the internal user logic. The IOB is identical with that used in the Programmable LCA. There are a wide variety of I/O options available to the user.

Summary of I/O Options

- Inputs
  - Direct
  - Flip-flop/latch
  - CMOS/TTL threshold (chip inputs)
  - Pull-up resistor/open circuit
- Outputs
  - Direct/registered
  - Inverted/not
  - 3-state/on/off
  - Full speed/slew limited
  - 3-state/output enable (inverse)

Configurable Logic Block

The array of Configurable Logic Blocks (CLBs) provides the functional elements from which the user's logic is constructed. The logic blocks are arranged in a matrix within the perimeter of IOBs. For example, the XC3330 has 100 such blocks arranged in 10 rows and 10 columns.

The configurable logic block is identical to that used in the XC3000 family of Programable LCAs. Each configurable logic block has a combinatorial logic section, two flip-flops, and an internal control section. (See Figure 6.) There are: five logic inputs [*.a*, *.b*, *.c*, *.d* and *.e*]; a common clock input [*.k*]; an asynchronous direct reset input [*.rd*]; and an enable clock [*.ec*]. All may be driven from the interconnect resources adjacent to the blocks. Each CLB also has two outputs [*.x* and *.y*] which may drive interconnect networks.

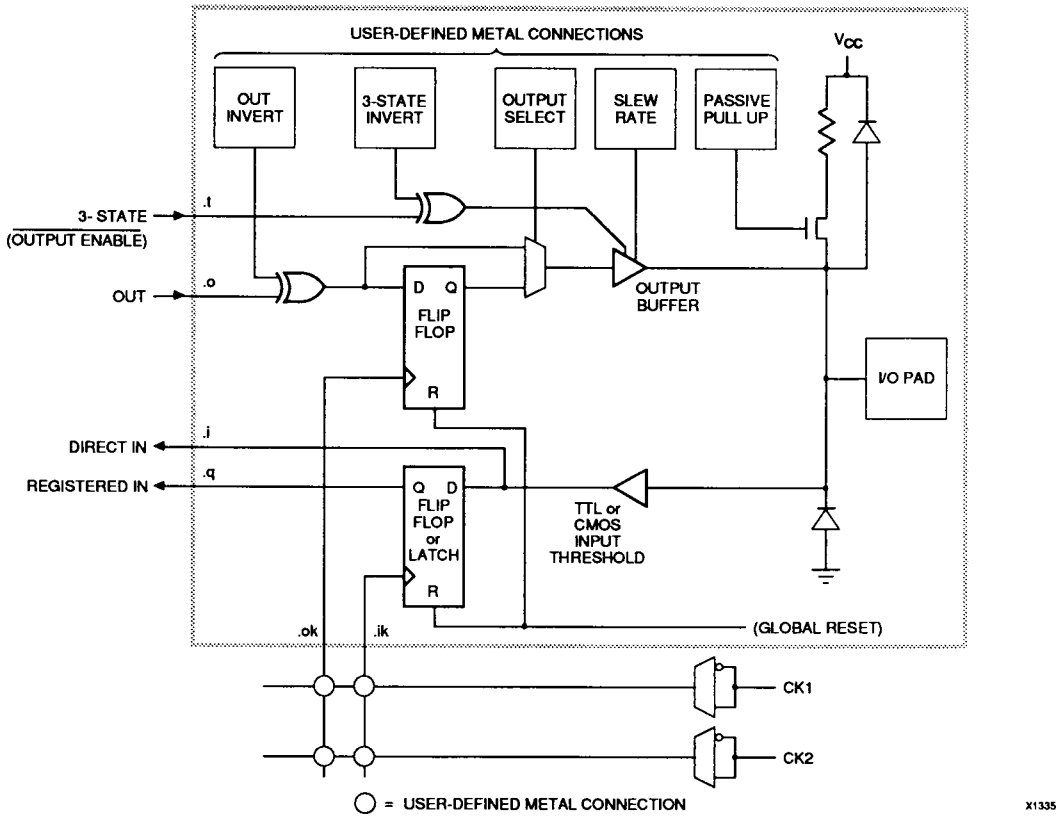


Figure 5. Input/Output Block. Each IOB includes input and output storage elements and I/O options pre-defined by the user. A choice of two clocks is available on each die edge. The polarity of each clock line (not each flip-flop or latch) is selectable. A clock line that triggers the flip-flop on the rising edge is an active Low Latch Enable (Latch transparent) signal and vice versa. Passive pull-up can only be enabled on inputs, not on outputs.
All user inputs are selectable for TTL or CMOS thresholds.

Interconnect

User-defined interconnect resources in the Logic Cell Array provide routing paths to connect inputs and outputs of the I/O and logic blocks into logic networks. Interconnections between blocks are composed from a two-layer grid of metal segments. The XACT development system provides automatic routing of these interconnections. The inputs of the IOBs and CLBs are multiplexers that are defined to select an input network from the adjacent interconnect segments.

Three types of metal resources are provided to accommodate various network interconnect requirements:

- General Purpose Interconnect
- Direct Connection
- Long Lines

The topology of all these interconnect resources is identical with that of the Programmable LCA, but the speed of the interconnect paths is significantly faster (since all interconnections are fixed metal connections).

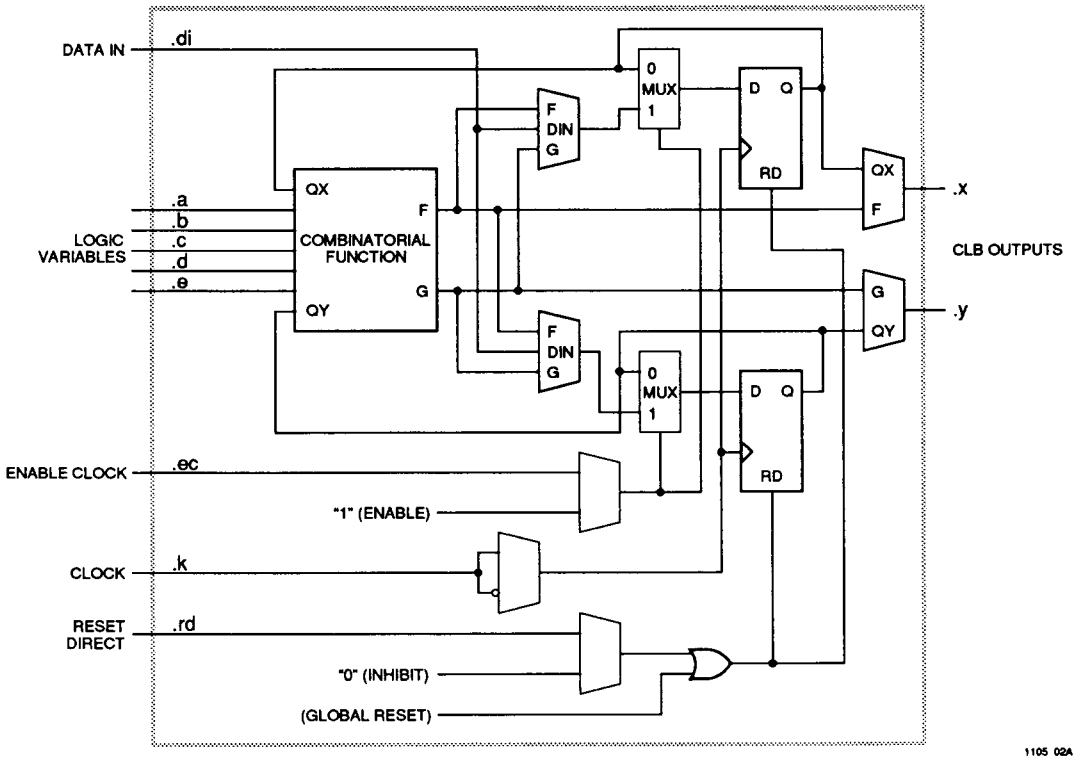


Figure 6. Configurable Logic Block. Each CLB includes a combinatorial logic section, two flip-flops and a user-defined multiplexer selection of function.

It has: five logic variable inputs .a, .b, .c, .d and .e.
a direct data in .di
an enable clock .ec
a clock (invertible) .k
an asynchronous reset .rd
two outputs .x and .y

CONFIGURATION and START-UP

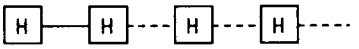
The XC3300 family of HardWire devices are designed to be fully compatible with their Programmable LCA equivalents. While the HardWire parts do not require the loading of configuration data, they fully support a wide variety of configuration modes.

Configuration

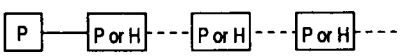
HardWire devices can be used stand-alone or in a daisy chain with other LCAs. A HardWire device cannot act in Master Parallel or Peripheral Mode. However designs which use these modes can be supported by selection of a mask option which forces the LCA into Master Mode. This allows HardWire devices to be used when the original design used Peripheral Mode, without requiring any changes to the circuit board.

Mode 1. As a stand alone HardWire Device.

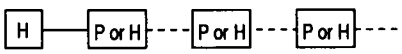
Mode 2. As a daisy chain of all HardWire Devices.



Mode 3. As a HardWire or programmable slave in a daisy chain with a Programmable device as a master.



Mode 4. As a HardWire device acting as a Serial Master with any combination of Programmable and HardWire devices as slaves.



(P = Programmable device, H = HardWire device)

X1336

A HardWire device will not "swallow" its own configuration data. Whatever configuration bits are fed into the DIN pin will appear on the DOUT pin after a delay TDIO. In any case where a HardWire device is ahead of a Programmable device in a daisy chain (as in Mode 3 and 4 shown above) the configuration data will need to be modified.

Start-up Sequence

The XC3300 HardWire devices are designed to emulate the start-up sequence of the Programmable LCA devices as closely as possible, however some differences do exist. The start-up sequence may be thought of as three stages: power-on-reset; internal clear; and configuration.

An internal power-on-reset circuit is triggered when power is applied. When VCC reaches the voltage at which portions of the LCA begin to operate, the device generates a POR (power-on reset) pulse. The I/O output buffers are disabled and a high-impedance pull-up resistor is provided for the user I/O pins. The length of the POR pulse is user-defined to be either 64 µs or 16 ms. The 64 µS pulse is used for a rapid reset cycle; the 16 ms pulse emulates the power-on sequence of a Programmable LCA. If the M0 pin is held Low during the POR cycle (or if the mask option to force the HardWire LCA into Master Mode is selected) the device will operate as a Master Mode device and the POR pulse will be extended to 4 times its nominal delay. This ensures that all daisy-chained slave devices will have sufficient time to power up.

Following the POR cycle, the HardWire device enters a "clearing" state. This state emulates the configuration memory clear performed by a Programmable LCA upon power-up. The length of the clear cycle is 256 cycles (nominally 256 µs) for a standard POR, but is only 2 cycles if the rapid reset cycle was selected.

At the completion of the clear cycle the RESET pin is sampled. If the RESET pin is being held Low, the "configuration" will be delayed (with the INIT pin held Low) until RESET is driven High. If the RESET pin is being driven High (or once it has been driven High following a delayed "configuration") the open drain INIT pin will be released and the value of the M0 pin will be latched. If the device is in Master Mode (M0 = Low) it will begin to produce CCLKs. If the device is in Slave Mode (M0 = High) it will require CCLKs to be supplied from another device. After 4 CCLK cycles the part is "configured" and the Done/Program (D/P) pin will be released. (If the device is in a daisy chain with the D/P pins tied together the D/P pin will remain Low until all devices have completed configuration.) One CCLK after the D/P pin goes High the I/Os will become active. The internal user-logic reset is user-defined to release either one CCLK cycle before or after the I/O pins become active. A HardWire device operating in Master Mode will stop producing CCLKs one cycle after the I/Os become active.

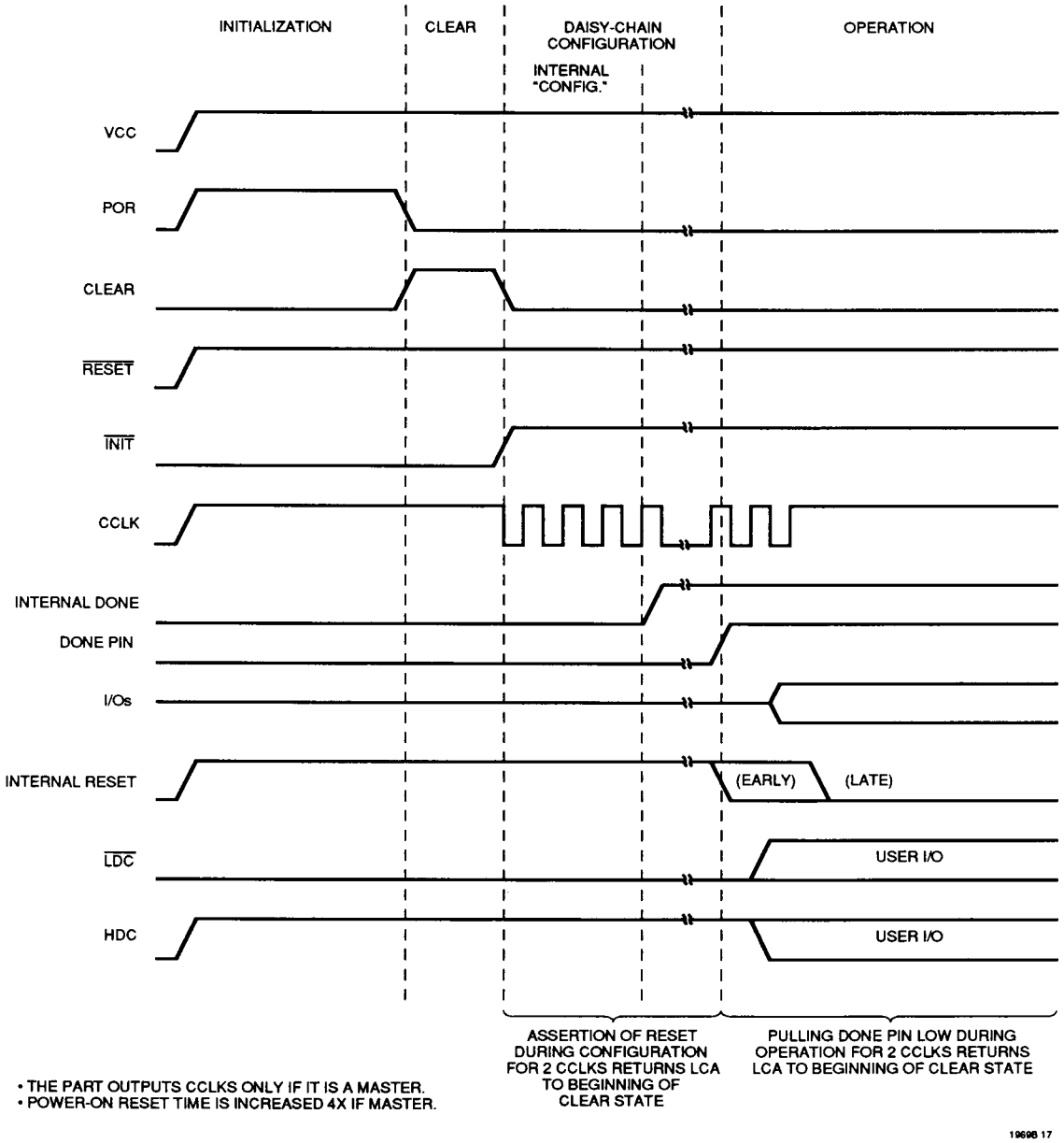


Figure 7. Psuedo-Configuration Waveform (Normal Power-Up)

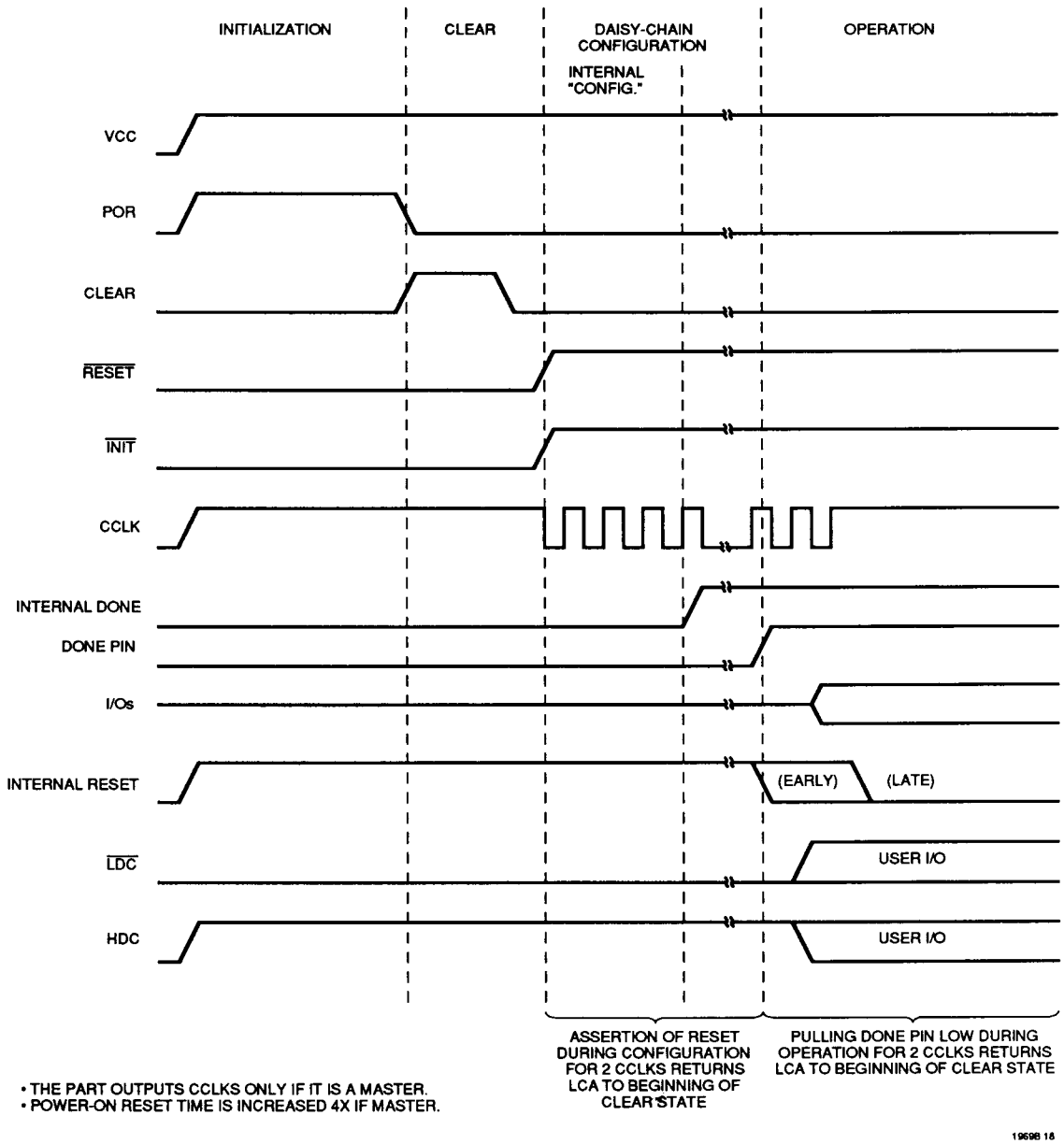


Figure 8. Psuedo-Configuration Waveform (Configuration Delay by Reset)

PERFORMANCE

The XC3300 family of HardWire devices are manufactured in the same high-performance 1.2µ CMOS technology as their Programmable LCA equivalents. Traditionally the toggle frequency of a flip-flop has been used to describe the overall performance of a semi-custom device. The configuration used for determining this rate is shown in Figure 9.

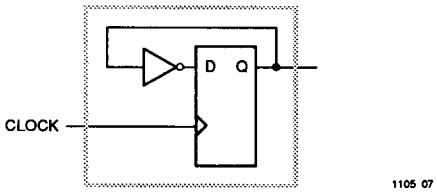


Figure 9. Toggle Flip-Flop. This is used to characterize device performance.

Actual LCA performance is determined by the timing of critical paths, including the timing for the logic and storage elements in that path and the timing of the associated interconnect. HardWire logic block performance is equal to or slightly faster than the equivalent Programmable LCA, while the interconnect performance is significantly faster.

All HardWire devices are specified and tested for operation at the fastest equivalent Programmable LCA speed available at the time the HardWire device is introduced. For the XC3300 family, this means all parts are guaranteed to the -100 speed grade. Since the finished HardWire product is customized for a specific customer and application, speed grading is not available.

POWER

Power for the LCA is distributed through a grid to achieve high noise immunity and isolation between logic and I/O. Inside the LCA, dedicated V_{CC} and ground rings surround the logic array and provide power to the I/O drivers. (See Figure 10.) An independent matrix of V_{CC} and ground lines supplies the interior logic of the device. This power distribution grid provides a stable supply and ground for all internal logic, providing the external package power pins are all connected and appropriately decoupled. Typically a 0.1-µF capacitor connected near the V_{CC} and ground pins will provide adequate decoupling.

Output buffers capable of driving the specified 4-mA loads under worst-case conditions may be capable of driving 25 to 30 times that current in a best case. Noise can be reduced by minimizing external load capacitance and reducing simultaneous output transitions in the same direction. It may also be beneficial to locate heavily loaded output buffers near the ground pads. The I/O Block output buffers have a slew-limited mode which should be used where output rise and fall times are not speed critical. Slew-limited outputs maintain their dc drive capability, but generate less external reflections and internal noise. A maximum total external capacitive load for simultaneous fast mode switching in the same direction is 500 pF per power/ground pin pair. For slew-rate limited outputs this total is four times larger.

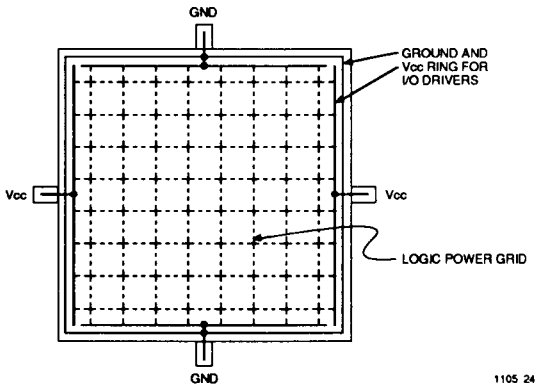


Figure 10. LCA Power Distribution.

HARDWIRE TESTABILITY

The XC3300 HardWire LCA products contain significant on-chip logic to facilitate manufacturability and testing. This logic, combined with Xilinx's internal Automatic Test Generation (ATG) software, assures 100% functionality. In fact, the HardWire device can be 100% functionally tested by Xilinx without the need for customer generated test vectors (as is required with custom gate arrays).

This section examines the two basic block structures and the special test circuitry in the HardWire LCA. An example of a small XC33XX (XC3330, XC3342, or XC3390) LCA design and the vectors generated for test are included.

Test Architecture

The HardWire LCA contains two types of internal blocks: the Input/Output Block (IOB) and the Configurable Logic Block (CLB). To accomplish 100% functional testing special test circuitry is designed into the device. This circuitry allows testing of each block (CLB and IOB) in a synchronized procedure known as "Scan Test". Special dedicated test latches (called TBLKs) are include on all HardWire devices. They are completely transparent to the normal operation of the circuit. Scan testing allows the contents of all internal flip-flops to be serially shifted off-chip, and for Xilinx generated test vectors to be shifted into the device, thus enabling all flip-flops to be initialized to any desired state.

These special dedicated test latches are placed into each CLB and IOB. Each CLB has four internal test latches, (placed at the CLB outputs), while each IOB contains three test latches (placed at the IOB inputs) as shown in Figures 11 and 12. The placement of these test latches is very important, since each CLB output or IOB input can fanout to multiple destinations. All sources and destinations of logic blocks come from other logic blocks, thus this placement of the latches provides complete access to all nets and synchronized control of all CLBs and IOBs.

The test latches are connected into a daisy chain which passes through every flip-flop in the LCA. Figure 13 shows an overview of the scan path. The path begins at the Scan In pin, sequences through each CLB, then through the IOBs, and finally exits at the Scan Out pin. This scan path can be seen in more detail in Figure 14, which shows the precise sequence with which the CLB and IOB internal test latches are loaded or read.

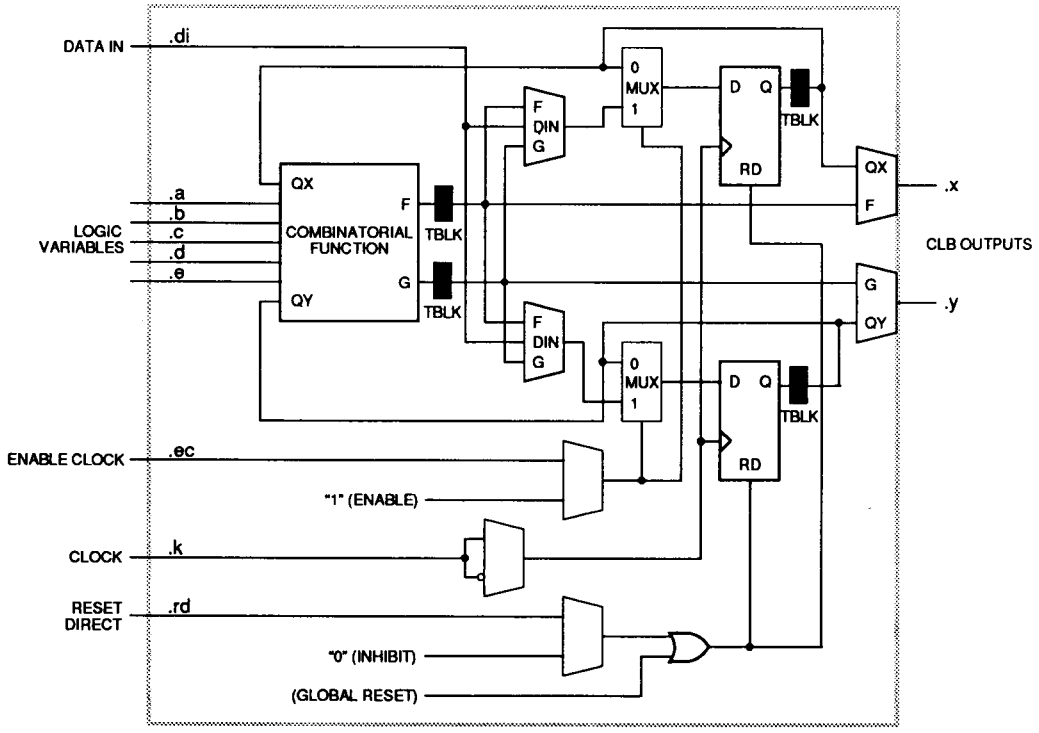


Figure 11. XC33XX HardWire CLB Test Latch Locations

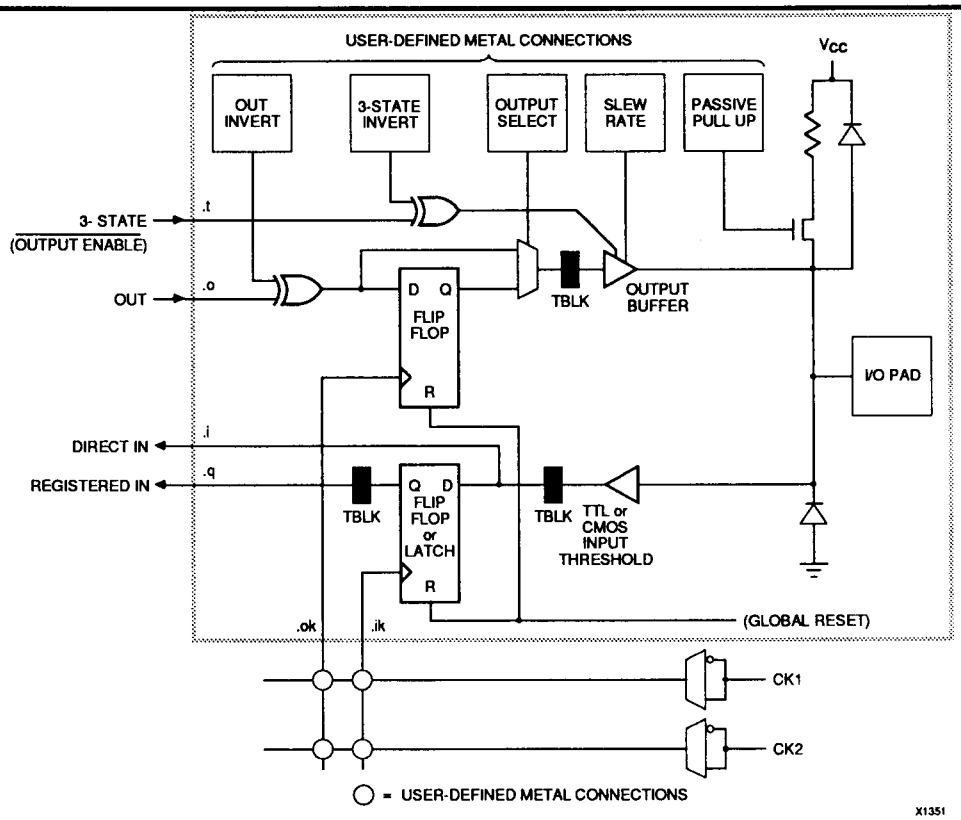


Figure 12. XC33XX HardWire IOB Test Latch Location

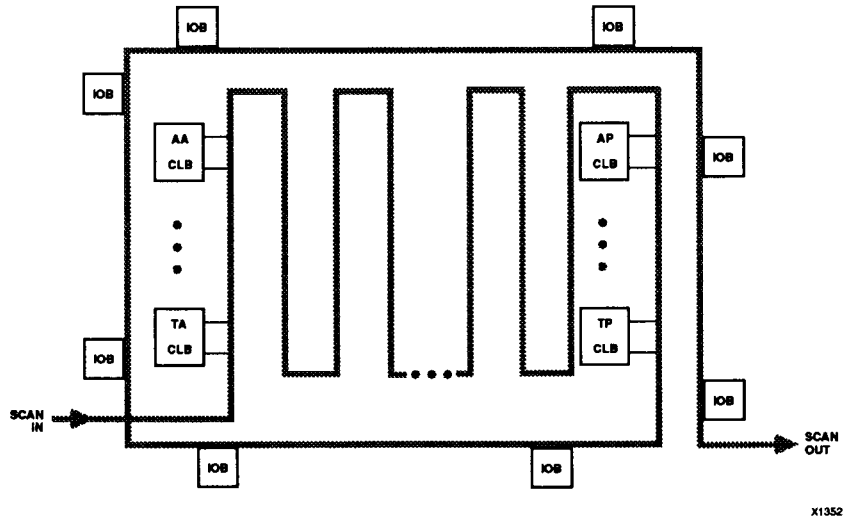


Figure 13. XC3390 Scan Path Overview

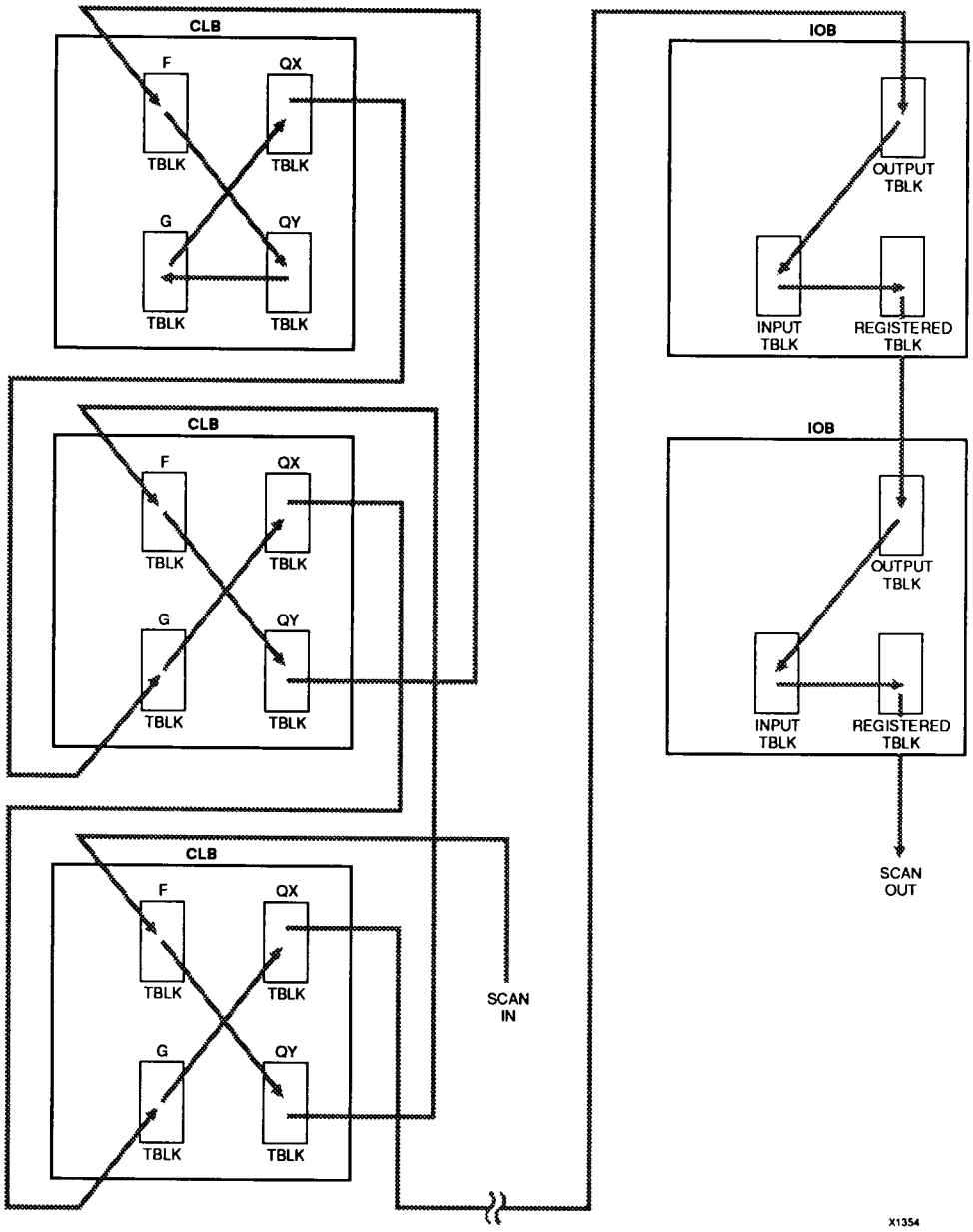


Figure 14. Detailed Scan Path

The internal architecture of a TBLK is shown in Figure 15. In the normal operation mode of the HardWire LCA, SW1 is in position A and all the test latches are bypassed completely. The HardWire device is set into Test Mode (SW1 = position B) by Xilinx ATG software. This software inputs unique conditions on several control pins while serially loading a "password" into the device. For this reason, it is not possible for a customer design to inadvertently place the HardWire into Test Mode. When SW1 is in position B (Test Mode) all the latches can receive data from either the CLB output or the previous latch in the daisy chain (SQn).

Synchronized together by a special test clock, all the test latches operate in two phases. The first phase serially loads all the latches to place a specific vector at the inputs of the logic block to be tested. The second phase is a parallel load of all latches, storing the expected output data of the logic block being tested (SW2 = A). At this point testing returns to phase one and serially clocks out the results, while simultaneously clocking in a new input vector.

Scan Test

To see how scan testing can be used to provide complete functional test coverage, consider the logic shown in Figure 16. This diagram shows a CLB (CLB2) with three inputs being driven by three different CLBs and the other two inputs being driven by two different IOBs. If we apply every possible combination of inputs to CLB2 and all expected output conditions are met, then CLB2 has been 100% functionally tested. The input conditions applied also include any register control signals (such as Clock, Reset, or Clock Enable). The same procedure is used for testing IOBs.

Looking again at Figure 16, CLB2 is tested by first serially loading the X output latches of CLB1, CLB3, and CLB4 and the input latches of IOB1 and IOB2. Note that the latches on CLB2's outputs are also loaded in this first phase. Not all CLBs and IOBs can be tested at once, due to signal dependencies. To position the correct data into the latches all unused latches still need "don't cares" loaded. Regardless of which CLBs and IOBs are being tested by a particular scan vector, the complete scan path is always shifted in and out for testing and verification. The state of CLB2's output latches will be opposite to their expected results in phase two. This guarantees that CLB2's input data changed the state of its output latches and therefore, is current data.

CLB or IOB data registers using a synchronous or asynchronous clock are not a problem during this special test mode. All customer-used registers are clock inhibited during the phase one load. The inhibit of register clocking is accomplished by logically "ANDing" the register clocks with the global inhibit control line.

The test vectors needed to perform this thorough testing are created by Xilinx. No additional effort or engineering time is required from the user to ensure proper device performance. The customer design file used to create the HardWire LCA is used in conjunction with specially developed Xilinx Automatic Test Generation software, which creates the complete set of test vectors required to perform 100% functional testing. This software creates the data for all possible input conditions and corresponding output data for each CLB and IOB used in the customer design. This data is then compiled into the test vectors used to perform the actual testing.

Scan Test Example

Finally, Figure 17 shows an example of a very simple design implemented in an XC3300 HardWire LCA. This example uses only two CLBs and one IOB, and therefore contains only 11 test latches. The sample test vectors in Figure 18 show how scan test would be used to perform functional testing of this design. Note that the set of vectors shown tests only one input condition (input A of the CLB under test). The actual test file would contain all the additional vectors needed to completely test this design.

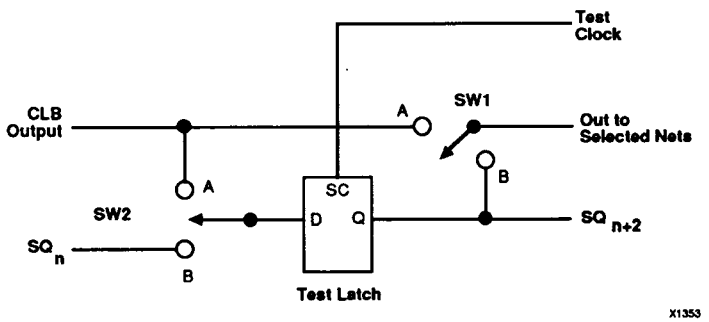


Figure 15. TBLK Block Diagram

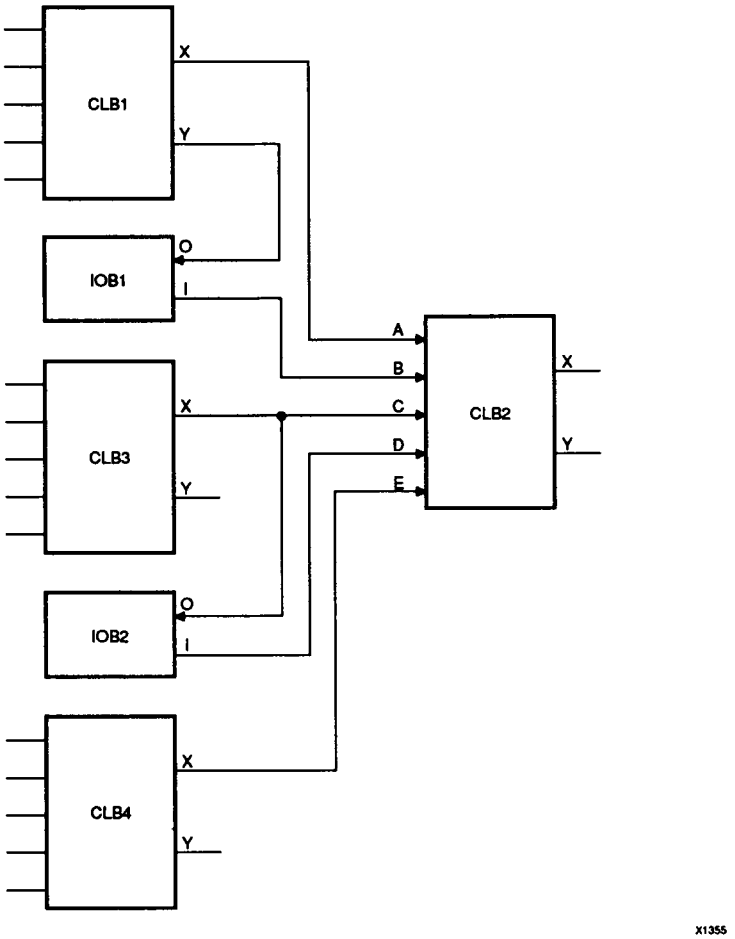


Figure 16. 5 Input CLB (CLB2) Driven by 3 Different CLB Outputs and 2 Different IOB Outputs

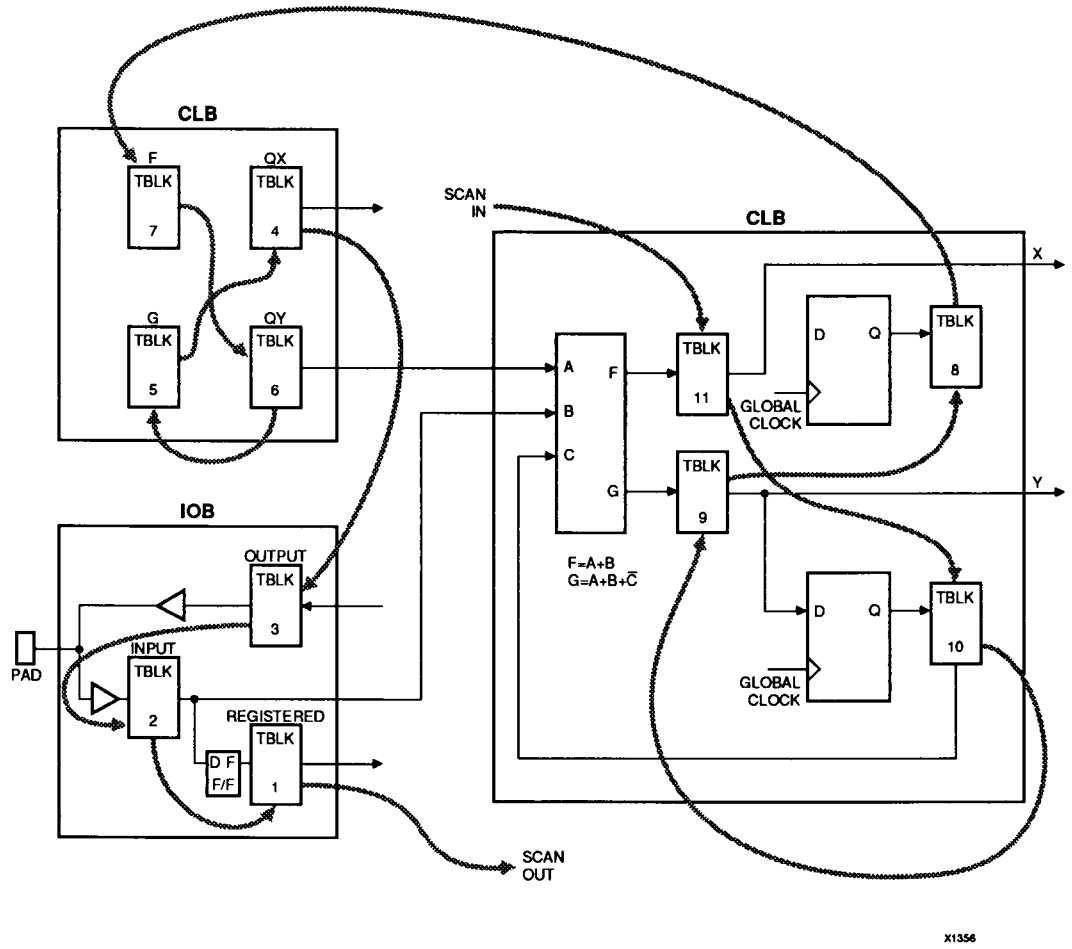


Figure 17. Test Example

The following vectors and comments show the testing of one input condition (input A of the CLB under test).

SCAN CLOCK	SCAN IN	SCAN OUT	GLOBAL CLOCK	COMMENTS
c	x	x	x	Load a "don't care" (0 or 1) into latch #1, not used.
c	1	x	x	Load a 1 into Scan In pin, knowing it will be positioned in latch #2, input B. The global clock is inhibited and the scan out data are "don't cares".
c	x	x	x	Load a "don't care" into latch #3, not used.
c	x	x	x	Load a "don't care" into latch #4, not used.
c	x	x	x	Load a "don't care" into latch #5, not used.
c	1	x	x	Load a 1 into Scan In pin for input A (latch #6).
c	x	x	x	Load a "don't care" into latch #7, not used.
c	x	x	x	Load a "don't care" into latch #8, not used.
c	0	x	x	Load a 0 into latch #9, expecting the G output to be a 1 after phase two.
c	0	x	x	Load a 0 into latch #10, expecting the register output to be a 1 after phase two.
c	0	x	x	Load a 0 into latch #11, exepcting the F output to be a 1 after phase two.
At this point all the latches are loaded. Enter phase two by changing the control pin (not shown here).				
0	x	x	c	Clock the data register after entering phase two. Now the register data is current but latch #10 still has a 0 inside.
c	x	x	0	Load all the latches with their functional results.
This completes phase two. Return to phase one and load the next set of input data, while simultaneously verifying the scan out pin. We expect to see latches 9, 10, and 11 with ones as we scan the data out.				
c	x	x	x	Load a "don't care" into latch #1, not used.
c	1	x	x	Load a 1 into Scan In pin, knowing it will be positioned in latch #2, input B.
c	x	x	x	Load a "don't care" into latch #3, not used.
c	x	x	x	Load a "don't care" into latch #4, not used.
c	x	x	x	Load a "don't care" into latch #5, not used.
c	0	x	x	Load a 0 into Scan In pin for input A (latch #6). This is a different from the first load.
c	x	x	x	Load a "don't care" into latch #7, not used.
c	x	x	x	Load a "don't care" into latch #8, not used.
c	1	1	x	Load a 1 into latch #9, expecting the G output to be a 0 after phase two. The Scan out pin will be showing the results of latch #9 from the previous load.
c	0	1	x	Load a 0 into latch #10, expecting the register output to be a 1 after phase two. The Scan out pin shows latch #10 results.
c	0	1	x	Load a 0 into latch #11, expecting the F output to be a 1 after phase two. The Scan out pin shows latch #11 results.

Figure 18. Sample Test Vectors for Simple Design Example

XC3300 Family Configuration Pin Assignments

CONFIGURATION MODE: <M0>		68	** 84	** 100	132	160	175	USER
SLAVE <1>	MASTER < 0>	PLCC	PLCC	PQFP	PGA	PQFP	PPGA	OPERATION
PWR DWN (I)	PWR DWN (I)	10	12	29	A1	159	B2	PWR DWN (I)
VCC	VCC	18	22	41	C8	20	D9	VCC
M1 (I)	M1 (I)	25	31	52	B13	40	B14	M1
M0 (HIGH) (I)	M0 (LOW) (I)	26	32	54	A14	42	B15	M0 (I)
		27	33	56	C13	44	C15	I/O
HDC (HIGH)	HDC (HIGH)	28	34	57	B14	45	E14	I/O
LDC (LOW)	LDC (LOW)	30	36	59	D14	49	D16	I/O
INIT *	INIT *	34	42	65	G14	59	H15	I/O
GND	GND	35	43	66	H12	19	J14	GND
		43	53	76	M13	76	P15	XTL2 OR I/O
RESET (I)	RESET (I)	44	54	78	P14	78	R15	RESET (I)
DONE	DONE	45	55	80	N13	80	R14	PROGRAM (I)
		46	56	81	M12	81	N13	I/O
		47	57	82	P13	82	T14	XTL1 OR I/O
		48	58	83	N11	86	P12	I/O
		49	60	87	M9	92	T11	I/O
		50	61	88	N9	93	R10	I/O
		51	62	89	N8	98	R9	I/O
VCC	VCC	52	64	91	M8	100	N9	VCC
		53	65	92	N7	102	P8	I/O
		54	66	93	P6	103	R8	I/O
		55	67	94	M6	108	R7	I/O
		56	70	98	M5	114	R5	I/O
		57	71	99	N4	115	P5	I/O
DIN (I)	DIN (I)	58	72	100	N2	119	R3	I/O
DOUT	DOUT	59	73	1	M3	120	N4	I/O
CCLK (I)	CCLK	60	74	2	P1	121	R2	CCLK (I)
		61	75	5	M2	124	P2	I/O
		62	76	6	N1	125	M3	I/O
		63	77	8	L2	128	P1	I/O
		64	78	9	L1	129	N1	I/O
		65	81	12	K1	132	M1	I/O
		66	82	13	J2	133	L2	I/O
		67	83	14	H1	136	K2	I/O
		68	84	15	H2	137	K1	I/O
GND	GND	1	1	16	H3	139	J3	GND
		2	2	17	G2	141	H2	I/O
		3	3	18	G1	142	H1	I/O
		4	4	19	F2	147	F2	I/O
		5	5	20	E1	148	E1	I/O
		6	8	23	D1	151	D1	I/O
		7	9	24	D2	152	C1	I/O
		8	10	25	B1	155	E3	I/O
		9	11	26	C2	156	C2	I/O
		X	X	X				XC3330
		X	X	X				XC3342
			X**	X**	X	X	X	XC3390

AVAILABLE PACKAGES

REPRESENTS A 50-kΩ TO 100-kΩ PULL-UP

* INIT IS AN OPEN DRAIN OUTPUT DURING CONFIGURATION

(I) REPRESENTS AN INPUT

** PIN ASSIGNMENTS FOR THE XC3390 DIFFER FROM THOSE SHOWN. SEE PAGE 22.

X1348

Note: Pin assignments of "PGA Footprint" PLCC sockets and PGA packages are not electically identical.
Generic I/O pins are not shown

XC3000 FAMILY PIN ASSIGNMENTS

Xilinx offers the three members of the XC3300 family in a variety of surface-mount and through-hole package types, with pin counts from 68 to 175.

Each chip is offered in several package types to accomodate the available pc board space and manufacturing technology. Most package types are also offered with different chips to accomodate design changes without the need for pc board changes.

Note that there may not be a perfect match between the number of bonding pads on the chip and the number of pins on a package. In some cases, the chip has more pads than there are pins on the package, as indicated by the information ("unused" pads) below the line in the following table. The IOBs of the unconnected pads can still be used as storage elements if the specified propagation delays and set-up times are acceptable.

In other cases, the chip has fewer pads than there are pins on the package; therefore, some package pins are not connected (n.c.), as shown above the line in the following table.

		Number of Package Pins					
Device	**Pads**	**68**	**84**	**100**	**132**	**160**	**175**
XC3330	98	30 unused	14 unused	2 n.c.	—	—	—
XC3342	118	—	34 unused	18 unused	—	—	—
XC3090	166	—	82 unused	—	32 unused	6 unused	9 n.c.

PIN DESCRIPTIONS

Permanently Dedicated Pins.

V_{CC}
Two to eight (depending on package type) connections to the nominal +5 V supply voltage. All must be connected.

GND
Two to eight (depending on package type) connections to ground. All must be connected.

$\overline{PWRDWN}$
A Low on this CMOS-compatible input stops all internal activity. All flip-flops and latches are reset, all outputs are 3-stated, and all inputs are interpreted as High, independent of their actual level. While $\overline{PWRDWN}$ is Low, V_{CC} may be reduced to any value >2.3 V. When $\overline{PWDWN}$ returns High, the LCA becomes operational with DONE Low for two cycles of the internal 1-MHz clock. During configuration, $\overline{PWRDWN}$ must be High. If not used, $\overline{PWRDWN}$ must be tied to V_{CC}.

$\overline{RESET}$
This is an active Low input which has three functions.

Prior to the start of configuration, a Low input will delay the start of the configuration process. An internal circuit senses the application of power and begins a minimal time-out cycle. When the time-out and $\overline{RESET}$ are complete, the level of the M0 line is sampled and configuration begins.

If $\overline{RESET}$ is asserted during a configuration, the LCA device is re-initialized and restarts the configuration at the termination of $\overline{RESET}$.

If $\overline{RESET}$ is asserted after configuration is complete, it provides a global asynchronous reset of all IOB and CLB storage elements of the LCA device.

CCLK
During configuration, Configuration Clock is an output of an LCA in Master mode or Peripheral mode, but an input in Slave mode.

CCLK drives dynamic circuitry inside the LCA. The Low time may, therefore, not exceed a few microseconds. When used as an input, CCLK must be "parked High". An internal pull-up resistor maintains High when the pin is not being driven.

DONE/$\overline{PROG}$
DONE is an open-drain output, configurable with or without an internal pull-up resistor. At the completion of configuration, the LCA circuitry becomes active in a synchronous order, and DONE/$\overline{PROG}$ goes active High one cycle before the outputs go active.

Once configuration is done, a High-to-Low transition of this pin will cause an initialization of the LCA and start a reconfiguration.

M0
As Mode 0, this input sampled is before the start of configuration to establish the configuration mode to be used.

M1
This input is used only for manufacturer test. The user must tie this pin either High or Low in-system.

User I/O Pins that can have special functions.

HDC
During configuration, this output is held at a High level to indicate that configuration is not yet complete. After configuration, this pin is a user-programmable I/O pin.

$\overline{\text{LDC}}$
During Configuration, this output is held at a Low level to indicate that the configuration is not yet complete. After configuration, this pin is a user-programmable I/O pin. $\overline{\text{LDC}}$ is particularly useful in Master mode as a Low enable for an EPROM, but it must then be programmed as a High after configuration.

$\overline{\text{INIT}}$
This is an active Low open-drain output which is held Low during the power stabilization and internal clearing of the configuration memory. It can be used to indicate status to a configuring microprocessor, as a wired AND of several slave mode devices, or as a hold-off signal for a master mode device. After configuration this pin becomes a user programmable I/O pin.

BCLKIN
This is a direct CMOS level input to the alternate clock buffer (Auxiliary Buffer) in the lower right corner.

XTL1
This user I/O pin can be used to operate as the output of an amplifier driving an external crystal and bias circuitry.

XTL2
This user I/O pin can be used as the input of an amplifier connected to an external crystal and bias circuitry. The I/O Block is left unconfigured. The oscillator configuration is activated by routing a net from the oscillator buffer symbol output.

DIN
During Slave or Master Serial configuration, this pin is used as a serial-data input.

DOUT
During configuration this pin is used to output serial-configuration data to the DIN pin of a daisy-chained slave.

TCLKIN
This is a direct CMOS level input to the global clock buffer.

Unrestricted User I/O Pins.

I/O
An I/O pin may be programmed by the user to be an Input or an Output pin following configuration. All unrestricted I/O pins, plus the special pins mentioned previously, have a weak pull-up resistor of 50 kΩ to 100 kΩ that becomes active as soon as the device powers up, and stays active until the end of configuration.

XC3300 Family 68-Pin and 84-Pin PLCC Pinouts

XC-3330, XC-3342	68 PLCC	84 PLCC
PWRDN	10	12
TCLKIN-I/O	11	13
I/O		14
I/O	12	15
I/O	13	16
I/O	—	17
I/O	14	18
I/O	15	19
I/O	16	20
I/O	17	21
VCC	18	22
I/O	19	23
I/O	—	24
I/O	20	25
I/O	21	26
I/O	22	27
I/O	—	28
I/O	23	29
I/O	24	30
M1	25	31
M0	26	32
I/O	27	33
HDC-I/O	28	34
I/O	29	35
LDC-I/O	30	36
I/O	31	37
I/O		38
I/O	32	39
I/O	33	40
I/O		41
INIT-I/O	34	42
GND	35	43
I/O	36	44
I/O	37	45
I/O	38	46
I/O	39	47
I/O	40	48
I/O	41	49
I/O		50
I/O		51
I/O	42	52
XTL2(IN)-I/O	43	53

XC-3330, XC-3342	68 PLCC	84 PLCC
RESET	44	54
DONE-PG	45	55
I/O	46	56
XTL1(OUT)-BCLKIN-I/O	47	57
I/O	48	58
I/O	—	59
I/O	49	60
I/O	50	61
I/O	51	62
I/O	—	63
VCC	52	64
I/O	53	65
I/O	54	66
I/O	55	67
I/O	—	68
I/O		69
I/O	56	70
I/O	57	71
DIN-I/O	58	72
DOUT-I/O	59	73
CCLK	60	74
I/O	61	75
I/O	62	76
I/O	63	77
I/O	64	78
I/O		79
I/O		80
I/O	65	81
I/O	66	82
I/O	67	83
I/O	68	84
GND	1	1
I/O	2	2
I/O	3	3
I/O	4	4
I/O	5	5
I/O		6
I/O		7
I/O	6	8
I/O	7	9
I/O	8	10
I/O	9	11

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

This table describes the pinouts of two different chips in two different packages. The first column lists 84 of the 118 pads on the XC3342 (and 84 of the 98 pads on the XC3330) that are connected to the 84 package pins. Six pads, indicated by a dash (–) in the 68 PLCC column, have no connections in the 68 PLCC package, but are connected in the 84-pin package. (See table on page 16.)

XC3390 84-Pin PLCC Pinout

PLCC Pin Number	XC3390
12	PWRDN
13	TCLKIN-I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	GND*
22	VCC
23	I/O
24	I/O
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	M1
32	M0
33	I/O
34	HDC-I/O
35	I/O
36	LDC-I/O
37	I/O
38	I/O
39	I/O
40	I/O
41	INIT/I/O*
42	VCC*
43	GND
44	I/O
45	I/O
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	I/O
53	XTL2(IN)-I/O

PLCC Pin Number	XC3390
54	RESET
55	DONE-PG
56	I/O
57	XTL1(OUT)-BCLKIN-I/O
58	I/O
59	I/O
60	I/O
61	I/O
62	I/O
63	I/O
64	VCC
65	GND*
66	I/O*
67	I/O*
68	I/O*
69	I/O
70	I/O
71	I/O
72	DIN-I/O
73	DOUT-I/O
74	CCLK
75	I/O
76	I/O
77	I/O
78	I/O
79	I/O
80	I/O
81	I/O
82	I/O
83	I/O
84	I/O
1	GND
2	VCC*
3	I/O*
4	I/O*
5	I/O*
6	I/O*
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs.
Programmed ouptuts are default slew-rate limited. DEVICE POWER MUST BE LESS THAN 1 WATT.

* Different pin definition than XC3342 PC84 package

XC3300 Family 100-Pin PQFP Pinouts

PQFP Pin No.	XC3330 XC3342
16	GND
17	I/O
18	I/O
19	I/O
20	I/O
21	I/O
22	I/O
23	I/O
24	I/O
25	I/O
26	I/O
27	VCC
28	GND
29	$\overline{\text{PWRDN}}$
30	TCLKIN-I/O
31	I/O**
32	I/O
33	I/O
34	I/O
35	I/O
36	I/O
37	I/O
38	I/O
39	I/O
40	I/O
41	VCC
42	I/O
43	I/O
44	I/O
45	I/O
46	I/O
47	I/O
48	I/O
49	I/O

PQFP Pin No.	XC3330 XC3342
50	I/O
51	I/O
52	M1
53	GND
54	M0
55	VCC
56	I/O
57	HDC-I/O
58	I/O
59	$\overline{\text{LDC}}$-I/O
60	I/O
61	I/O
62	I/O
63	I/O
64	I/O
65	$\overline{\text{INIT}}$-I/O
66	GND
67	I/O
68	I/O
69	I/O
70	I/O
71	I/O
72	I/O
73	I/O
74	I/O
75	I/O
76	XTAL2-I/O
77	GND
78	$\overline{\text{RESET}}$
79	VCC
80	DONE-$\overline{\text{PG}}$
81	I/O
82	BCLKIN-XTAL1-I/O
83	I/O

PQFP Pin No.	XC3330 XC3342
84	I/O
85	I/O
86	I/O
87	I/O
88	I/O
89	I/O
90	I/O
91	VCC
92	I/O
93	I/O
94	I/O
95	I/O
96	I/O
97	I/O
98	I/O
99	I/O
100	DIN-I/O
1	DOUT-I/O
2	CCLK
3	VCC
4	GND
5	I/O
6	I/O
7	I/O**
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs.
Programmed outputs are default slew-rate limited.

This table describes the pinouts of two different chips in two different packages. The second column lists 100 of the 118 pads on the XC3342 that are connected to the 100 package pins. Two pads, indicated by double asterisks, do not exist on the XC3330, which has 98 pads; therefore the corresponding pins have no connections.

XC3300 Family 132-Pin Plastic PGA Pinout

PGA Pin Number	XC-3390	PGA Pin Number	XC-3390	PGA Pin Number	XC-3390	PGA Pin Number	XC-3390
C4	GND	B13	M1	P14	RESET	M3	DOUT-I/O
A1	PWRDN	C11	GND	M11	VCC	P1	CCLK
C3	I/O-TCLKIN	A14	M0	N13	DONE-PG	M4	VCC
B2	I/O	D12	VCC	M12	I/O	L3	GND
B3	I/O	C13	I/O	P13	XTAL1-I/O-BCLKIN	M2	I/O
A2	I/O	B14	HDC-I/O	N12	I/O	N1	I/O
B4	I/O	C14	I/O	P12	I/O	M1	I/O
C5	I/O	E12	I/O	N11	I/O	K3	I/O
A3	I/O	D13	I/O	M10	I/O	L2	I/O
A4	I/O	D14	LDC-I/O	P11	I/O	L1	I/O
B5	I/O	E13	I/O	N10	I/O	K2	I/O
C6	I/O	F12	I/O	P10	I/O	J3	I/O
A5	I/O	E14	I/O	M9	I/O	K1	I/O
B6	I/O	F13	I/O	N9	I/O	J2	I/O
A6	I/O	F14	I/O	P9	I/O	J1	I/O
B7	I/O	G13	I/O	P8	I/O	H1	I/O
C7	GND	G14	INIT-I/O	N8	I/O	H2	I/O
C8	VCC	G12	VCC	P7	I/O	H3	GND
A7	I/O	H12	GND	M8	VCC	G3	VCC
B8	I/O	H14	I/O	M7	GND	G2	I/O
A8	I/O	H13	I/O	N7	I/O	G1	I/O
A9	I/O	J14	I/O	P6	I/O	F1	I/O
B9	I/O	J13	I/O	N6	I/O	F2	I/O
C9	I/O	K14	I/O	P5	I/O	E1	I/O
A10	I/O	J12	I/O	M6	I/O	F3	I/O
B10	I/O	K13	I/O	N5	I/O	E2	I/O
A11	I/O	L14	I/O	P4	I/O	D1	I/O
C10	I/O	L13	I/O	P3	I/O	D2	I/O
B11	I/O	K12	I/O	M5	I/O	E3	I/O
A12	I/O	M14	I/O	N4	I/O	C1	I/O
B12	I/O	N14	I/O	P2	I/O	B1	I/O
A13	I/O	M13	XTAL2(IN)-I/O	N3	I/O	C2	I/O
C12	I/O	L12	GND	N2	DIN-I/O	D3	VCC

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs.
Programmed outputs are default slew-rate limited.

XC3300 Family 160-Pin PQFP Pinout

PLCC Pin Number	XC3390
1	I/O
2	I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	GND
20	VCC
21	I/O
22	I/O
23	I/O
24	I/O
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O
36	I/O
37	I/O
38	I/O
39	I/O
40	M1

PLCC Pin Number	XC3390
41	GND
42	M0
43	VCC
44	I/O
45	HDC-I/O
46	I/O
47	I/O
48	I/O
49	$\overline{\text{LDC}}$-I/O
50	I/O
51	I/O
52	I/O
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	I/O
59	$\overline{\text{INIT}}$-I/O
60	VCC
61	GND
62	I/O
63	I/O
64	I/O
65	I/O
66	I/O
67	I/O
68	I/O
69	I/O
70	I/O
71	I/O
72	I/O
73	I/O
74	I/O
75	I/O
76	XTAL2-I/O
77	GND
78	$\overline{\text{RESET}}$
79	VCC
80	DONE/$\overline{\text{PG}}$

PLCC Pin Number	XC3390
81	I/O
82	XTAL1-I/O-BCLKIN
83	I/O
84	I/O
85	I/O
86	I/O
87	I/O
88	I/O
89	I/O
90	I/O
91	I/O
92	I/O
93	I/O
94	I/O
95	I/O
96	I/O
97	I/O
98	I/O
99	I/O
100	VSS
101	GND
102	I/O
103	I/O
104	I/O
105	I/O
106	I/O
107	I/O
108	I/O
109	I/O
110	I/O
111	I/O
112	I/O
113	I/O
114	I/O
115	I/O
116	I/O
117	I/O
118	I/O
119	DIN-I/O
120	DOUT

PLCC Pin Number	XC3390
121	CCLK
122	VCC
123	GND
124	I/O
125	I/O
126	I/O
127	I/O
128	I/O
129	I/O
130	I/O
131	I/O
132	I/O
133	I/O
134	I/O
135	I/O
136	I/O
137	I/O
138	I/O
139	GND
140	VCC
141	I/O
142	I/O
143	I/O
144	I/O
145	I/O
146	I/O
147	I/O
148	I/O
149	I/O
150	I/O
151	I/O
152	I/O
153	I/O
154	I/O
155	I/O
156	I/O
157	VCC
158	GND
159	$\overline{\text{PWRDWN}}$
160	TCLKIN-I/O

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs.
Programmed IOBs are default slew-rate limited.

XC3300 Family 175-Pin Plastic PGA Pinout

PGA Pin Number	XC-3390	PGA Pin Number	XC-3390	PGA Pin Number	XC-3390	PGA Pin Number	XC-3390
B2	PWRDN	D13	I/O	R14	DONE-PG	R3	DIN-I/O
D4	TCLKIN-I/O	B14	M1	N13	I/O	N4	DOUT-I/O
B3	I/O	C14	GND	T14	XTAL1(OUT)-BCLKIN-I/O	R2	CCLK
C4	I/O	B15	M0	P13	I/O	P3	VCC
B4	I/O	D14	VCC	R13	I/O	N3	GND
A4	I/O	C15	I/O	T13	I/O	P2	I/O
D5	I/O	E14	HDC-I/O	N12	I/O	M3	I/O
C5	I/O	B16	I/O	P12	I/O	R1	I/O
B5	I/O	D15	I/O	R12	I/O	N2	I/O
A5	I/O	C16	I/O	T12	I/O	P1	I/O
C6	I/O	D16	LDC-I/O	P11	I/O	N1	I/O
D6	I/O	F14	I/O	N11	I/O	L3	I/O
B6	I/O	E15	I/O	R11	I/O	M2	I/O
A6	I/O	E16	I/O	T11	I/O	M1	I/O
B7	I/O	F15	I/O	R10	I/O	L2	I/O
C7	I/O	F16	I/O	P10	I/O	L1	I/O
D7	I/O	G14	I/O	N10	I/O	K3	I/O
A7	I/O	G15	I/O	T10	I/O	K2	I/O
A8	I/O	G16	I/O	T9	I/O	K1	I/O
B8	I/O	H16	I/O	R9	I/O	J1	I/O
C8	I/O	H15	INIT-I/O	P9	I/O	J2	I/O
D8	GND	H14	VCC	N9	VCC	J3	GND
D9	VCC	J14	GND	N8	GND	H3	VCC
C9	I/O	J15	I/O	P8	I/O	H2	I/O
B9	I/O	J16	I/O	R8	I/O	H1	I/O
A9	I/O	K16	I/O	T8	I/O	G1	I/O
A10	I/O	K15	I/O	T7	I/O	G2	I/O
D10	I/O	K14	I/O	N7	I/O	G3	I/O
C10	I/O	L16	I/O	P7	I/O	F1	I/O
B10	I/O	L15	I/O	R7	I/O	F2	I/O
A11	I/O	M16	I/O	T6	I/O	E1	I/O
B11	I/O	M15	I/O	R6	I/O	E2	I/O
D11	I/O	L14	I/O	N6	I/O	F3	I/O
C11	I/O	N16	I/O	P6	I/O	D1	I/O
A12	I/O	P16	I/O	T5	I/O	C1	I/O
B12	I/O	N15	I/O	R5	I/O	D2	I/O
C12	I/O	R16	I/O	P5	I/O	B1	I/O
D12	I/O	M14	I/O	N5	I/O	E3	I/O
A13	I/O	P15	XTAL2(IN)-I/O	T4	I/O	C2	I/O
B13	I/O	N14	GND	R4	I/O	D3	VCC
C13	I/O	R15	RESET	P4	I/O	C3	GND
A14	I/O	P14	VCC				

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs.
Programmed outputs are default slew-rate limited.

Pins A2, A3, A15, A16, T1, T2, T3, T15 and T16 are not connected.
Pin A1 does not exist.

ABSOLUTE MAXIMUM RATINGS

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	–0.5 to 7.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to Vcc + 0.5	V
V_{TS}	Voltage applied to three-state output	–0.5 to Vcc + 0.5	V
T_{STG}	Storage temperature (ambient)	–65 to + 150	°C
T_{SOL}	Maximum soldering temperature (10 sec @ 1/16 in.)	+ 260	°C
T_J	Junction temperature plastic	+ 125	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

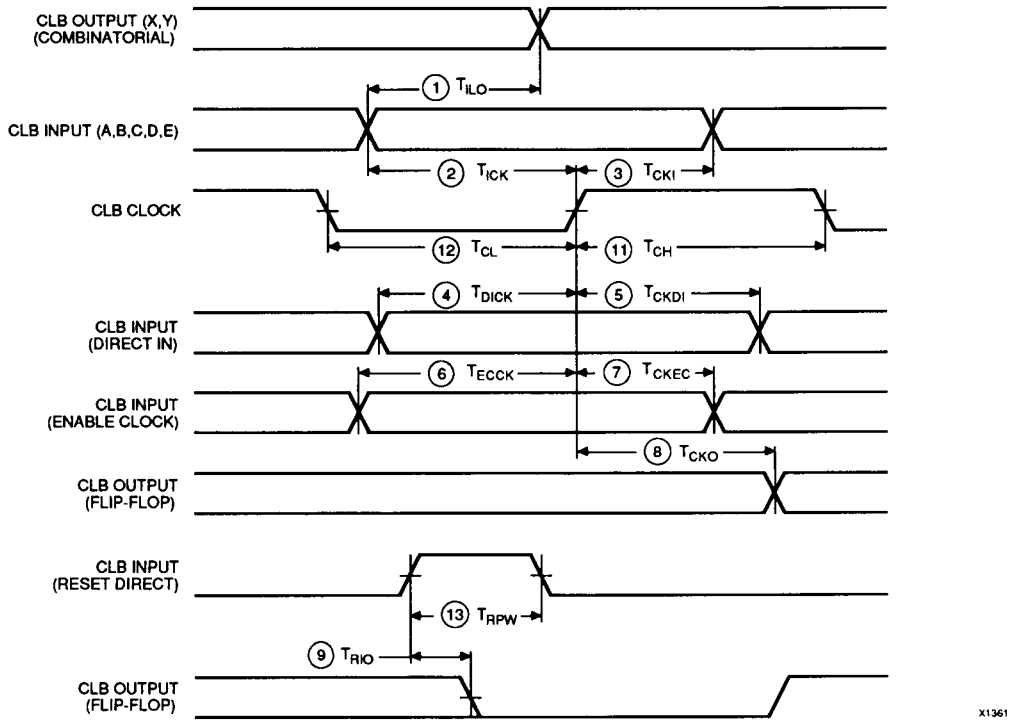
Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial 0°C to 70°C	4.75	5.25	V
V_{IHT}	High-level input voltage — TTL configuration	2.0	Vcc	V
V_{ILT}	Low-level input voltage — TTL configuration	0	0.8	V
V_{IHC}	High-level input voltage — CMOS configuration	70%	100%	Vcc
V_{ILC}	Low-level input voltage — CMOS configuration	0	20%	Vcc
T_{IN}	Input signal transition time		250	ns

DC CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

Symbol	Descirption		Min	Max	Units
V_{OH}	High-level output voltage (@ I_{OH} = –4.0 mA, V_{CC} min)	Commercial	3.86		V
V_{OL}	Low-level output voltage (@ I_{OL} = 4.0 mA, V_{CC} min)			0.32	V
I_{CCPD}	Power-down supply current (V_{CC} = 5.0 V @ 70°C)	XC3330		80	µA
		XC3342		120	µA
		XC3390		250	µA
I_{CCO}	Quiescent LCA supply current in addition to I_{CCPD}[1]				
	Chip thresholds programmed as CMOS levels			500	µA
	Chip thresholds programmed as TTL levels			10	mA
I_{IL}	Input Leakage Current		–10	+10	µA
C_{IN}	Input capacitance, all packages except PGA 175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2			 10 15	 pF pF
	Input capacitance, PGA 175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2			 15 20	 pF pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0V (sample tested)		0.02	0.17	mA
I_{RLL}	Horizontal long line pull-up (when selected) @ logic LOW		0.4	3.4	mA

Note: 1. With no output current loads, no active input or long line pull-up resistors, all package pins at Vcc or GND.

CLB SWITCHING CHARACTERISTIC GUIDELINES



BUFFER (Internal) SWITCHING CHARACTERISTIC GUIDELINES

Description	Symbol		Min	Max	Units
Global and Alternate Clock Distribution					
Either: **Normal** IOB input pad to clock buffer input	TPID			4	ns
Or: **Fast** (CMOS only) input pad to clock buffer input	TPIDC			2	ns
Plus: Clock buffer input to any clock k**				5	ns
TBUF driving a Horizontal Longline (L.L.)**					
I to L.L. while T is Low (buffer active)	TIO			4	ns
T↓ to L.L. active and valid	TON			7	ns
T↑ to L.L. (inactive) with single pull-up resistor	TPUS			14	ns
with pair of pull-up resistors	TPUF			7	ns
BIDI					
Bi-directional buffer delay				3	ns

** Timing is based on the XC3020, for other devices see XACT timing calculator.

CLB SWITCHING CHARACTERISTIC GUIDELINES (Continued)

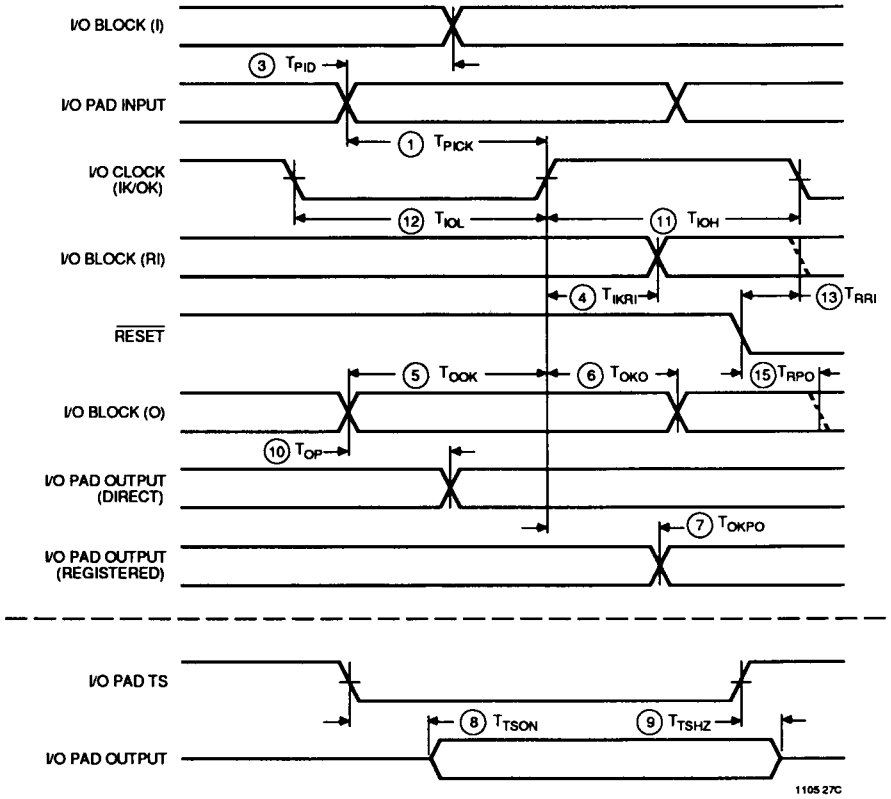
Testing of the switching characteristic guidelines is modeled after testing specified by MIL-M-38510/605. Devices are 100% functionally tested. Benchmark timing patterns are used to provide correlation to the switching characteristic guideline values. Actual worst-case timing is provided by the XACT Timing calculator or Simulation modeling.

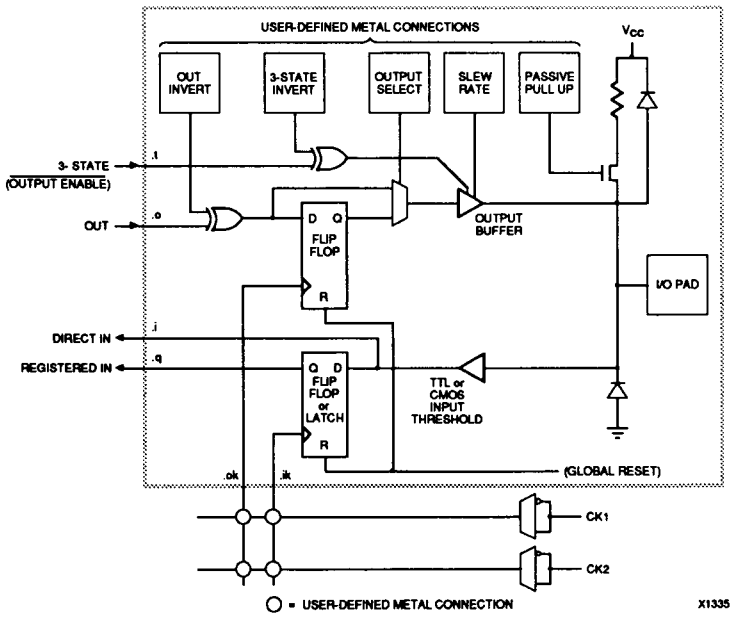
	Speed Grade			-100		Units
Description	Symbol			Min	Max	
Combinatorial Delay						
Logic Variables a, b, c, d, e, to outputs x, y	1	T_{ILO}			7	ns
Sequential delay						
Clock k to outputs x, y	8	T_{CKO}			7	ns
Clock k to outputs x,y when Q is returned through function generators F or G to drive x, y					12	ns
Set-up time before clock K						
Logic Variables a, b, c, d, e	2	T_{ICK}		7		ns
Data In di	4	T_{DICK}		4		ns
Enable Clock ec	6	T_{ECCK}		5		ns
Reset Direct inactive rd				1		ns
Hold Time after clock k						
Logic Variables a, b, c, d, e	3	T_{CKI}		0		ns
Data In di	5	T_{CKDI}		2		ns
Enable Clock ec	7	T_{CKEC}		0		ns
Clock						
Clock High time*	11	T_{CH}		5		ns
Clock Low time*	12	T_{CL}		5		ns
Max. flip-flop toggle rate*		F_{CLK}		100		MHz
Reset Direct (rd)						
rd width	13	T_{RPW}		7		ns
delay from rd to outputs x, y	9	T_{RIO}			7	ns
Master Reset (MR)						
MR width		T_{MRW}		21		ns
delay from MR to outputs x, y		T_{MRQ}			17	ns

* These timing limits are based on calculations.

Note: The CLB K to Q output delay (TCKO, #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold time requirement (TCKD1, #5) of any CLB on the same die.

IOB SWITCHING CHARACTERISTIC GUIDELINES





IOB SWITCHING CHARACTERISTIC GUIDELINES (Continued)

Testing of the switching characteristic guidelines is modeled after testing specified by MIL-M-38510/605. Devices are 100% functionally tested. Benchmark timing patterns are used to provide correlation to the switching charcteristic guideline values. Actual worst-case timing is provided by the XACT Timing calculator or Simulation modeling.

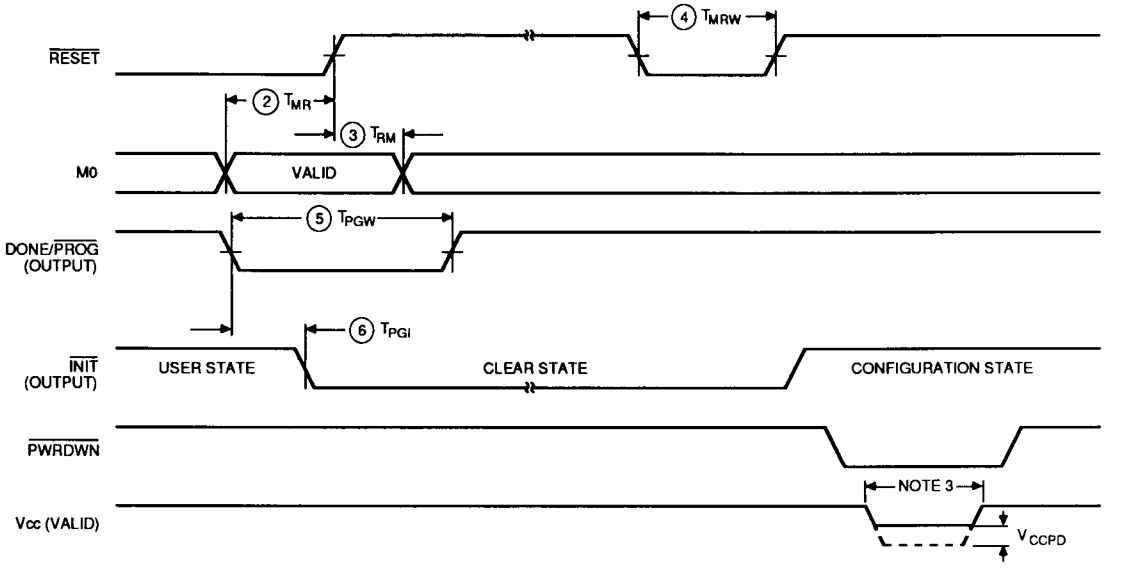
				-100		Units
Description	Symbol			Min	Max	
Propagation Delays (Input)						
Pad to Direct In (i)	3	TPID			4	ns
Pad to Registered In (q) with latch transparent		TPTG			17	ns
Clock (ik) to Registered In (q)	4	TIKRI			6	ns
Set-up Time (Input)						
Pad to Clock (ik) set-up time	1	TPICK		17		ns
Propagation Delays (Output)						
Clock (ok) to Pad (fast)	7	TOKPO			10	ns
(slew rate limited)	7	TOKPO			27	ns
Output (o) to Pad (fast)	10	TOPF			6	ns
(slew-rate limited)	10	TOPS			23	ns
Three-state to Pad begin hi-Z (fast)	9	TTSHZ			8	ns
(slew-rate limited)	9	TTSHZ			25	ns
Three state to Pad active and valid (fast)	8	TTSON			12	ns
(slew -rate limited)	8	TTSON			29	ns
Set-up and Hold Times (Output)						
Output (o) to clock (ok) set-up time	5	TOOK		9		ns
Output (o) to clock (ok) hold time	6	TOKO		0		ns
Clock						
Clock High time	11	TCH		5		ns
Clock Low time	12	TCL		5		ns
Max. flip-flop toggle rate		FCLK		100		MHz
Master Reset Delays						
$\overline{\text{RESET}}$ Pad to Registered In (q)	13	TRRI			20	ns
$\overline{\text{RESET}}$ Pad to output pad	15	TRPO			28	ns

Notes: 1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture).
Typical fast mode output rise/fall times are 2 ns and will increase approximately 2%/pF of additional load.
Typical slew rate limited output rise/fall times are approximately 4 times longer.
A maximum total external capacitive load for simultaneous fast mode switching in the same direction is 500 pF per power/ground pin pair. For slew-rate limited outputs this total is 4 times larger.

2. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.

3. Input pad set-up time is specified with respect to the internal clock (.ik)
In order to calculate system set-up time, subtract clock delay (pad to ik) from the input pad set-up time value.
Input pad holdtime with respect to the internal clock (ik) is negative. This means that pad level changes immediately before the internal clock edge (ik) will not be recognized.
For a more detailed description see the discussion on "LCA Performance" in the Applications chapter of the *Xilinx Programmable Gate Array Data Book*.

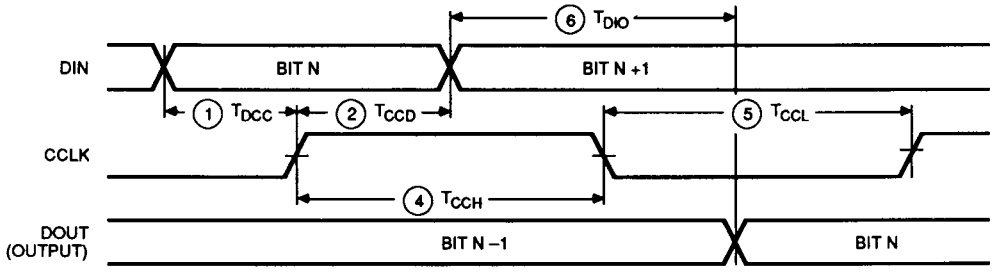
GENERAL LCA SWITCHING CHARACTERISTICS



								-100		Units
	Description	Symbol						Min	Max	
RESET (2)	M0 setup time required	2	TMR					1		µs
	M0 hold time required	3	TRM					1		µs
	RESET Width (Low) req. for Abort	4	TMRW					6		µs
DONE/PROG(4)	Width (Low) required for Re-config.	5	TPGW					6		µs
(D/P)	INIT response after D/P is pulled Low	6	TPGI						7	µs
PWRDWN (3)	Power Down Vcc		VCCPD					2.3		V

Notes: 1. At power-up, Vcc must rise from 2.0 V to Vcc min in less than 25 ms. If this is not possible, configuration can be delayed by holding RESET Low until Vcc has reached 4.0 V. A very long Vcc rise time of >100 ms, or a non-monotonically rising Vcc may require a RESET pulse (High-to-Low-to-High) of >6 µs duration after Vcc has reached 4.0 V.
2. RESET timing relative to valid mode lines (M0) is relevant when RESET is used to delay configuration.
3. PWRDWN transitions must occur during operational Vcc levels.
4. After completion of configuration, D/P pin is released and must be pulled High within 400 ns max.
5. If the internal D/P pull-up is used, the loading on the D/P pin should be no more than 50pf to meet the rise time specification. Otherwise, use an external pull-up.

SLAVE MODE PROGRAMMING SWITCHING CHARACTERISTICS

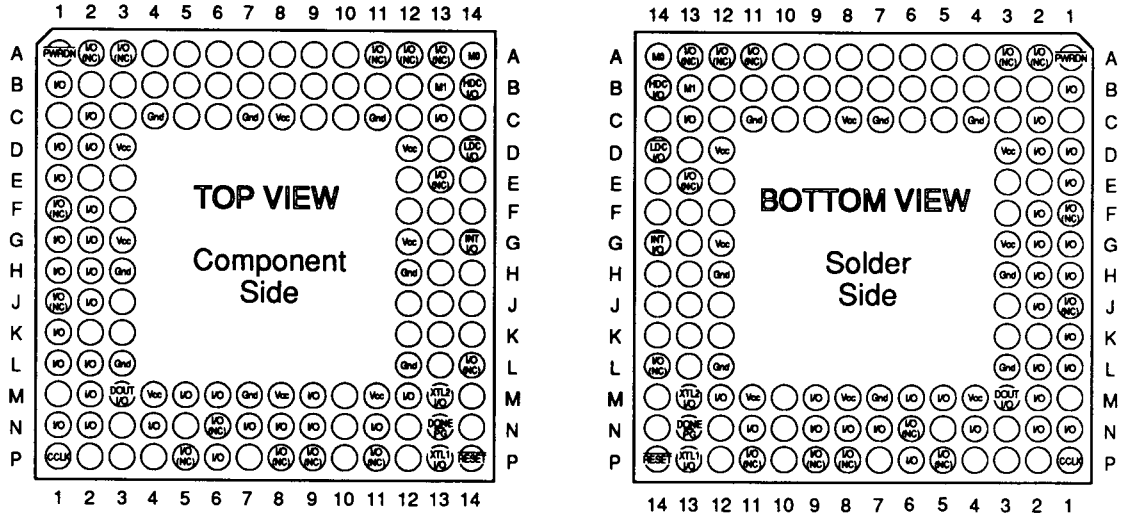


X1360

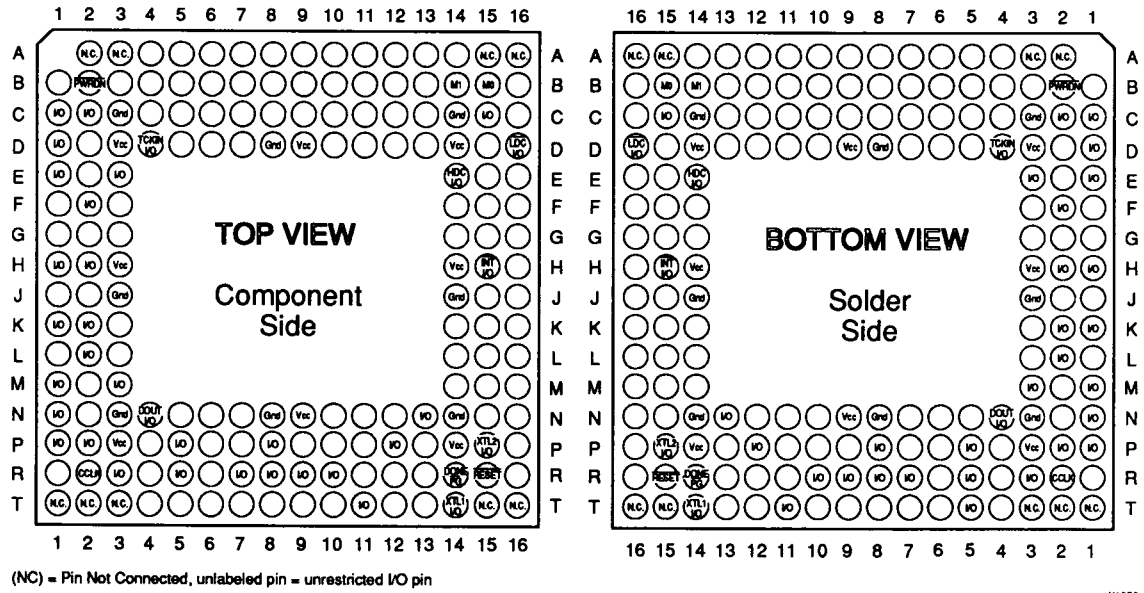
	Description	Symbol		Min	Rec	Max	Units
CCLK	High time	4	TCCH	0.5	0.5		µs
	Low time	5	TCCL	0.3	0.5	1.0	µs
	Frequency		FCC	0.5	1.0	1.5	MHz
	DIN to DOUT*	6	TDIO			50	ns

Note: Configuration must be delayed until the $\overline{\text{INIT}}$ of all LCAs is HIGH.

PGA PIN-OUTS



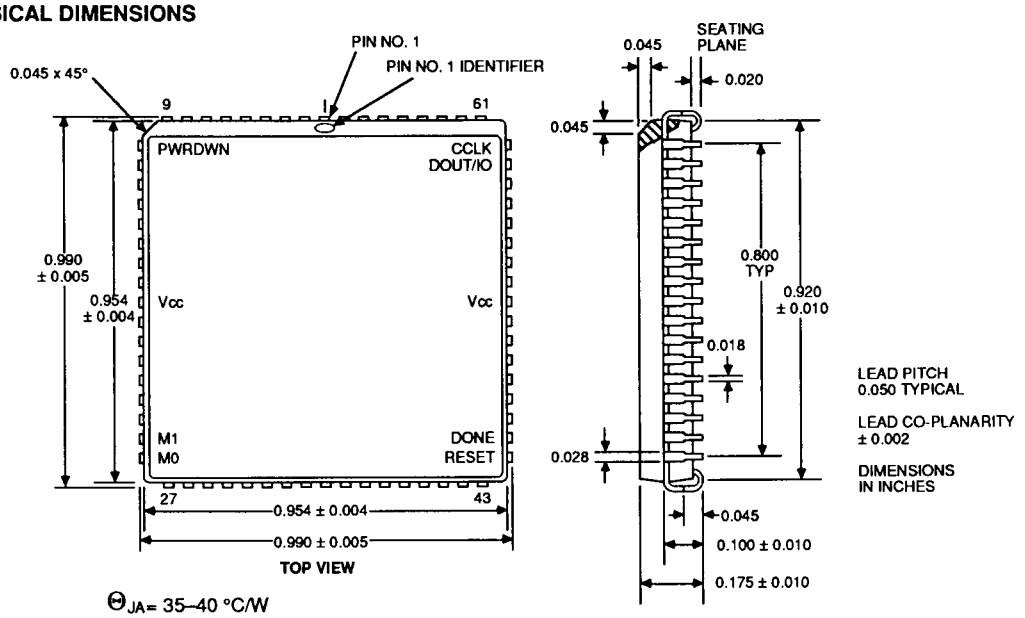
PG132 Pin-out – XC3390-PP



(NC) = Pin Not Connected, unlabeled pin = unrestricted I/O pin

PG175 Pin-out – XC3390-PP

PHYSICAL DIMENSIONS

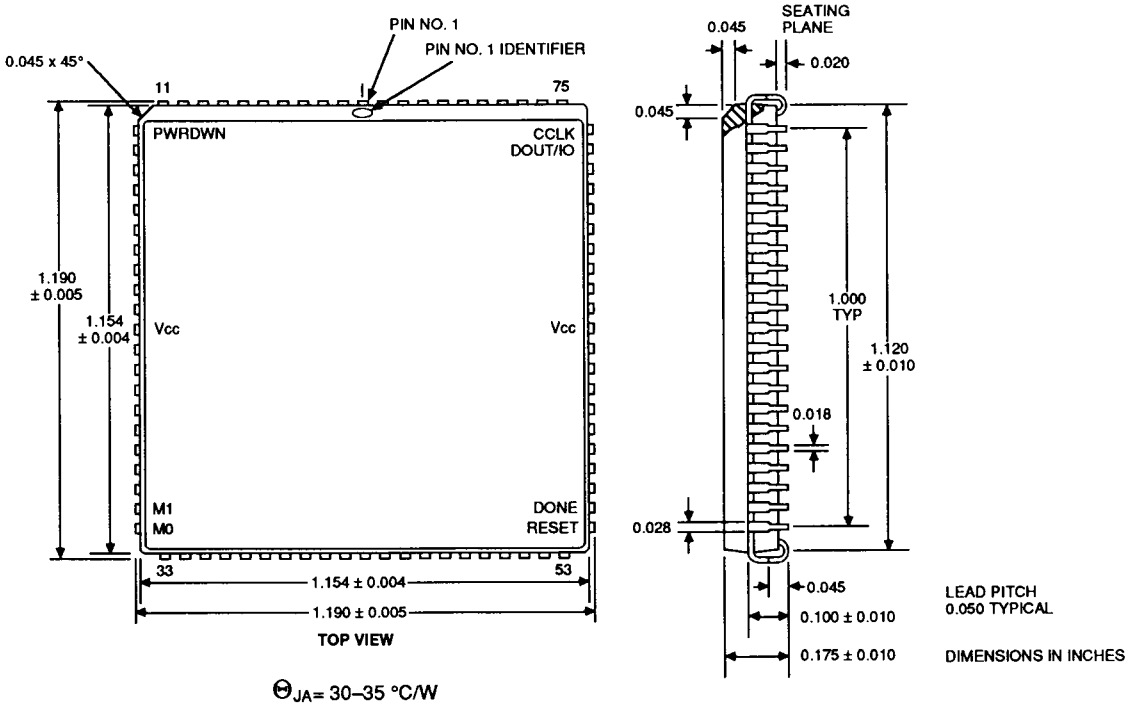


Θ_{JA}= 35–40 °C/W

Θ_{JC}= 7–10 °C/W

1105 34C

68-Pin PLCC Package



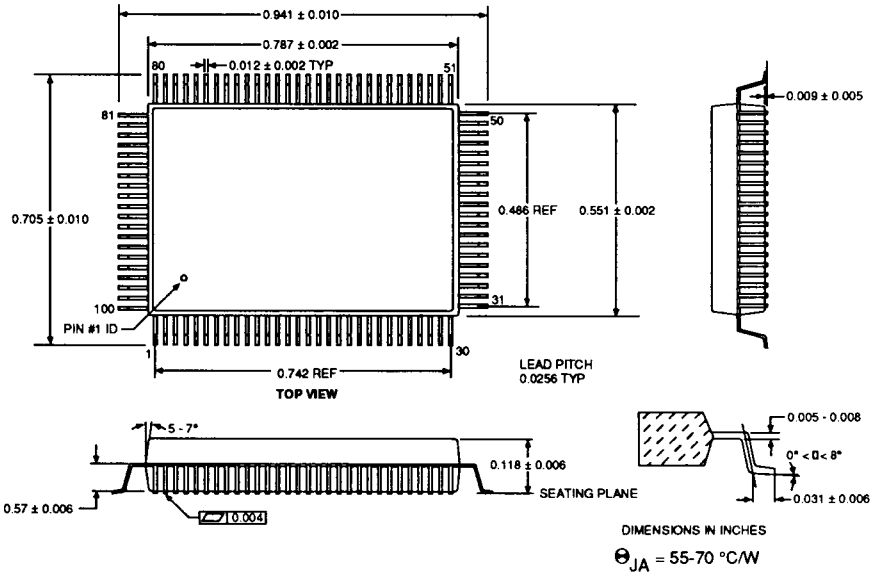
Θ_{JA}= 30–35 °C/W

Θ_{JC}= 3–7 °C/W

1105 36C

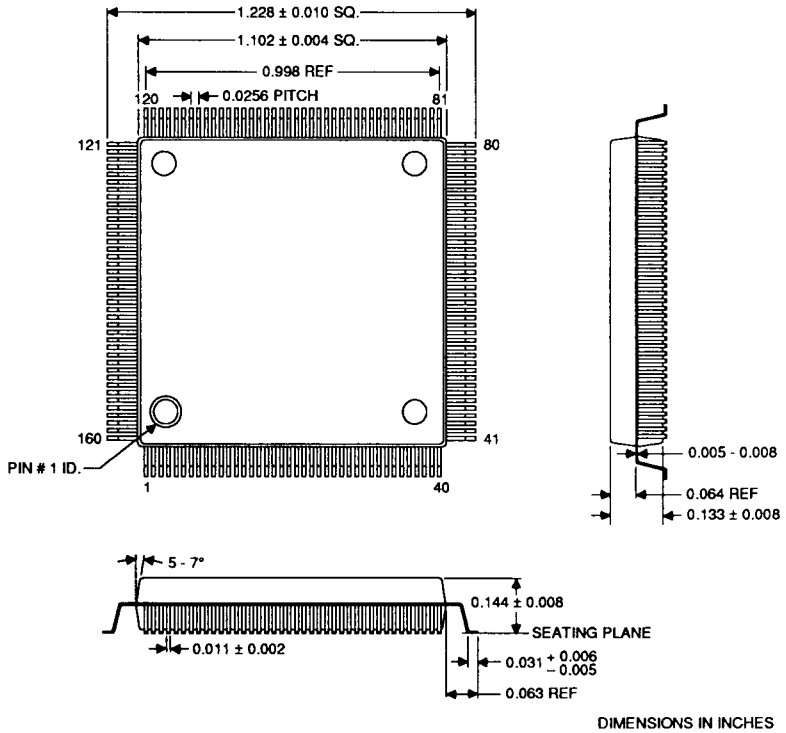
84-Pin PLCC Package

PHYSICAL DIMENSIONS (Continued)



1105 39C

100-Pin PQFP Package

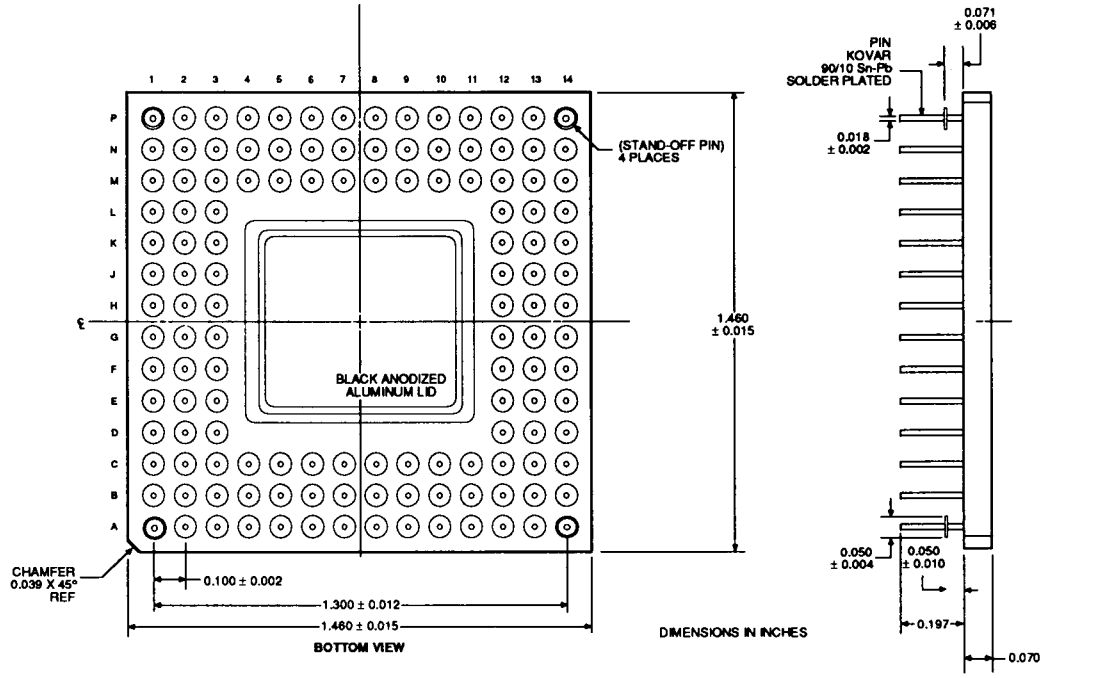


160-Pin PQFP Package

X1159

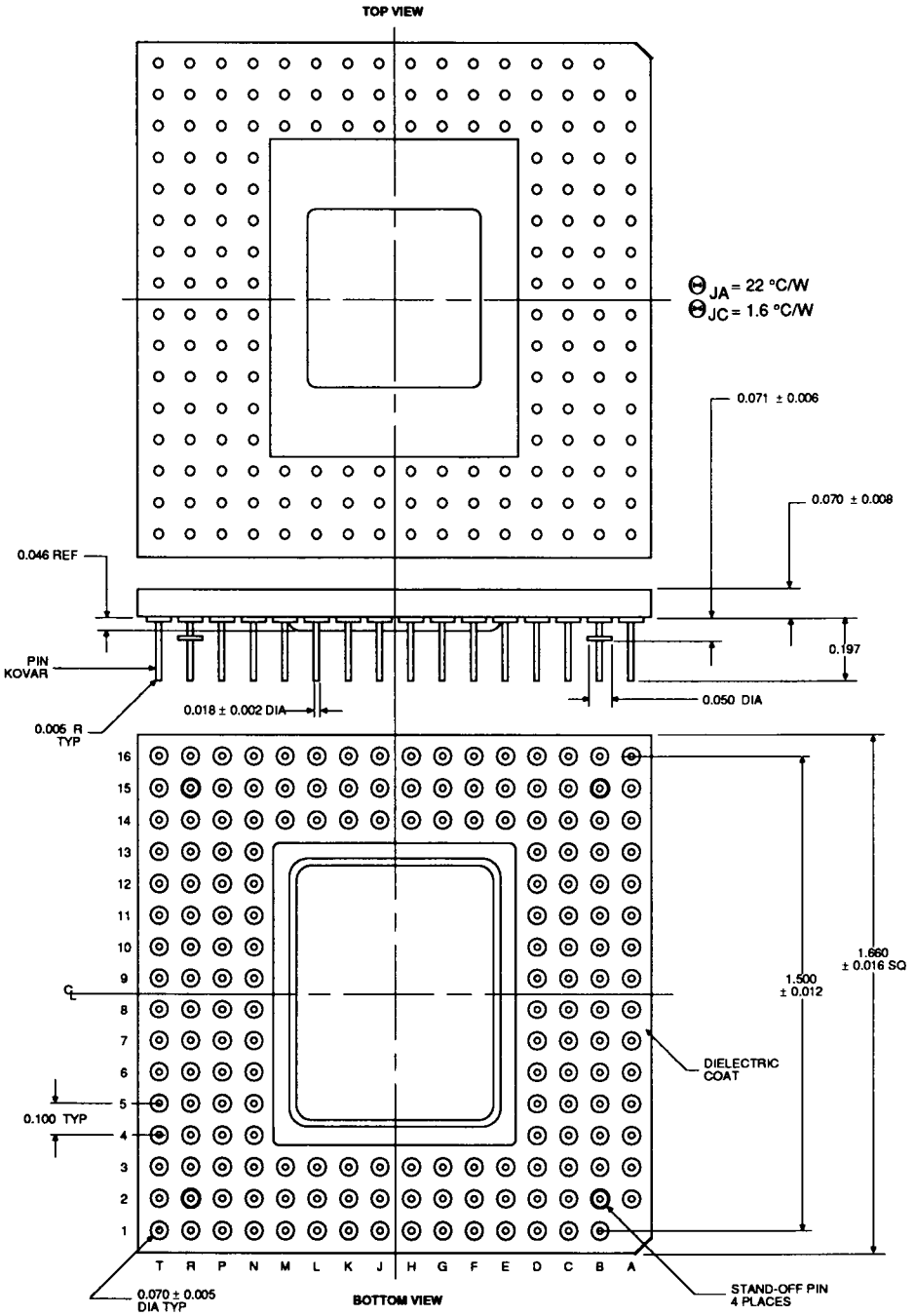
X1158

PHYSICAL DIMENSIONS (Continued)



132-Pin PPGA Package

PHYSICAL DIMENSIONS (Continued)



1991 01B

175-Pin PPGA Package (Plastic)