GENERAL DESCRIPTION

The XR16L651[1] (651) is a 2.5V, 3.3V and 5V Universal Asynchronous Receiver and Transmitter (UART) with 5V tolerant inputs. This new device supports Intel and Motorola data bus interface and is software compatible to industry standard 16C450, 16C550, ST16C580 and ST16C650A UARTs.

The 651 has 32 bytes of TX and RX FIFOs and is capable of operating up to serial data rate of 2 Mbps at 3.3V supply voltage. The internal registers include the 16C550 register set plus Exar's enhanced registers for additonal features to support today's highly demanding data communication needs. The enhanced features include automatic hardware and software flow control, selectable TX and RX trigger levels, and wireless infrared (IrDA) encoder/decoder.

The device provides a new capability to give user the ability to program the wireless infrared encoder output pulse width, hence, reduces the power consumption of the handheld unit.

The XR16L651 device comes in in a small 7x7x1mm 48-pin TQFP package with commercial and industrial temperature ranges.

NOTE: *Covered by US patents #5,649,122 and #5,949,787*

NOTE: *Underline features are exclusive to XR16L651.*

FEATURES

- 2.5V, 3.3V and 5V Operation w/ 5V tolerant Inputs[2]
- ST16C450/550/580/650A Software Compatible
- Intel, Motorola[2] or PC Mode 8-bit Bus Interface
- Up to 1Mbps Data Rate at 3.3V Operation
- 32-byte Transmit and Receive FIFOs
- Automatic Hardware (RTS/CTS) Flow Control
- Hardware Flow Control Hysteresis
- Automatic Software (Xon/Xoff) Flow Control
- Infrared (IrDA) Encoder/Decoder Enable Input[2]
- Programmable Infrared Encoder Pulse Witdh
- Sleep Mode with Wake-up Indicator
- 48-pin TQFP Package (7x7x1mm)
- Commercial and Industrial Temperature Grades

APPLICATIONS

- Battery Operated Electronics
- Internet Appliances
- Handheld Terminal
- Personal Digital Assistants
- Cellular Phones DataPort
- Wireless Infrared Data Communications Systems

FIGURE 1. BLOCK DIAGRAM

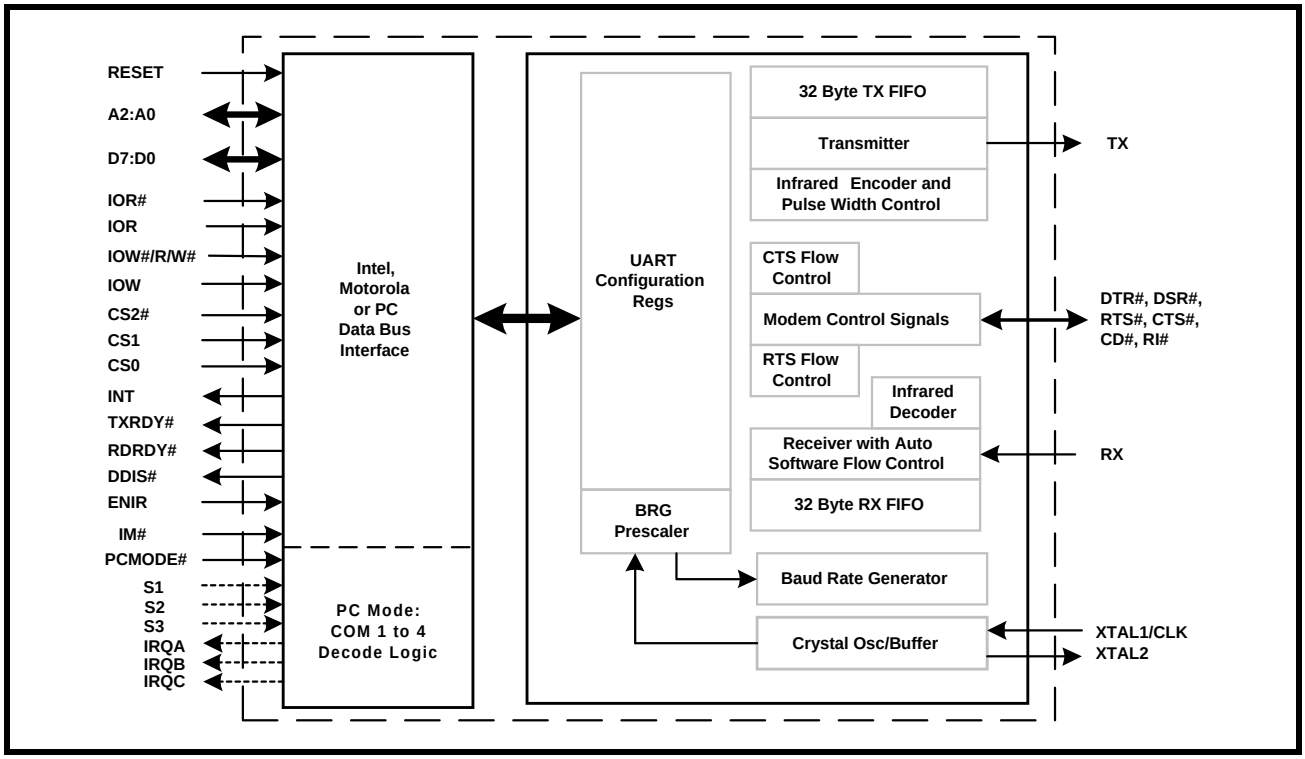
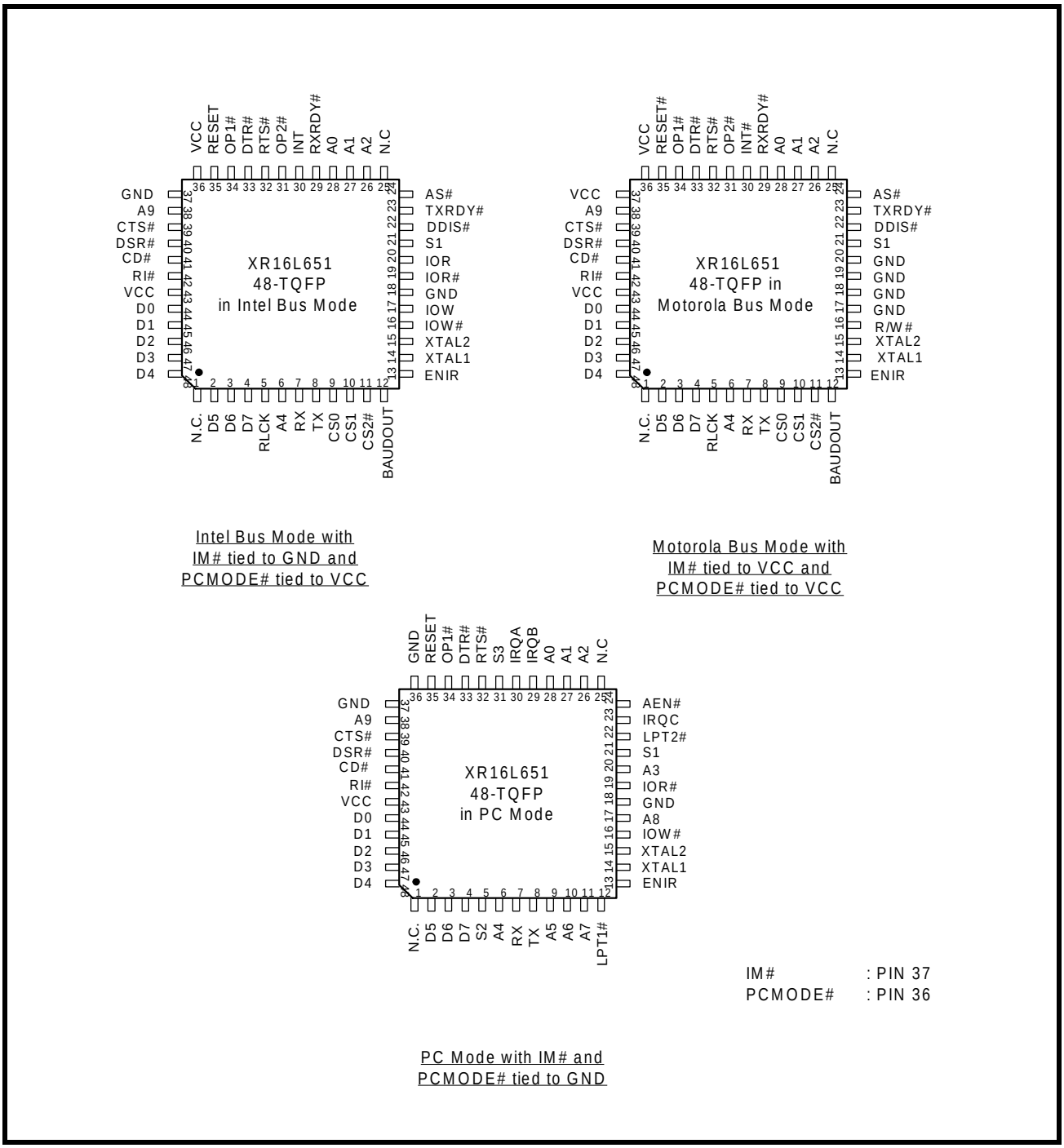


FIGURE 2. INTEL, MOTOROLA AND PC MODE PIN OUT.



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGR
XR16L651CM	48-TQFP	0°C to +70°C
XR16L651IM	48-TQFP	-40°C to +85°C

PIN DESCRIPTIONS

NOTE: Pin type: I=Input, O=Output, IO= Input/output, OD=Output Open Drain.

NAME	PIN #	TYPE	DESCRIPTION
16 (Intel) or 68 (Motorola) MODE DATA BUS INTERFACE. The PCMODE# pin is connected to VCC.			
A2-A0	26,27,28	I	Address data lines [2:0]. A0:A2 selects internal UART's configuration registers.
D7:D0	4,3,2,48-44	IO	Data bus lines [7:0] (bidirectional).
IOR#	19	I	Input/Output Read (active low). When IM# pin is at logic 0, it selects Intel bus interface and this input is read strobe (active low). The falling edge instigates an internal read cycle and retrieves the data byte from an internal register pointed by the address lines [A2:A0], places it on the data bus to allow the host processor to read it on the leading edge. When IM# pin is at logic 1, it selects Motorola bus interface and the IOR# input is not used and it should be connected to GND to minimize supply curent. Its function is the same as IOR, except it is active low. Either an active IOR# or IOR is required to transfer data from 651 to CPU during a read operation.
IOR	20		Input/Output Read (active high). Same as IOR# but active high. When IM# pin is at logic 1 for Motorola bus mode, this pin is not used and should be connected to GND to minimize supply curent.
IOW# (R/W#)	16	I	When IM# pin is at logic 0, it selects Intel bus interface and this input becomes write strobe (active low). The falling edge instigates the internal write cycle and the trailing edge transfers the data byte on the data bus to an internal register pointed by the address lines [A2:A0]. Its function is the same as IOW, except it is active low. Either an active IOW# or IOW is required to transfer data from 651 to the Intel type CPU during a write operation. When IM# pin is at logic 1, it selects Motorola bus interface and this input becomes R/W# signal for read (logic 1) and write (logic 0).
IOW	17		Input/Output Write. Same as IOW# but active high. When IM# pin is at logic 1 for Motorola bus mode, this pin must be connected to GND to allow IOW# input to function correctly.
CS0	9	I	Chip Select 0 input (active high). This input selects the XR16L651 device. If CS1 or CS2# is used as the chip select then this pin must be connected to VCC.
CS1	10		Chip Select 1 input (active high). This input selects the XR16L651 device. If CS0 or CS2# is used as the chip select then this pin must be connected to VCC.
CS2#	11		Chip Select 2 input (active low). This input selects the XR16L651 device. If CS0 or CS1 is used as the chip select then this pin must be connected to GND.
INT (INT#)	30	O	Interrupt Output. This output becomes active whenever the transmitter, receiver, line and/or modem status register has an active condition. See interrupt section for more detail. When IM# pin is at logic 0 (Intel bus mode), this interrupt output may be set to normal active high or active high open source to provide wire-OR capability by connecting a 1k to 10k ohms resistor between this pin and ground. When IM# pin is at logic 1 (Motorola bus mode), this interrupt output becomes an open drain, active low output. It requires an external pull-up resistor of 1K-10K ohms to operate properly. The output may be wire-OR'ed with other devices in the system to form a single interrupt request to the host processor and have the software driver poll all devices to determine the interrupting condition(s).

NAME	PIN #	TYPE	DESCRIPTION
AS#	24	I	Address Strobe input (active low). In the Intel bus mode, the leading-edge transition of AS# latches the chip selects (CS0, CS1, CS2#) and the address lines A0, A1 and A2. This input is used when the address lines and chip select inputs are not stable for the duration of a read or write operation, i.e.,for a processor that needs to de-multiplex the address and data lines. If not required, this input can be permanently tied to GND. This input is not used in the Motorola mode.
PC Mode Interface Signals. Connect PCMODE# pin to GND and IM# pin to GND to select PC Mode.			
A3, A4, A5, A6, A7, A8, A9	20, 6, 9, 10,11,17,38	I	In the PC mode, these are the addtional address lines from the host address bus. They are inputs to the on-board chip select decode function for COM 1-4 and LPT ports. See Table 1 for details. The pins A4 and A9 have internal 100kΩ pull-up resistors.
AEN#	24	I	Address Enable input (active low). When AEN# transition to logic 0, it decodes and validates COM 1-4 ports address per S1, S2 and S3 inputs.
S1, S2, S3	21,5,31	I	Select 1 to 3. These are the standard PC COM 1-4 ports and IRQ selection inputs. See Table 1 and Table 2 for details. The S1 pin has an internal 100kΩ pull-up resistor.
IRQA, IRQB, IRQC	30,29,23	O	Interrupt Request A, B and C Outputs (active high, tri-state). These are the interrupt outputs associated with COM 1-4 to be connected to the host data bus. See interrupt section for details. The Interrupt Requests A, B or C functions as IRQx to the PC bus. IRQx is enabled by setting MCR bit-3 to logic 1 and the desired interrupt(s) in the interrupt enable register (IER).
LPT1#	12	O	Line Printer Port-1 Decode Logic Output (active low). This pin functions as the PC standard LPT-1 printer port address decode logic output, see Table 1. The baud rate generator clock output, BAUDOUT#, is internally connected to the RCLK input in the PC mode.
LPT2#	22	O	Line Printer Port-2 Decode Logic Output (active low) - This pin functions as the PC standard LPT-2 printer port address decode logic output, see Table 1.
MODEM OR SERIAL I/O INTERFACE			
TX	8	O	Transmit Data or wireless infrared transmit data. This output is active low in normal standard serial interface operation (RS-232, RS-422 or RS-485) and active high in the infrared mode. Infrared mode can be enabled by connecting pin ENIR to VCC or through software settling after power up.
RX	7	I	Receive Data or wireless infrared receive data. Normal received data input idles at logic 1 condition and logic 0 in the infrared mode. The wireless infrared pulses are applied to the decoder. This input must be connected to its idle logic state in either normal, logic 1, or infrared mode, logic 0, else the receiver may report “receive break” and/or “error” condition(s).
RTS#	32	O	Request to Send or general purpose output (active low). This port may be used for one of two functions: 1) automatic hardware flow control, see EFR bit-6, MCR bits-1 & 2, FCTR bits 0-3 and IER bit-6. 2) RS485 half-duplex direction control, see FCTR bit-5, MCR bit-2 and MSR bits 4-7. RTS# output must be asserted before auto RTS flow control can start.

NAME	PIN #	TYPE	DESCRIPTION
CTS#	39	I	Clear to Send or general purpose input (active low). If used for automatic hardware flow control, data transmission will be stopped when this pin is de-asserted and will resume when this pin is asserted again. See EFR bit-7, MCR bit-2 and IER bit-7.
DTR#	33	O	Data Terminal Ready or general purpose output (active low).
DSR#	40	I	Data Set Ready input or general purpose input (active low).
CD#	41	I	Carrier Detect input or general purpose input (active low).
RI#	42	I	Ring Indicator input or general purpose input (active low).
ANCILLARY SIGNALS			
XTAL1	14	I	Crystal or external clock input.
XTAL2	15	O	Crystal or buffered clock output.
RCLK	5	I	This input is used as external 16X clock input to the receiver section. Connect the -BAUDOUT pin to this input externally.
BAUDOUT#	12	O	Baud Rate Generator Output (active low). This pin provides the 16X clock of the selected data rate from the baud rate generator. The RCLK pin must be connected externally to BAUDOUT# when the receiver is operating at the same data rate. When the PC mode is selected, the baud rate generator clock output is internally connected to the RCLK input. This pin then functions as the LPT-1 printer port decode logic output, see Table 2.
PCMODE#	36	I	PC Mode Select (active low). When this input is at logic 0, it enables the on-board chip select decode function according to PC ISA bus COM[4:1] and IRQ[4,3] port definitions. See Table 2 for details. This pin has an internal 100kΩ pull-up resistor.
DDIS#	22	O	Drive Disable Output. This pin goes to a logic 0 whenever the host CPU is reading data from the 651. It can control the direction of a data bus transceiver between the CPU and 651 or other logic functions.
ENIR	13	I	Enable Infrared Mode (active high). This pin can be used to start up the UART in wireless infrared mode upon power up or a reset. The TX output would idle at logic 0 instead of normal logic 1. The software infrared enable bit (MCR bit-6) will have full enable/disable control after the power up.
RESET (RESET#)	35	I	Reset Input. When it is asserted, the UART configuration registers are reset to default values, see Table 13. When IM# pin is at a logic 0, Intel bus mode, reset input is active high. When IM# pin is at a logic 1, Motorola bus mode, reset input is active low.
IM#	37	I	Intel or Motorola data bus interface select. A logic 0 selects Intel bus interface and a logic 1 selects Motorola interface. This input affects the functionality of IOR#, IOW#, CS# and INT pins.
OP1#	34	O	Output Port 1. General purpose output.
OP2#	331	O	Output Port 2. General purpose output.
VCC	43		2.5V, 3.3V or 5V.
GND	18		Power supply common ground.
NC	1,25		No Connect. Conenct to VCC or GND to minimize noise.

PRODUCT DESCRIPTION

The XR16L651 (651) is industry first multi-voltage UART that can operate at 2.5, 3.3 or 5V power supplies. Its inputs are 5V tolerant to facilitate interconnection to transceiver devices of RS-232, RS-422 or RS-485. The 651 is software compatible to the industry standad 16C550 with additional enhanced features.

The 651 provides serial asynchronous receive data synchronization, parallel-to-serial and serial-to-parallel data conversions for both the transmitter and receiver sections. These functions are necessary for converting the serial data stream into parallel data that is required with digital data systems. Synchronization for the serial data stream is accomplished by adding start and stops bits to the transmit data to form a data character (character orientated protocol). Data integrity is ensured by attaching a parity bit to the data character. The parity bit is checked by the receiver for any transmission bit errors. The electronic circuitry to provide all these functions is fairly complex especially when manufactured on a single integrated silicon chip. The XR16L651 represents such an integration with greatly enhanced features. The 651 is fabricated with an advanced CMOS process.

The 651 supports standard 8-bit Intel, Motorola or PC bus interfaces through 2 input selection pins. The Intel bus uses separate input/output read and write signals for all bus transactions while the Motorola bus uses a read/write signal and chip select to conduct the same transactions. The PC bus mode associates with the PC ISA bus and follow the industry standard PC definitions for COM 1-4 serial port addresses. The 651 includes on-board chip select decode logic and selection for the proper interrupt request. This eliminates the need for an external logic array device.

The 651 has 32-byte each of transmit and receive FIFOs, automatic RTS/CTS hardware flow control with hysteresis, automatic Xon/Xoff and special character software flow control, programmable transmit and receive FIFO trigger levels, wireless infrared encoder and decoder (IrDA ver 1.0), programmable baud rate generator with a prescaler of divide by 1 or 4, and data rate up to 1.0 Mbps at 16X sampling clock rate.

The 651 is an upward solution that provides 32 bytes of transmit and receive FIFO memory, instead of 16 bytes provided in the 16C550, or none in the 16C450. The 651 is designed to work with high speed communication devices, that require fast data processing time. Increased performance is realized in the 651 by the larger transmit and receive FIFOs. This allows the external processor to handle more networking tasks within a given time. For example, the standard ST16C550 with a 16 byte FIFO, unloads 16 bytes of receive data in 1.53 ms (This example uses a character length of 11 bits, including start/stop bits at 115.2Kbps). This means the external CPU will have to service the receive FIFO at 1.53 ms intervals. However with the 32 byte FIFO in the 651, the data buffer will not require unloading/loading for 3.05 ms. This increases the service interval giving the external CPU additional time for other applications and reducing the overall UART interrupt servicing time. In addition, the 4 selectable levels of FIFO trigger interrupt and automatic hardware/software flow control is uniquely provided for maximum data throughput performance especially when operating in a multi-channel environment. The combination of the above greatly reduces the bandwidth requirement of the external controlling CPU, increases performance, and reduces power consumption.

The rich feature set of the 651 is available through internal registers. Automatic hardware/software flow control, selectable transmit and receive FIFO trigger levels, selectable TX and RX baud rates, infrared encoder/decoder interface, modem interface controls, and a sleep mode are all standard features. In the PC mode, two tri-state interrupt lines (IRQB and IRQC) and one selectable open source interrupt output (IRQA) are available. The open source interrupt scheme allows multiple interrupts to be combined in a “wire-OR” operation, thus reducing the number of interrupt lines in larger systems. Following a power on reset or an external reset, the 651 is software compatible with previous generation of UARTs, 16C450, 16C550 and ST16C650A.

FUNCTIONAL DESCRIPTIONS

1.0 HOST DATA BUS INTERFACE

The host interface is a 8 data bit wide with 3 address lines and control signals to execute bus read and write transactions. The 651 supports 3 type of host interfaces: Intel, Morotola and PC mode. The Intel and Motorola interfaces provide support for their respective microcontroller or processor. This facilitates the hardware design and interconnections. The Intel bus interface is selected by connecting IM# to logic 0 and PCMODE# to logic 1. The Intel bus interconnections are shown in Figure 3. The Motorola bus is selected with the IM# input connected to logic 0 and PCMODE# input ties to logic 1. The Motorola bus interconnections are shown in Figure 4. The special PC mode is selected when IM# and PCMODE# are connected to logic 0. The PC mode interconnections are shown in Figure 5.

FIGURE 3. XR16L651 INTEL BUS INTERCONNECTIONS

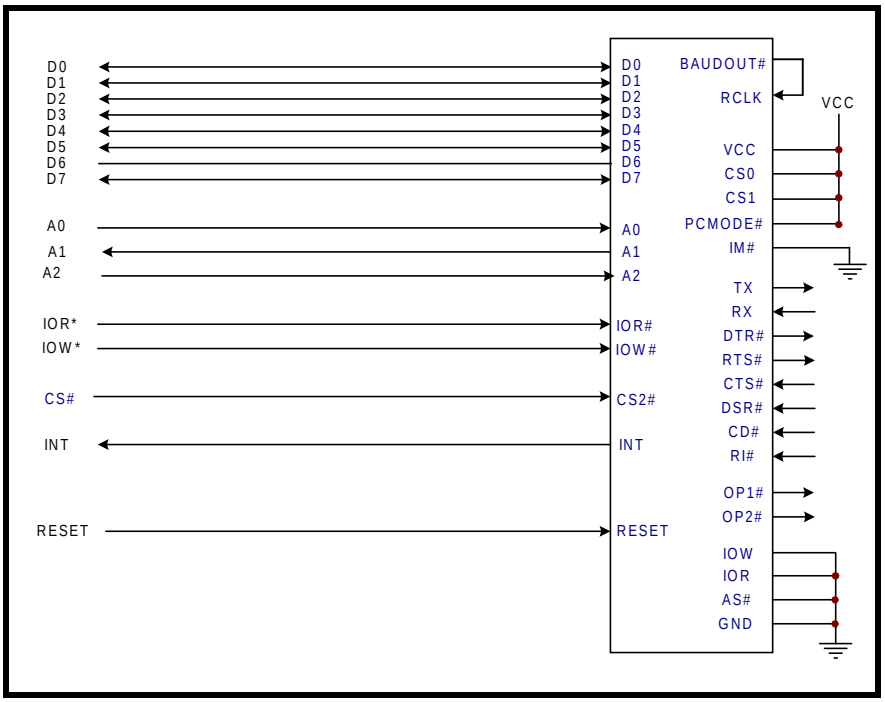


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FIGURE 4. XR16L651 MOTOROLA BUS INTERCONNECTIONS.

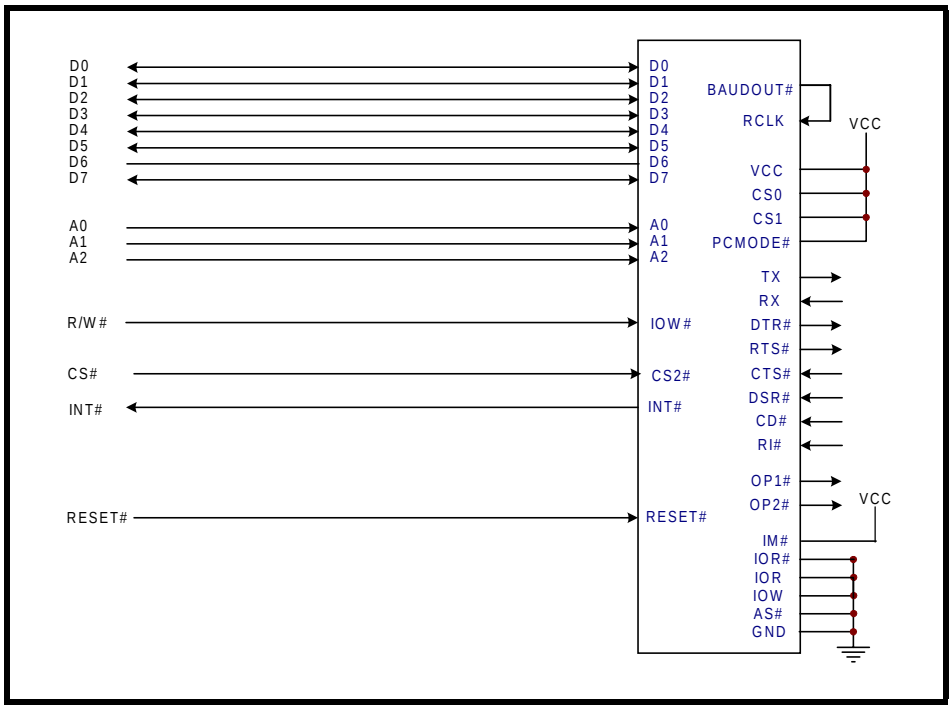
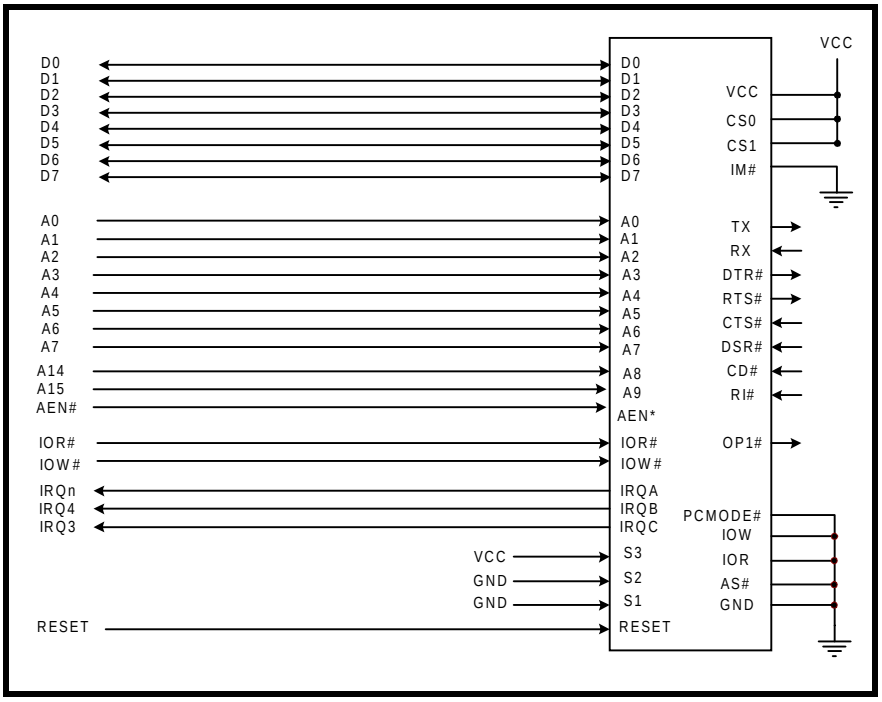


FIGURE 5. XR16L651 PC MODE INTERCONNECTIONS



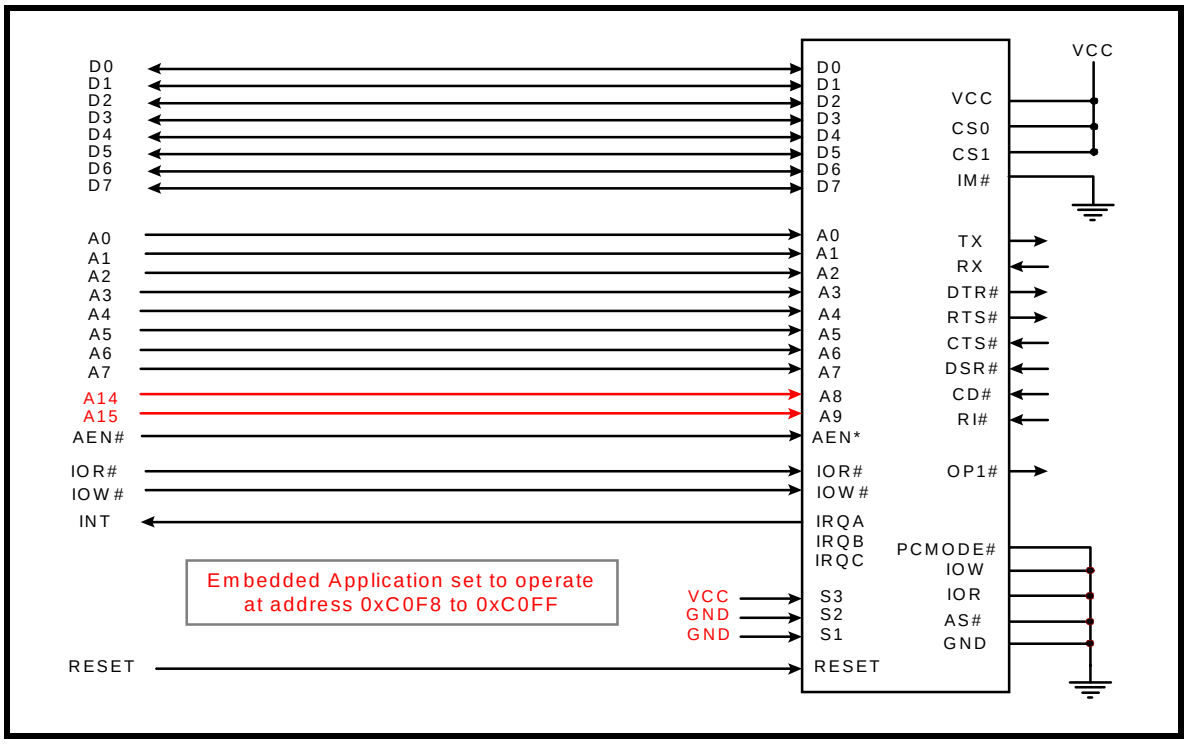
1.1 PC MODE

The PC mode interface includes an on-chip address decoder and interrupt selection function for the standard PC COM 1-4 ports addresses. The selection is made through three input signals: S1, S2 and S3. The selection summary is shown in Table 1. Although the on-chip address decoder was designed for PC applications ranging from 0x278 to 0x3FF, it can fit into an embedded applications by offsetting the address lines to the 651. An example is shown in Figure 6 where the UART is operating from 0xC0F8 to 0xC0FF address space. Operating in the PC mode eliminates external address decode components.

TABLE 1: PC MODE INTERFACE ON-CHIP ADDRESS DECODER AND INTERRUPT SELECTION.

PCMODE# INPUT	S3, S2, S1 INPUTS	A3-A9 ADDRESS LINES TO ON-CHIP DECODER	COM/LPT PORT SELECTION	IRQ OUTPUT SELECTION
0	0 0 0	0x3F8 - 0x3FF	COM-1	IRQB (for PC's IRQ4)
0	0 0 1	0x2F8 - 0x2FF	COM-2	IRQC (for PC's IRQ3)
0	0 1 0	0x3E8 - 0x3EF	COM-3	IRQB (for PC's IRQ4)
0	0 0 0	0x3F8 - 0x3FF	COM-4	IRQB (for PC's IRQ4)
0	1 0 0	0x2F8 - 0x2FF	COM-1	IRQA (for PC's IRQn
0	1 0 1	0x3E8 - 0x3EF	COM-2	IRQA (for PC's IRQn)
0	1 1 0	0x2E8 - 0x2EF	COM-3	IRQA (for PC's IRQn)
0	1 1 1	0x3F8 - 0x3FF	COM-4	IRQA (for PC's IRQn)
0	- - -	0x278 - 0x27F	LPT-2	N/A
0	- - -	0x378 - 0x37F	LPT-1	N/A

FIGURE 6. PC MODE INTERFACE IN AN EMBEDDED APPLICATION.



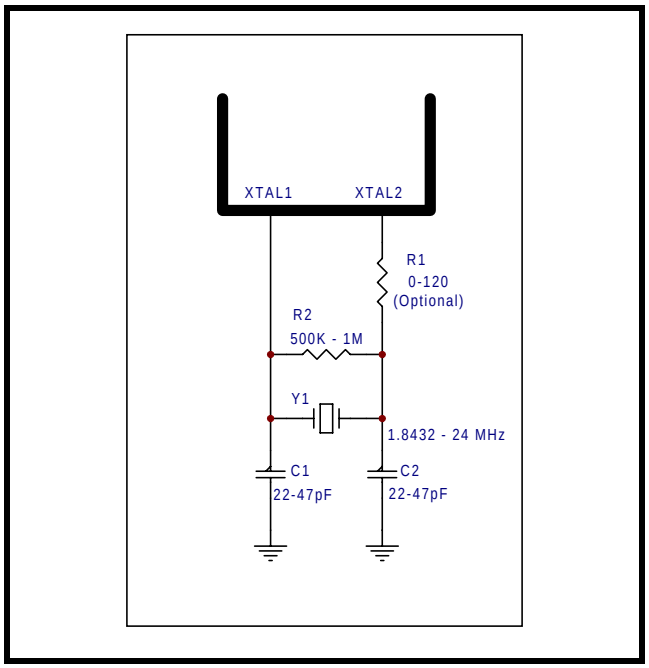
2.0 INTERRUPT

The output function of interrupt, INT, output changes according to the operating bus type and various factors. Table 2 sumarizes its behaviour in Intel, Motorola and PC mode of operation. Multiple interrupts can be wire-OR'ed. This is accomplished by setting MCR bit-5 to a logic 1 and connecting a 1k to 10k ohms resistor between this pin and ground to provide an acceptable logic 0 level.

TABLE 2: INTERRUPT OUTPUT (INT, INT# AND IRQA) FUNCTIONS

IM# INPUT (INTEL/ MOTOROLA)	PCMODE# INPUT	S3 INPUT	MCR BIT-5 (INT TYPE SELECT)	MCR BIT-3 (IRQN ENABLE)	INTERRUPT OUTPUT (INT, INT# OR IRQA)
Intel Bus Mode					
1	1	don't care	0	don't care	INT is logic 0 for inactive interrupt. INT is logic 1 for active interrupt (active high)
1	1	don't care	1	don't care	INT is tri-state for inactive interrupt INT is logic 1 for active interupt (open source). Requires a 1k-10k ohms resistor to GND.
Motorola Bus Mode					
0	X	don't care	0	don't care	INT# is tri-state for inactive interrupt. INT# is logic 0 for active interrupt (actie low, open drain). Requires a 1k-10k ohms resistor to VCC.
0	X	don't care	1	don't care	INT# is tri-state.
PC Mode					
1	0	0	don't care	don't care	IRQA is tri-state. Either IRQB or IRQC is used, see Table 1.
1	0	1	don't care	0	IRQA is tri-state.
1	0	1	0	1	IRQA is logic 0 for iactive interrupt. IRQA is logic 1 for active interrupt (active high).
1	0	1	1	1	IRQA is tri-state for no interrupt. IRQA is logic 1 for active interrupt (active high, open source).

FIGURE 7. TYPICAL OSCILLATOR CONNECTIONS



3.0 CRYSTAL OSCILLATOR OR EXTERNAL CLOCK.

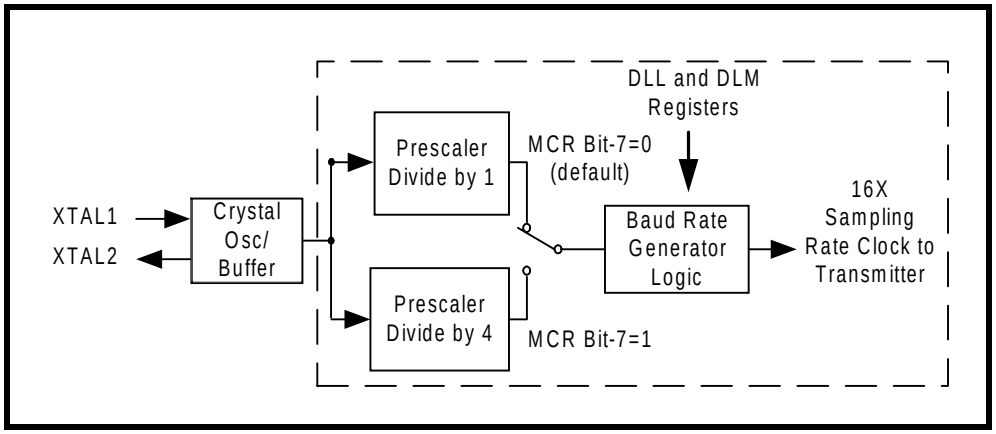
The 651 includes an on-chip oscillator (XTAL1 and XTAL2). The crystal oscillator provides the system clock to the Baud Rate Generators (BRG) in the UART. XTAL1 is the input to the oscillator or external clock buffer input with XTAL2 pin being the output. For programming details, see “Programmable Baud Rate Generator” on page 11 .

The on-chip oscillator is designed to use an industry standard microprocessor crystal (parallel resonant, fundamental frequency with 10-22 pF capacitance load, ESR of 20-80 ohms and 100ppm frequency tolerance) connected externally between the XTAL1 and XTAL2 pins (see Figure 7). Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal baud rate generator for standard or custom rates. Typically, the oscillator connections are shown in Figure 7. For further reading on oscillator circuit please see application note DAN108 on EXAR’s web site

3.1 PROGRAMMABLE BAUD RATE GENERATOR

The UART has its own Baud Rate Generator (BRG) with a prescaler for the transmiter. The prescaler is controlled by a software bit in the MCR register. The MCR register bit-7 sets the prescaler to divide the input crystal or external clock by 1 or 4. The clock output of the prescaler goes to the BRG. The BRG further divides this clock by a programmable divisor between 1 and (2^{16} -1) to obtain a 16X sampling clock of the serial data rate. The sampling clock is used by the transmitter for data bit shifting and receiver for data sampling. The BRG divisor (DLL and DLM registers) defaults to a random value upon power up or a reset . Therefore, the BRG must be programmed during initialization to the operating data rate.

FIGURE 8. BAUD RATE GENERATOR



Programming the Baud Rate Generator Registers DLM and DLL provides the capability of selecting the operating data rate. Table 3 shows the standard data rates available with a 14.7456 MHz crystal or external clock at 16X clock rate. When using a non-standard data rate crystal or external clock, the divisor value can be calculated for DLL/DLM with the following equation.

divisor (decimal) = (XTAL1 clock frequency / prescaler) / (serial data rate x 16)

TABLE 3: TYPICAL DATA RATES WITH A 14.7456 MHZ CRYSTAL OR EXTERNAL CLOCK

OUTPUT Data Rate MCR Bit-7=1	OUTPUT Data Rate MCR Bit-7=0	DIVISOR FOR 16X Clock (Decimal)	DIVISOR FOR 16X Clock (HEX)	DLM PROGRAM VALUE (HEX)	DLL PROGRAM VALUE (HEX)	DATA RATE ERROR (%)
100	400	2304	900	09	00	0
600	2400	384	180	01	80	0
1200	4800	192	C0	00	C0	0
2400	9600	96	60	00	60	0
4800	19.2k	48	30	00	30	0
9600	38.4k	24	18	00	18	0
19.2k	76.8k	12	0C	00	0C	0
38.4k	153.6k	6	06	00	06	0
57.6k	230.4k	4	04	00	04	0
115.2k	460.8k	2	02	00	02	0
230.4k	921.6k	1	01	00	01	0

4.0 TRANSMIT AND RECEIVE DATA

The 651 UART has a transmit holding register (THR) and a receive holding register (RHR). The software driver must first separately read the LSR content for associated received data byte error flags before reading the receive data byte off the register RHR. That is because upon reading the RHR register the FIFO pointer increments and points to next data byte.

4.1 FIFO DATA LOADING AND UNLOADING THROUGH REGISTERS THR AND RHR.

The serial transmitter section consists of an 8-bit Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the THR is provided in the Line Status Register (LSR). Writing to the THR transfers the contents of the data bus (D7-D0) to the THR, providing that the THR or TSR is empty. The THR empty flag in the LSR register will be set to a logic 1 when the transmitter is empty or when data is transferred to the TSR. Note that a write operation can be performed when the transmit holding register empty flag is set (logic 0 = at least one byte in FIFO / THR, logic 1= FIFO/THR empty).

The serial receive section also contains an 8-bit Receive Holding Register, RHR. Receive data is unloaded by reading the RHR register. The receive section provides a mechanism to prevent false starts. On the falling edge of a start or false start bit, an internal receiver counter starts counting clocks at 16x clock rate. After 7 1/2 clocks the start bit time should be shifted to the center of the start bit. At this time the start bit is sampled and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. Data byte error, if any, status is reported in LSR register.

The THR and RHR register address is located at 0x00. Transmit data byte is loaded to the THR when writting to address 0x00. Receive data is unloaded from the RHR register when reading that same address location.

5.0 AUTOMATIC RTS HARDWARE FLOW CONTROL OPERATION

Automatic RTS hardware flow control is used to prevent data overrun to the local receiver FIFO. The RTS# output is used to request remote unit to suspend/resume data transmission. The auto RTS flow control features is enabled to fit specific application requirement (see Figure 9):

- Enable auto RTS flow control using EFR bit-6.
- The auto RTS function must be started by asserting RTS output pin (MCR bit-0 or 1 to logic 1 after it is enabled.
- Enable RTS interrupt through IER bit-6 (after setting EFR bit-4). The UART issues an interrupt when the RTS# pin makes a transition: ISR bit-5 will be set to logic 1.

With the Auto RTS function enabled, the RTS# pin will not be de-asserted (logic 1) when the receive FIFO

reaches the programmed trigger level, but will be de-asserted when the FIFO reaches the next trigger level (See Table 10). The RTS# will be asserted again after the FIFO is unloaded to the next trigger level below the programmed trigger level. However, even under these conditions, the 651 will continue to accept data until the receive FIFO is full.

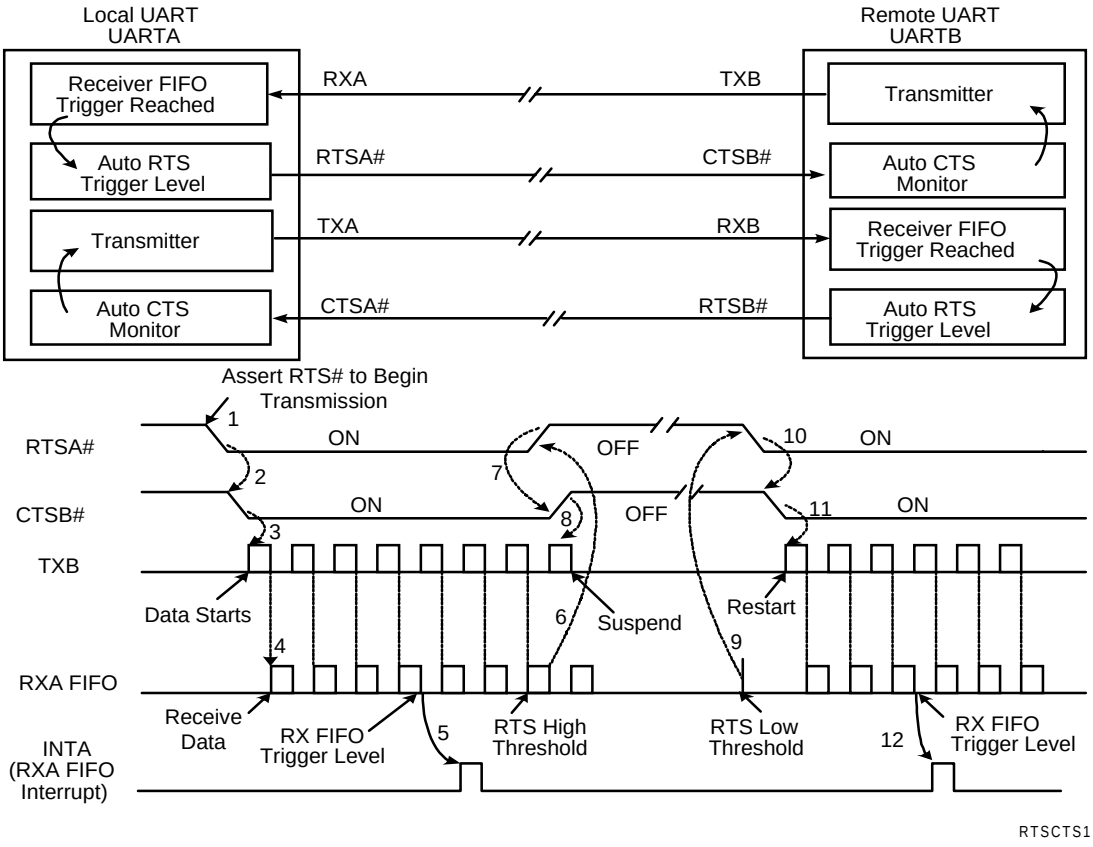
5.1 Auto CTS Flow Control

Automatic CTS flow control is used to prevent data overrun to the remote receiver FIFO. The CTS# input is monitored to suspend/restart the local transmitter.

The auto CTS flow control feature is selected to fit specific application requirement (see Figure 9):

- Enable auto CTS flow control using EFR bit-7.
- Enable CTS interrupt through IER bit-7 (after setting EFR bit-4). The UART issues an interrupt when the CTS# pin is de-asserted (logic 1): ISR bit-5 will be set to 1, and UART will suspend transmission as soon as the stop bit of the character in process is shifted out. Transmission is resumed after the CTS# input is re-asserted (logic 0), indicating more data may be sent.

Figure 9. Auto RTS and CTS Flow Control Operation



The local UART (UARTA) starts data transfer by asserting RTSA# (1). RTSA# is normally connected to CTSB# (2) of remote UART (UARTB). CTSB# allows its transmitter to send data (3). TXB data arrives and fills UARTA receive FIFO (4). When RXA data fills up to its receive FIFO trigger level, UARTA activates its RXA data ready interrupt (5) and continues to receive and put data into its FIFO. If interrupt service latency is long and data is not being unloaded, UARTA monitors its receive data fill level to match the upper threshold of RTS delay and de-assert RTSA# (6). CTSB# follows (7) and request UARTB transmitter to suspend data transfer. UARTB stops or finishes sending the data bits in its transmit shift register (8). When receive FIFO data in UARTA is unloaded to match the lower threshold of RTS delay (9), UARTA re-asserts RTSA# (10), CTSB# recognizes the change (11) and restarts its transmitter and data flow again until next receive FIFO trigger (12). This same event applies to the reverse direction when UARTA sends data to UARTB with RTSB# and CTSA# controlling the data flow.

5.2 Automatic Software Flow Control

When software flow control is enabled (See Table 12), the 651 compares compares one or two sequential receive data characters with the programmed Xon or Xoff-1,2 character value(s). If receive character(s) (RX) match the programmed values, the 651 will halt transmission (TX) as soon as the current character has completed transmission. When a match occurs, the Xoff (if enabled via IER bit-5) flag will be set and the interrupt output pin will be activated. Following a suspension due to a match of the Xoff characters values, the 651 will monitor the receive data stream for a match to the Xon-1,2 character value(s). If a match is found, the 651 will resume operation and clear the flags (ISR bit-4).

Reset initially sets the contents of the Xon/Xoff 8-bit flow control registers to a logic 0. Following reset the user can write any Xon/Xoff value desired for software flow control. Different conditions can be set to detect Xon/Xoff characters (See Table 12) and suspend/resume transmissions. When double 8-bit Xon/Xoff characters are selected, the 651 compares two consecutive receive characters with two software flow control 8-bit values (Xon1, Xon2, Xoff1, Xoff2) and controls TX transmissions accordingly. Under the above described flow control mechanisms, flow control characters are not placed (stacked) in the user accessible RX data buffer or FIFO.

In the event that the receive buffer is overfilling and flow control needs to be executed, the 651 automatically sends an Xoff message (when enabled) via the serial TX output to the remote modem. The 651 sends the Xoff-1,2 characters two-character-times (= time taken to send two characters at the programmed baud rate) after the receive FIFO crosses the programmed trigger level. To clear this condition, the 651 will transmit the programmed Xon-1,2 characters as soon as receive FIFO drops to one trigger level below the programmed trigger level. Table 4 below explains this:

Table 4: Auto Xon/Xoff (Software) Flow Control

RX Trigger Level	INT Pin Activation	Xoff Character(s) Sent (characters in RX FIFO)	Xon Character(s) Sent (characters in RX FIFO)
8	8	8*	0
16	16	16*	8
24	24	24*	16
28	28	28*	24

** After the trigger level is reached, an xoff character is sent after a short span of time (= time required to send 2 characters); for example, after 2.083ms has elasped for 9600 baud and 10-bit word length setting.*

5.3 Special Character Detect

A special character detect feature is provided to detect an 8-bit character when bit-5 is set in the Enhanced Feature Register (EFR). When this character (Xoff2) is detected, it will be placed in the FIFO along with normal incoming RX data.

The 651 compares each incoming receive character with Xoff-2 data. If a match exists, the received data will be transferred to FIFO and ISR bit-4 will be set to indicate detection of special character. Although the Internal Register Table shows each X-Register with eight bits of character information, the actual number of bits is dependent on the programmed word length. Line Control Register (LCR) bits 0-1 defines the number of character bits, i.e., either 5 bits, 6 bits, 7 bits, or 8 bits. The word length selected by LCR bits 0-1 also determines the number of bits that will be used for the special character comparison. Bit-0 in the X-registers corresponds with the LSB bit for the receive character.

5.4 Infrared Mode

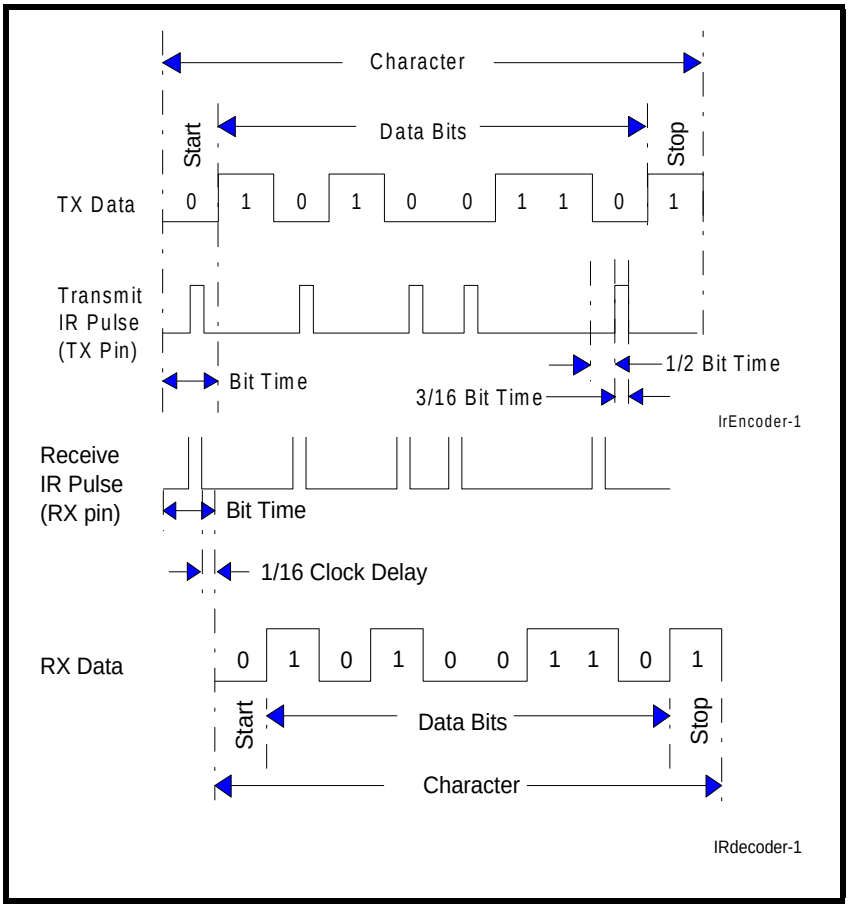
The 651 UART includes the infrared encoder and decoder compatible to the IrDA (Infrared Data Association) version 1.0. The input pin ENIR conveniently activates the infrared mode. Activating the ENIR pin prior to power up prevents the infrared light emitting diode (LED) from turning on and drawing large amount of supply current while the system is powering up. The ENIR pin also sets the MCR register bit-6 to a ‘1. After power up or a reset, the software can overwrite MCR bit-6 if so desired. In the infrared mode, the user can choose to send/receive data either half-duplex or full-duplex. The half-duplex mode is chosen by setting bit-0 of XFR register to a ‘1’. This prevents echoed data from reaching the receiver. When the infrared feature is enabled, the transmit data outputs, TX, idles at logic zero level. Likewise, the RX input assumes an idle level of logic zero, see Figure 10.

The IrDA standard defines the infrared encoder sends out a 3/16 of a bit wide HIGH-pulse for each “0” bit in the transmit data stream. This signal encoding reduc-

es the on-time of the infrared LED, hence reduces the power consumption. See Figure 10 below. The 651 has an additional feature to allow user to vary the transmit pulse width further reducing power consumption of the system where application permits (see IRPW register for details).

The wireless infrared decoder receives the input pulse from the infrared sensing diode on RX pin. Each time it senses a light pulse, it returns a logic 0 to the data bit stream. The 651 also includes another feature - inversion of the IR pulse (XFR register bit-1), where each “0” bit in the data stream is transmitted (and received) as a LOW IR pulse.

FIGURE 10. INFRARED TRANSMIT DATA ENCODING AND RECEIVE DATA DECODING



5.5 DMA OPERATION

The XR16L651 FIFO trigegr levels provide additional flexibility to the user for block mode operation. The user can optionally operate the transmit and receive FIFO’s in the DMA mode (FCR bit-3). The DMA mode affects the state of the -RXRDY and -TXRDY output pins. The following tables show this:

TABLE 5: -RXRDY PIN

NON-DMA MODE	DMA MODE
1 = FIFO empty	0 to 1 transition when FIFO empties
0 = at least 1 byte in FIFO	1 to 0 transition when FIFO reaches trigger level, or timeout occurs

TABLE 6: -TXRDY PIN

NON-DMA MODE	DMA MODE
1 = at least 1 byte in FIFO	1 = FIFO is full
0 = FIFO empty	0 = FIFO has at least 1 empty location

5.6 INTERNAL LOOPBACK

The 651 UART provides an internal loopback capability for system diagnostic purposes. The internal loopback mode is enabled by setting MCR register bit-4 to logic 1. All regular UART functions operate normally. Figure 11 shows how the modem port signals are reconfigured. Transmit data from the transmit shift register output is internally routed to the receive shift reg-

ister input allowing the system to receive the same data that it was sending. The TX pin is held at logic 1 or mark condition while RTS# and DTR# are de-asserted, and CTS#, DSR# CD# and RI# inputs are ignored.

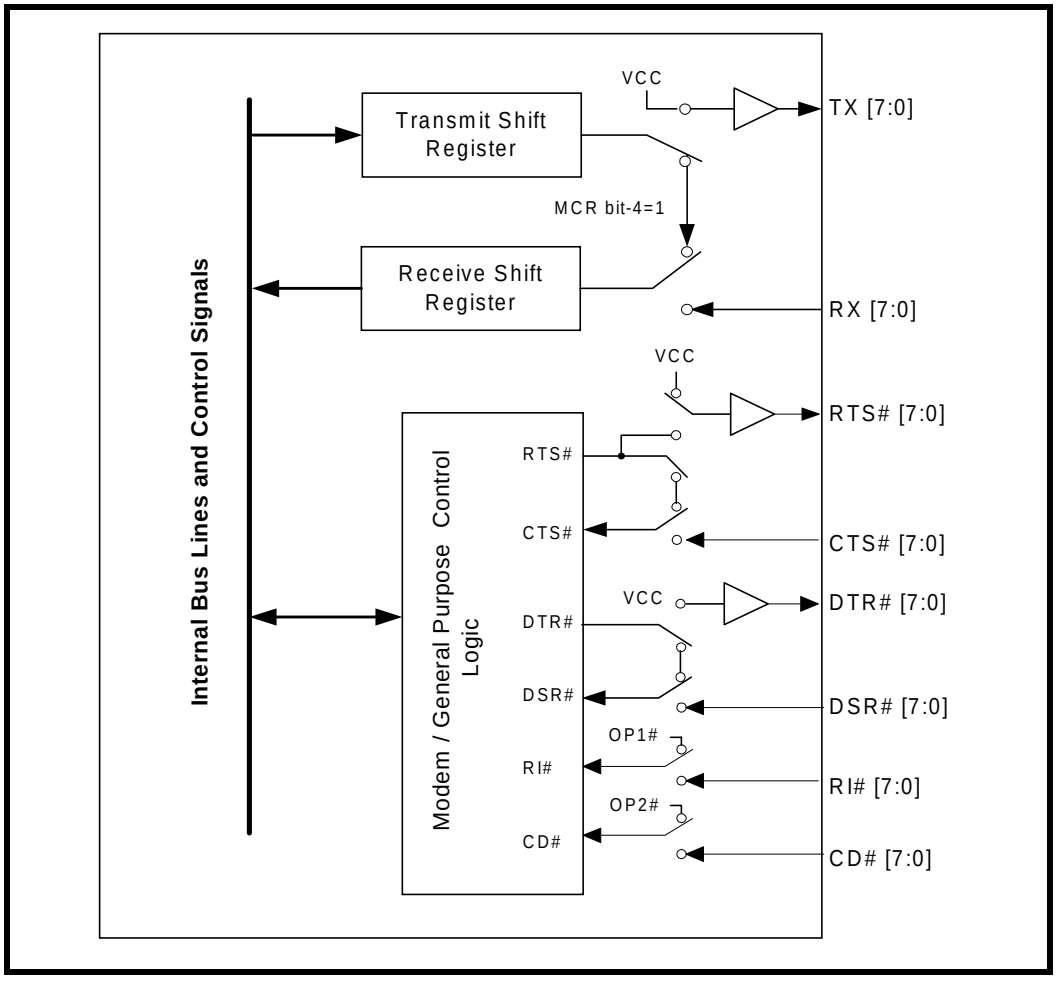
5.7 Device Identification and Revision

The XR16L651 provides a Device Identification code and a Device Revision code to distinguish the part from others. To read the identification code from the part, it is required to set the baud rate generator registers DLL and DLM both to 0x00. Now, reading the content of the DLM will provide 0x04 for the XR16L651 and reading the content of DLL will provide the revision of the part; for example, a reading of 0x01 means revision A.

5.8 Sleep Mode & Wake-up Indicator

The 651 is designed to operate with low power consumption. A special sleep mode is included to further reduce power consumption when the chip is not being used. With EFR bit-4 and IER bit-4 enabled (set to a logic 1), the 651 enters the sleep mode but resumes normal operation when a start bit is detected, a change of state on any of the modem input pins RX, -RI, -CTS, -DSR, -CD, or transmit data is provided by the user. If the sleep mode is enabled and the 651 is awakened by one of the conditions described above, an interrupt is issued by the 651 to signal to the CPU that it is awake. The interrupt source register (ISR) will read a value of 0x01 for this interrupt and reading the ISR clears this interrupt. Since the same value is also used to indicate no pending interrupt, users should exercise caution while using the sleep mode. Once awakened, the 651 will return to the sleep mode automatically after any other interrupting condition (the true cause of waking up the 651) has been serviced. In any case, the sleep mode will not be entered while an interrupt is pending. The 651 will stay in the sleep mode of operation until it is disabled by setting IER bit-4 to a logic 0.

Figure 11. Internal Loop Back



5.9 UART CONFIGURATION REGISTERS.

The 651 has a set of configuration registers selected by address lines A0 to A2. The based page registers are 16C550 compatible with EXAR enhanced feature registers located on the second page (mirror) addresses. The second page registers are only accessible by setting LCR register to a value of 0xBF. The register set is shown on Table 7 and Table 8.

TABLE 7: XR16L651 UART CONFIGURATION REGISTERS

ADDRESS	REGISTER	READ/WRITE	COMMENTS
A2 A1 A0			
16550 COMPATIBLE REGISTERS			
0 0 0	RHR - Receive Holding Reg THR - Transmit Holding Register	Read-only Write-only	LCR[7] = 0
0 0 0	DLL - Div Latch Low	Read/Write	LCR[7] = 1
0 0 1	DLM - Div Latch High	Read/Write	LCR[7] = 1
0 0 0	DREV - Device Revision Code	Read-only	DLL, DLM = 0x00
0 0 1	DVID - Device Identification Code	Read-only	DLL, DLM = 0x00
0 0 1	IER - Interrupt Enable Reg	Read/Write	LCR[7] = 0
0 1 0	ISR - Interrupt Status Reg FCR - FIFO Control Reg	Read-only Write-only	
0 1 1	LCR - Line Control Reg	Read/Write	
1 0 0	MCR - Modem Control Reg	Read/Write	
1 0 1	LSR - Line Status Reg Reserved	Read-only Write-only	
1 1 0	MSR - Modem Status Reg Reserved	Read-only Write-only	
1 1 1	SPR - Scratch Pad Reg	Read/Write	
ENHANCED REGISTERS			
0 1 0	EFR - Enhanced Function Reg	Read/Write	LCR = 0xBF
1 0 0	Xoff-1 - Xoff Character 1	Read/Write	LCR = 0xBF
1 0 1	Xoff-2 - Xoff Character 2 reserved	Read/Write	LCR = 0xBF
1 1 0	Xon-1 - Xon Character 1 reserved	Read/Write	LCR = 0xBF
1 1 1	Xon-2 - Xon Character 2 reserved	Read/Write	LCR = 0xBF

.

TABLE 8: UART CONFIGURATION REGISTERS DESCRIPTION. SHADED BITS ARE ENABLED WHEN EFR BIT-4=1.

ADDRESS A2-A0	REG NAME	READ/ WRITE	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	COMMENT
16C550 Compatible Registers											
0 0 0	RHR	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=0
0 0 0	THR	WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=0
0 0 0	DLL	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=1
0 0 1	DLM	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=1
0 0 0	DREV	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	DLL, DLM = 0x00
0 0 1	DVID	RD	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	DLL, DLM = 0x00
0 0 1	IER	RD/WR	0/ CTS Int. Enable	0/ RTS Int. Enable	0/ Xoff Int. Enable	Sleep Mode Enable	Modem Stat. Int. Enable	RX Line Stat. Int. Enable	TX Empty Int Enable	RX Data Int. Enable	LCR[7]=0
0 1 0	ISR	RD	0/ FIFOs Enable	0/ FIFOs Enable	INT Source Bit-5	INT Source Bit-4	INT Source Bit-3	INT Source Bit-2	INT Source Bit-1	INT Source Bit-0	LCR[7]=X
0 1 0	FCR	WR	0/ RX FIFO Trigger	0/ RX FIFO Trigger	0/ TX FIFO Trigger	0/ TX FIFO Trigger	DMA Mode 1 Enable	TX FIFO Reset	RX FIFO Reset	FIFOs Enable	LCR[7]=X
0 1 1	LCR	RD/WR	Divisor Enable	Set TX Break	Set Par-ity	Even Parity	Parity Enable	Stop Bits	Word Length Bit-1	Word Length Bit-0	LCR[7]=X
1 0 0	MCR	RD/WR	0/ BRG Pres-caler	0/ IR Enable	0/ INT Type Select	Internal Lopback Enable	OP2#/ IRQn Enable	OP1#/	RTS# Control	DTR# Control	LCR[7]=X
1 0 1	LSR	RD	RX FIFO ERROR	TSR Empty	THR Empty	RX Break	RX Fram-ing Error	RX Parity Error	RX Data Over-run	RX Data Ready	LCR[7]=X
1 0 1	XFR	WR	Rsrvd	Rsrvd	Invert RS485 Control Output	Enable XonAny	LSR INT Mode	Auto RS485 INT Mode	Invert IR RX Input	Enable Half-duplex IR	LCR[7]=X
1 1 0	MSR	RD	CD	RI	DSR	CTS	Delta CD#	Delta RI#	Delta DSR#	Delta CTS#	LCR[7]=X
	IRPW	WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=X
1 1 1	SPR	RD/WR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	User Data LCR[7]=X

TABLE 8: UART CONFIGURATION REGISTERS DESCRIPTION. SHADED BITS ARE ENABLED WHEN EFR BIT-4=1.

ADDRESS A2-A0	REG NAME	READ/ WRITE	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	COMMENT
Enhanced Registers											
0 0 1	EFR	R/W	Auto CTS Enable	Auto RTS Enable	Special Char Select	Enable IER [7:4], ISR [5:4], FCR[5:4], MCR[7:5] MSR[7:4] IRPW[7:0] XTRA[7:0]	Soft-ware Flow Cntl Bit-3	Soft-ware Flow Cntl Bit-2	Soft-ware Flow Cntl Bit-1	Soft-ware Flow Cntl Bit-0	LCR=0xBF
1 0 0	XOFF1	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR=0xBF
1 0 1	XOFF2	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR=0xBF
1 1 0	XON1	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR=0xBF
1 1 1	XON2	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR=0xBF

5.10 TRANSMITTER

The transmitter section comprises of an 8-bit Transmit Shift Register (TSR) and 32 bytes of FIFO which includes a byte-wide Transmit Holding Register (THR). THR receives a data byte from the host (non-FIFO mode) or a data byte from the FIFO when the FIFO is enabled by FCR bit-0. TSR shifts out every data bit with the 16X internal clock. A bit time is 16 clock periods. The transmitter sends the start-bit followed by the number of data bits, inserts the proper parity-bit if enabled, and adds the stop-bit(s). The status of the THR and TSR are reported in the Line Status Register (LSR bit-5 and bit-6).

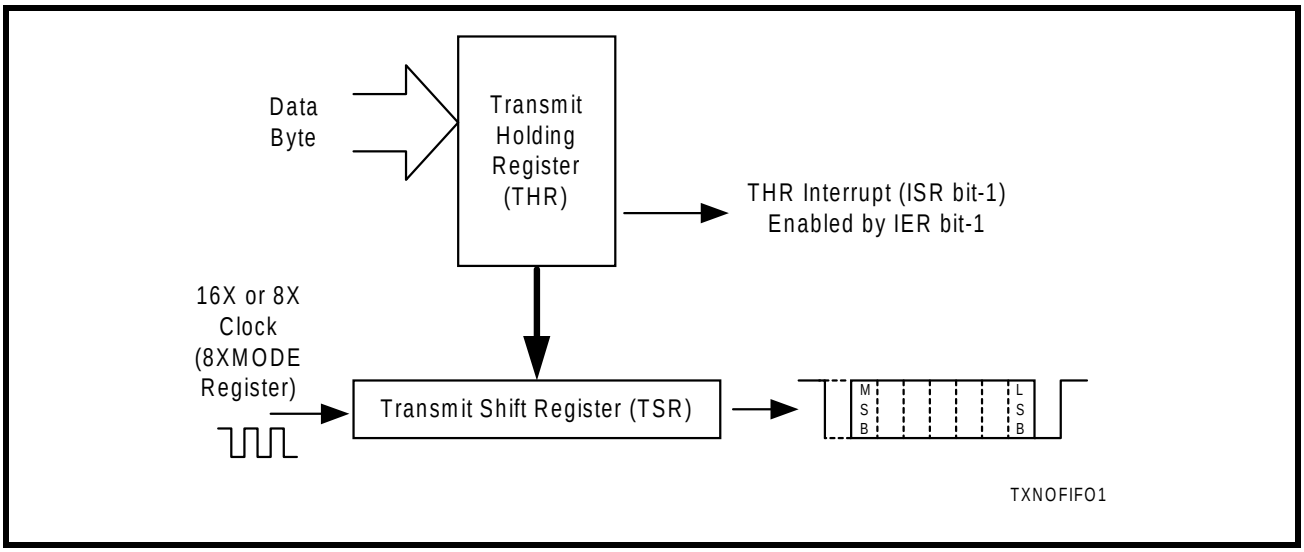
5.10.1 Transmit Holding Register (THR)

The transmit holding register is an 8-bit register providing a data interface to the host processor. The host writes transmit data byte to the THR to be converted into a serial data stream including start-bit, data bits, parity-bit and stop-bit(s). The least-significant-bit (Bit-0) becomes first data bit to go out. The THR is the input register to the transmit FIFO of 32 bytes when FIFO operation is enabled by FCR bit-0. Every time a write operation is made to the THR, its FIFO data pointer is automatically bumped to the next sequential data location. A THR empty interrupt can be generated when IER bit-1 is set to logic 1.

5.10.2 Transmitter Operation in non-FIFO Mode

The host loads transmit data to THR one character at a time. The THR empty flag (LSR bit-5) is set when the data byte is transferred to TSR. THR flag can generate a transmit empty interrupt (ISR bit-1) when it is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR becomes completely empty.

FIGURE 12. TRANSMITTER OPERATION IN NON-FIFO MODE



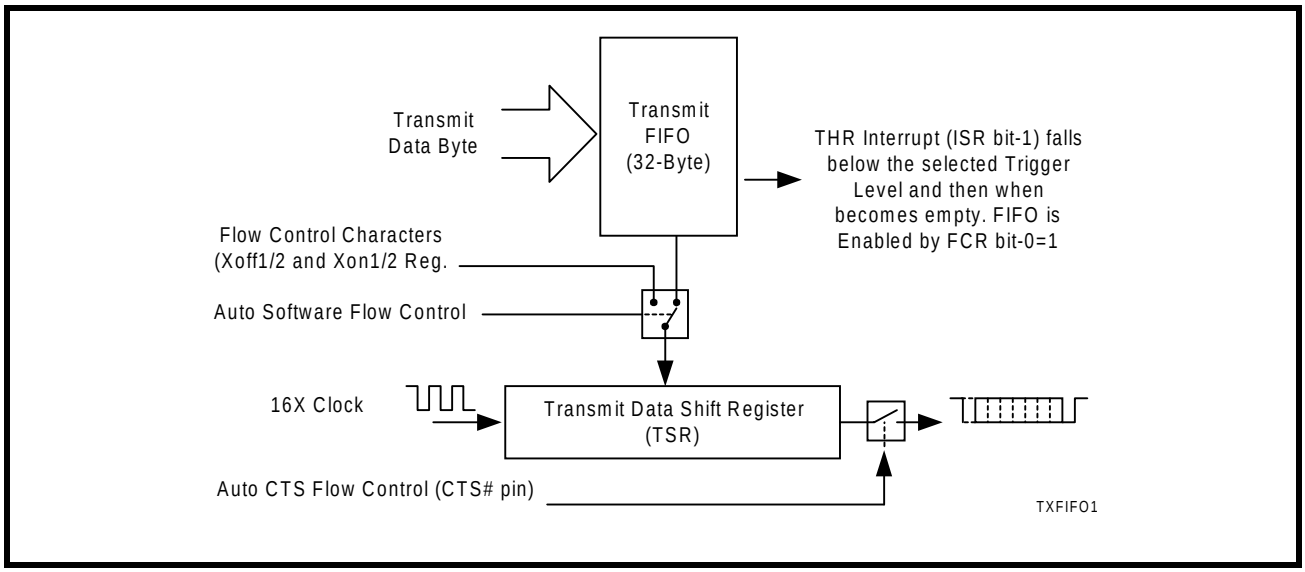
5.10.3 Transmitter Operation in FIFO Mode

The host may fill the transmit FIFO with up to 32 bytes of transmit data. The THR empty flag (LSR bit-5) is set whenever the FIFO is empty. The THR empty flag can generate a transmit empty interrupt (ISR bit-1) when the amount of data in the FIFO falls below its programmed trigger level (see TXTRG register). The transmit empty interrupt is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR/FIFO becomes empty. Furthermore, with the RS485 half-duplex direction control enabled (XFR bit-2 = 1), the source of the transmit empty interrupt changes to TSR empty instead of THR empty. This is to ensure the RTS# output is not changed until the last stop bit of the last character is shifted out.

5.10.4 Auto RS485 Half-duplex Control

The auto RS485 half-duplex direction control changes the behavior of the transmitter when enabled by XFR bit-2. It de-asserts RTS# output following the last stop bit of the last character that has been transmitted. This helps in turning around the transceiver to receive the remote station's response. The auto RS485 half-duplex direction contol also changes the transmitter empty interrupt to TSR empty instead of THR empty. When the host is ready to transmit next polling data packet again, it only has to load data bytes to the transmit FIFO. The transmitter automatically re-asserts RTS# output prior sending the data.

FIGURE 13. TRANSMIITTER OPERATION IN FIFO AND FLOW CONTROL MODE



5.11 RECEIVER

The receiver section contains an 8-bit Receive Shift Register (RSR) and 32 bytes of FIFO which includes a byte-wide Receive Holding Register (RHR). The RSR uses the 16X clock for timing. It verifies and validates every bit on the incoming character in the middle of each data bit. On the falling edge of a start or false start bit, an internal receiver counter starts counting at the 16X clock rate. After 8 clocks the start bit period should be at the center of the start bit. At this time the start bit is sampled and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. The rest of the data bits and stop bits are sampled and validated in this same manner to prevent false framing. If there were any error(s), they are reported in the LSR register bits 1- 4. Upon unloading the receive data byte from RHR, the receive FIFO pointer is bumped and the error flags are immediately updated to reflect the status of the data byte in RHR register. RHR can generate a receive data ready interrupt upon receiving a character or delay until it reaches the FIFO trigger level. Furthemore, data delivery to the host is guaranteed by a receive data ready time-out function when receive data does not reach the receive FIFO trigger level. This time-out delay is 4 word lengths as defined by LCR[1,0] plus 12 bits time. The RHR interrupt is enabled by IER bit-0.

6.0 REGISTERS

6.1 RECEIVE HOLDING REGISTER (RHR)

The receive holding register is a 8-bit register that holds a receive data byte from the receive shift register. It provides the receive data interface to the host processor. The host reads the receive data byte on this register whenever a data byte is trasferred from the RSR. The RHR register is part of the receive FIFO of 32 bytes by 11-bit wide, the 3 extra bits are for the 3 error flags to be reported in LSR register. When the FIFO is enabled by FCR bit-0, it acts as the first-out register of the FIFO as new data are put over the first-in register. Every time a read operation is made to the receive holding register, its FIFO data pointer is automatically bumped to the next sequential data location. Also, the error flags associated with the data byte are immediately updated onto the line status register (LSR) bits 2-4.

6.2 BAUD RATE GENERATOR DIVISORS (DLL AND DLM)

The Baud Rate Generator (BRG) is a 16-bit counter that generates the data rate for the transmitter. The rate is programmed through registers DLL and DLM which are only accessible when LCR bit-7 is set to ‘1’. See Programmable Baud Rate Generator section for more details.

FIGURE 14. RECEIVER OPERATION IN NON-FIFO MODE

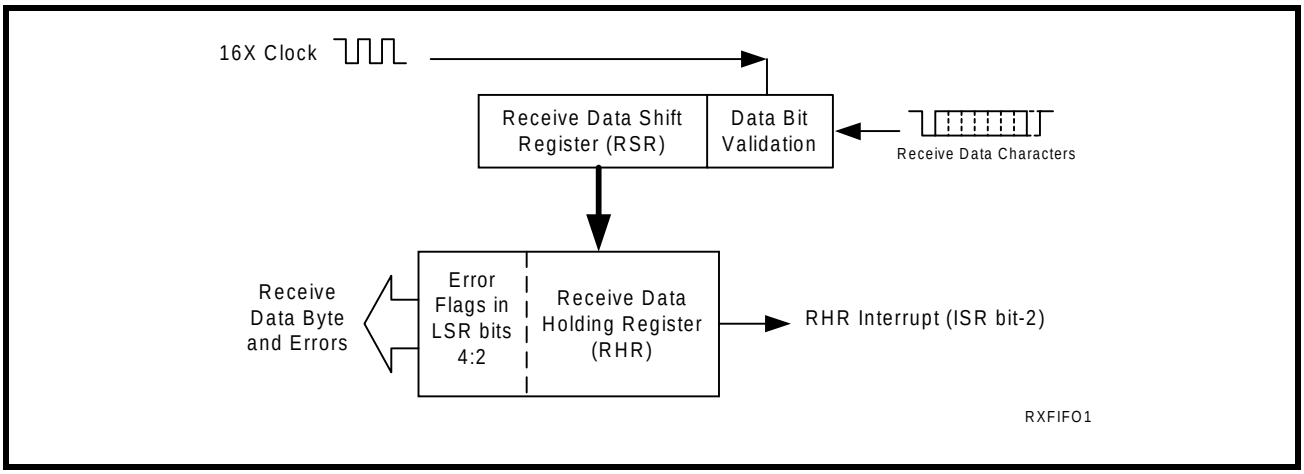
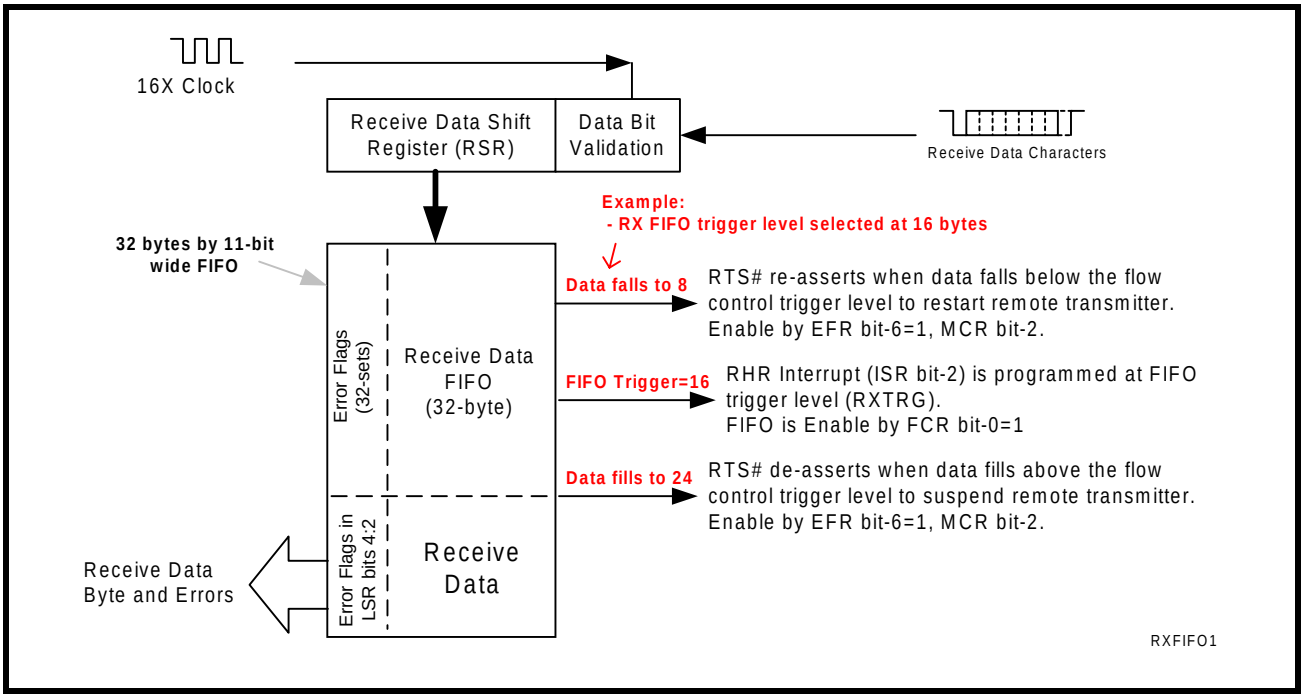


FIGURE 15. RECEIVER OPERATION IN FIFO AND AUTO RTS FLOW CONTROL MODE



6.3 INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the interrupts from receive data ready, transmit empty, line status and modem status registers. These interrupts are reported in the Interrupt Status Register (ISR) register.

6.3.1 IER versus Receive FIFO Interrupt Mode Operation

When the receive FIFO (FCR BIT-0 = a logic 1) and receive interrupts (IER BIT-0 = logic 1) are enabled, the RHR interrupts (see ISR bits 2 and 3) status will reflect the following:

A. The receive data available interrupts are issued to the host when the FIFO has reached the programmed trigger level. It will be cleared when the FIFO drops below the programmed trigger level.

B. FIFO level will be reflected in the ISR register when the FIFO trigger level is reached. Both the ISR register status bit and the interrupt will be cleared when the FIFO drops below the trigger level.

C. The receive data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift

register to the receive FIFO. It is reset when the FIFO is empty.

6.3.2 IER versus Receive/Transmit FIFO Polled Mode Operation

When FCR BIT-0 equals a logic 1 for FIFO enable; resetting IER bits 0-3 enables the XR16L651 in the FIFO polled mode of operation. Since the receiver and transmitter have separate bits in the LSR either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

A. LSR BIT-0 indicates there is data in RHR or RX FIFO.

B. LSR BIT 1-4 provides the type of receive data errors encountered for the data byte in RHR, if any.

C. LSR BIT-5 indicates THR is empty.

D. LSR BIT-6 indicates when both the transmit FIFO and TSR are empty.

E. LSR BIT-7 indicates the wire-OR function of all errors in the RX FIFO.

IER[0]: RHR Interrupt Enable

The receive data ready interrupt will be issued when RHR has a data character in the non-FIFO mode or when the receive FIFO has reached the programmed trigger level in the FIFO mode.

Logic 0 = Disable the receive data ready interrupt. (default)

Logic 1 = Enable the receiver data ready interrupt.

IER[1]: THR Interrupt Enable

This bit enables the Transmit Ready interrupt which is issued whenever the THR becomes empty or when data in the FIFO falls below the programmed trigger level.

Logic 0 = Disable Transmit Holding Register empty interrupt. (default)

Logic 1 = Enable Transmit Holding Register empty interrupt.

IER[2]: Receive Line Status Interrupt Enable

Any change of state of the LSR register bits 1,2,3 or 4 will generate an interrupt to inform the host controller about the error status of the current data byte in FIFO.

Logic 0 = Disable the receiver line status interrupt. (default)

Logic 1 = Enable the receiver line status interrupt.

IER[3]: Modem Status Interrupt Enable

Logic 0 = Disable the modem status register interrupt. (default)

Logic 1 = Enable the modem status register interrupt.

IER[4]: Sleep Mode Enable (requires EFR bit-4 = 1)

Logic 0 = Disable Sleep Mode (default).

Logic 1 = Enable Sleep Mode. See Sleep Mode section for further details.

IER[5]: Xoff Interrupt Enable (requires EFR bit-4=1)

Logic 0 = Disable the software flow control, receive Xoff interrupt. (default)

Logic 1 = Enable the software flow control, receive Xoff interrupt. See Software Flow Control section for details.

IER[6]: RTS# Output Interrupt Enable (requires EFR bit-4=1)

Logic 0 = Disable the RTS# interrupt. (default).

Logic 1 = Enable the RTS# interrupt. The UART issues an interrupt when the RTS# pin makes a transition.

IER[7]: CTS# Input Interrupt Enable (requires EFR bit-4=1)

Logic 0 = Disable the CTS# interrupt. (default).

Logic 1 = Enable the CTS# interrupt. The UART issues an interrupt when CTS# pin makes a transition.

6.4 Interrupt Status Register (ISR)

The UART provides multiple levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with six interrupt status bits. Performing a read cycle on the ISR will give the user the current highest pending interrupt level to be serviced, others queue up for next service. No other interrupts are acknowledged until the pending interrupt is serviced. The Interrupt Source Table, Table 9, shows the data values (bit 0-5) for the six prioritized interrupt levels and the interrupt sources associated with each of these interrupt levels.

6.4.1 Interrupt Generation:

- LSR is by any of the LSR bits 1, 2, 3 and 4.
- RXRDY is by RX trigger level.
- RXRDY Time-out is by the a 4-char plus 12 bits delay timer if data doesn't reach FIFO trigger level.
- TXRDY is by LSR bit-5 (or bit-6 in auto RS485 control).
- MSR is by any of the MSR bits, 0, 1, 2 and 3.
- Receive Xoff/Special character is by detection of a Xoff or Special character.

- CTS# is by a change of state on the input pin with auto flow control enabled, EFR bit-7, and depending on selection on MCR bit-2.
- RTS# is when its receiver changes the state of the output pin during auto RTS flow control enabled by EFR bit-6 and selection of MCR bit-2.

6.4.2 Interrupt Clearing:

- LSR interrupt is cleared by a read to the LSR register.
- RXRDY and RXRDY Time-out are cleared by reading data until FIFO falls below the trigger level.
- TXRDY interrupt is cleared by a read to the ISR register.
- MSR interrupt is cleared by a read to the MSR register.
- Xoff or Special character interrupt is cleared by a read to ISR.
- RTS# and CTS# status change interrupts are cleared by a read to the MSR register.

TABLE 9: INTERRUPT SOURCE AND PRIORITY LEVEL

PRIORITY LEVEL	ISR REGISTER STATUS BITS						SOURCE OF INTERRUPT+
	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	
1	0	0	0	1	1	0	LSR (Receiver Line Status Register)
2	0	0	0	1	0	0	RXRDY (Received Data Ready)
3	0	0	1	1	0	0	RXRDY (Receive Data Time-out)
4	0	0	0	0	1	0	TXRDY (Transmitter Holding Register Empty)
5	0	0	0	0	0	0	MSR (Modem Status Register)
6	0	1	0	0	0	0	RXRDY (Received Xoff or Special character)
7	1	0	0	0	0	0	CTS#/DSR#, RTS#/DTR# change of state
-	0	0	0	0	0	1	None (default)

ISR[0]: Interrupt Status

Logic 0 = An interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.

Logic 1 = No interrupt pending. (default condition)

ISR[3:1]: Interrupt Status

These bits indicate the source for a pending interrupt at interrupt priority levels 1, 2, 3 and 4 (See Interrupt Source Table 9).

ISR[5:4]: Interrupt Status

These bits are enabled when EFR bit-4 is set to a logic 1. ISR bit-4 indicates that the receiver detected a data match of the Xoff character(s).

NOTE: *Note that once set to a logic 1, the ISR bit-4 will stay a logic 1 until a Xon character is received. ISR bit-5 indicates that CTS# or RTS# has changed state.*

ISR[7:6]: FIFO Enable Status

These bits are set to a logic 0 when the FIFOs are disabled. They are set to a logic 1 when the FIFOs are enabled.

6.5 FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the transmit/receive FIFO trigger levels, and select the DMA mode. The DMA, and FIFO modes are defined as follows:

FCR BIT-0: TX and RX FIFO Enable

Logic 0 = Disable the transmit and receive FIFO. (default).

Logic 1 = Enable the transmit and receive FIFOs. This bit must be set to logic 1 when other FCR bits are written or they will not be programmed.

FCR[1]: RX FIFO Reset

This bit is only active when FCR bit-0 is a ‘1’.

Logic 0 = No receive FIFO reset. (default)

Logic 1 = Reset the receive FIFO pointers and FIFO level counter logic (the receive shift register is not cleared or altered). This bit will return to a logic 0 after resetting the FIFO.

FCR[2]: TX FIFO Reset

This bit is only active when FCR bit-0 is a ‘1’.

Logic 0 = No transmit FIFO reset. (default)

Logic 1 = Reset the transmit FIFO pointers and FIFO level counter logic (the transmit shift register is not cleared or altered). This bit will return to a logic 0 after resetting the FIFO.

FCR[3]: DMA Mode Select

Controls the behavior of the -TXRDY and -RXRDY pins. See DMA operation section for details.

Logic 0 = Set DMA to mode 0. (default)

Logic 1 = Set DMA to mode 1.

FCR[5:4]: Transmit FIFO Trigger Select

(logic 0 = default, TX trigger level = one)

These 2 bits set the trigger level for the transmit FIFO interrupt. The UART will issue a transmit interrupt when the number of characters in the FIFO falls below the selected trigger level, or when it gets empty in case that the FIFO did not get filled over the trigger level on last re-load. Table 10 below shows the selections. EFR bit-4 must be set to '1' before these bits can be accessed.

FCR[7:6]: Receive FIFO Trigger Select

(logic 0 = default, RX trigger level =1).

The FCTR Bits 6-7 are associated with these 2 bits. These 2 bits are used to set the trigger level for the receiver FIFO interrupt. Table 10 shows the complete selections.

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TABLE 10: TRANSMIT AND RECEIVE FIFO TRIGGER LEVEL SELECTION WITH AUTO RTS HYSTERESIS

FCR BIT-7	FCR BIT-6	FCR BIT-5	FCR BIT-4	TRANSMIT INT TRIGGER LEVEL	RECEIVE INT TRIGGER LEVEL	AUTO RTS DE-ASSERT	AUTO RTS RE-ASSERT	COMPATIBILITY
		0	0	16				16C650A compatible.
		0	1	8				
		1	0	24				
		1	1	30				
0	0				8	16	0	
0	1				16	24	8	
1	0				24	28	16	
1	1				28	28	24	

6.6 LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The word or character length, the number of stop bits, and the parity are selected by writing the appropriate bits in this register.

LCR[1-0]: TX and RX Word Length Select

These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	WORD LENGTH
0	0	5 (default)
0	1	6
1	0	7
1	1	8

LCR[2]: TX and RX Stop-bit Length Select

The length of stop bit is specified by this bit in conjunction with the programmed word length.

BIT-2	WORD LENGTH	STOP BIT LENGTH (BIT TIME(S))
0	5,6,7,8	1 (default)
1	5	1-1/2
1	6,7,8	2

LCR[3]: TX and RX Parity Select

Parity or no parity can be selected via this bit. The parity bit is a simple way used in communications for data integrity check. See Table 11 for parity selection summary below.

- Logic 0 = No parity.
- Logic 1 = A parity bit is generated during the transmission while the receiver checks for parity error of the data character received.

LCR[4]: TX and RX Parity Select

If the parity bit is enabled with LCR bit-3 set to a logic 1, LCR BIT-4 selects the even or odd parity format. Logic 0 = ODD Parity is generated by forcing an odd number of logic 1's in the transmitted character. The receiver must be programmed to check the same format. (default).

- Logic 1 = EVEN Parity is generated by forcing an even the number of logic 1's in the transmitted character. The receiver must be programmed to check the same format.

LCR[5]: TX and RX Parity Select

If the parity bit is enabled, LCR BIT-5 selects the forced parity format.

- LCR BIT-5 = logic 0, parity is not forced. (default)
- LCR BIT-5 = logic 1 and LCR BIT-4 = logic 0, parity bit is forced to a logical 1 for the transmit and receive data.
- LCR BIT-5 = logic 1 and LCR BIT-4 = logic 1, parity bit is forced to a logical 0 for the transmit and receive data.

TABLE 11: PARITY SELECTION

LCR BIT-5	LCR BIT-4	LCR BIT-3	PARITY SELECTION
X	X	0	No parity
0	0	1	Odd parity
0	1	1	Even parity
1	0	1	Force parity to mark, "1"
1	1	1	Forced parity to space, "0"

LCR[6]: Transmit Break Enable

- When enabled the Break control bit ~~it~~ causes a break condition to be transmitted (the TX output is forced to a "space', logic 0, state). This condition remains until disabled by setting LCR bit-6 to a logic 0.
- Logic 0 = No TX break condition. (default)
- Logic 1 = Forces the transmitter output (TX) to a "space", logic 0, for alerting the remote receiver of a line break condition.

LCR[7]: Baud Rate Divisors Enable

Baud rate generator divisor (DLL/DLM) enable.

- Logic 0 = Data registers are selected. (default)
- Logic 1 = Divisor latch registers are selected.

6.7 MODEM CONTROL REGISTER (MCR) OR GENERAL PURPOSE OUTPUTS CONTROL.

The MCR register is used for controlling the serial/modem interface signals or general purpose inputs/outputs.

MCR[0]: DTR# Pins

The DTR# pin is a modem control output. If the modem interface is not used, this output may be used for general purpose.

- Logic 0 = Force DTR# output to a logic 1. (default)
- Logic 1 = Force DTR# output to a logic 0.

MCR[1]: RTS# Pins

The RTS# pin is a modem control output and may be used for automatic hardware flow control by enabled by EFR bit-6. If the modem interface is not used, this output may be used for general purpose.

- Logic 0 = Force RTS# output to a logic 1. (default)
- Logic 1 = Force RTS# output to a logic 0.

MCR[2]: OP1# Output

OP1# is a general purpose output.

- Logic 0 = OP1# output is at logic 1.
- Logic 1 = OP1# output is at logic 0

MCR[3]: OP2# or IRQn Enable during PC Mode

OP2# is a general purpose output available during the Intel or Motorola bus interface mode of operation. In the PC bus mode, it enables the IRQn operation. See PC Mode section.

During Intel or Motorola Bus Mode Operation:

- Logic 0 = OP2# output is at logic 1.
- Logic 1 = OP2# output is at logic 0.

During PC Mode Operation:

- Logic 0 = Disable IRQn operation. (default).
- Logic 1 = Enable IRQn operation.

MCR[4]: Internal Loopback Enable

- Logic 0 = Disable loopback mode. (default)
- Logic 1 = Enable local loopback mode, see loopback section and Figure 11.

MCR[5]: Active/Tristate Interrupt Output Enable

- Logic 0 = Enable active or tristate interrupt output (default).
- Logic 1 = Enable open source interrupt output mode. See Table 2 for detailed information.

MCR[6]: Infrared Encoder/Decoder Enable

Logic 0 is the default unless the IR mode is forced by the ENIR pin. This bit can overwrite the ENIR state after a power up or reset.

- Logic 0 = Enable the standard modem receive and transmit input/output interface. (Default)
- Logic 1 = Enable infrared IrDA receive and transmit inputs/outputs. The TX/RX output/input are routed to the infrared encoder/decoder. The data input and output levels conform to the IrDA infrared interface requirement. The infrared TX output is at logic 0 during idle condition. The infrared receive data input polarity is also logic 0, however, it may be inverted when using an infrared modules that provides inverted signal output. Use register XFR bit-1 to invert the receive input signal level going to the infrared decoder. Also see XFR bit-0 for half-duplex operation where the receiver can be disabled while transmiting.

MCR[7]: Clock Prescaler Select

- Logic 0 = Divide by one. The input clock from the crystal or external clock is fed directly to the Programmable Baud Rate Generator without further modification, i.e., divide by one. (default).
- Logic 1 = Divide by four. The prescaler divides the input clock from the crystal or external clock by four and feeds it to the Programmable Baud Rate Generator, hence, data rates become one forth.

6.8 Line Status Register (LSR) - Read Only

This register provides the status of data transfers between the UART and the host.

LSR[0]: Receive Data Ready Indicator

- Logic 0 = No data in receive holding register or FIFO. (default).
- Logic 1 = Data has been received and is saved in the receive holding register or FIFO.

LSR[1]: Receiver Overrun Flag

- Logic 0 = No overrun error. (default)
- Logic 1 = Overrun error. A data overrun error condition occurred in the receive shift register. This happens when additional data arrives while the FIFO is full. In this case the previous data in the receive shift register is overwritten. Note that under this condition the data byte in the receive shift register is not transferred into the FIFO, therefore the data in the FIFO is not corrupted by the error.

LSR[2]: Receive Data Parity Error Flag

- Logic 0 = No parity error. (default)
- Logic 1 = Parity error. The receive character in RHR does not have correct parity information and is suspect. This error is associated with the character available for reading in RHR.

LSR[3]: Receive Data Framing Error Flag

- Logic 0 = No framing error. (default)
- Logic 1 = Framing error. The receive character did not have a valid stop bit(s). This error is associated with the character available for reading in RHR.

LSR[4]: Receive Break Flag

- Logic 0 = No break condition. (default)
- Logic 1 = The receiver received a break signal (RX was a logic 0 for at least one character frame time). In the FIFO mode, only one break character is loaded into the FIFO. The break indication remains

until the RX input returns to the idle condition, "mark" or logic 1.

LSR[5]: Transmit Holding Register Empty Flag

This bit is the Transmit Holding Register Empty indicator. This bit indicates that the transmitter is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the host when the THR interrupt enable is set. The THR bit is set to a logic 1 when the last data byte is transferred from the transmit holding register to the transmit shift register. The bit is reset to logic 0 concurrently with the data loading to the transmit holding register by the host. In the FIFO mode this bit is set when the transmit FIFO is empty, it is cleared when the transmit FIFO contains at least 1 byte.

LSR[6]: Transmit Shift Register Empty Flag

This bit is the Transmit Shift Register Empty indicator. This bit is set to a logic 1 whenever the transmitter goes idle. It is set to logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode this bit is set to one whenever the transmit FIFO and transmit shift register are both empty.

LSR[7]: Receive FIFO Data Error Flag

- Logic 0 = No FIFO error. (default)
- Logic 1 = A global indicator for the sum of all error bits in the RX FIFO. At least one parity error, framing error or break indication is in the FIFO data. This bit clears when there is no more error(s) in the FIFO.

6.9 Extra Feature Register (XFR) - Write Only

This register provides additonal features and controls to the XR16L651 UART.

XFR [0]: Half-duplex Infrared Mode Enable

When infrared mode is enabled, MCR bit-6=1, this bit selects the infrared mode to operate in normal full-duplex or half-duplex mode. This half-duplex mode feature is very desirable when user does not want to "see" his own sending data that are echoed through the reflection of lights.

- Logic 0 = Disable. The receiver is active during data transmission.
- Logic 1 = Enabled half-duplex operation. The infrared receiver is disabled during data transmission.

XFR [1]: Invert Received Infrared Input Signal

This bit controls the input polarity of the infrared data.

- Logic 0 = Infrared data input idles at logic 0. (default)
- Logic 1 = Infrared data idles at logic 1, pulses low.

XFR [2]: Auto RS485 Enable

This bit enables the auto RS485 direction control feature for half-duplex operation with RS-485 transceiver. The feature should only be enabled when normal RTS# output and auto RTS flow control are not in used.

- Logic 0 = Disable the auto RS485 direction control function. This allows normal RTS# output or auto RTS flow control operation.
- Logic 1 = Enable the auto RS485 direction function. The RTS# output will automatically change its logic state to control the RS-485 transceiver from sending and receiving. Also see XFR bit-5 and section 5.6.3.

XFR [3]: LSR Bad Data Interrupt Operation

When the LSR interrupt is enabled, IER bit-2=1, this bit selects when the interrupt pin (INT) will report received character error: parity, framing or break. Use this feature only if application needs immediate knowledge when a bad character is received.

- Logic 0 = Received data error interrupt (LSR interrupt) will be generated when the bad character is available for reading from the FIFO. This is compatible to industry standard 16C550 operation.
- Logic 1 = Received data error interrupt (LSR interrupt) is generated immediately upon receipt of the bad character. It will be reset when LSR is read. If user does not read the bad character out, another bad character interrupt is generated when it's available for reading from the FIFO.

XFR [4]: XonAny Enable

This bit enables and disables the Xon-Any function when Xon/Xoff software flow control is enabled.

- Logic 0 = Disable the Xon-Any function.
- Logic 1 = Enable the Xon-Any function. The receiver will use any received character as an Xon character and resume data transmission.

XFR [5]: Invert Auto RS-485 Control Output

When Auto RS485 feature is enabled, XFR bit-2=1, RTS# output automatically changes its logic state to control the RS-485 transceiver.

- Logic 0 = During auto RS-485, RTS# control output signal to the transceiver is logic 1 for transmit and logic 0 for receive.
- Logic 1 = The RTS# output control signal to the transceiver is logic 0 for transmit and logic 1 for receive. User must assert RTS# for operation to take effect.

XFR [7:6]

Not used, reserved.

6.10 Modem Status Register (MSR) - Read Only

This register provides the current state of the modem interface signals, or other peripheral device that the UART is connected. Lower four bits of this register are used to indicate the changed information. These bits are set to a logic 1 whenever a signal from the modem changes state. These bits may be used as general purpose inputs/outpus when they are not used with modem signals.

MSR[0]: Delta CTS# Input Flag

- Logic 0 = No change on CTS# input (default).
- Logic 1 = The CTS# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3.

MSR[1]: Delta DSR# Input Flag

- Logic 0 = No change on DSR# input (default).
- Logic 1 = The DSR# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3.

MSR[2]: Delta RI# Input Flag

- Logic 0 = No change on RI# input (default).
- Logic 1 = The RI# input has changed from a logic 0 to a logic 1, ending of the ringing signal. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3.

MSR[3]: Delta CD# Input Flag

- Logic 0 = No change on CD# input (default).
- Logic 1 = Indicates that the CD# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3.

MSR[4]: CTS Input Status

CTS# pin may function as automatic hardware flow control signal input if it is enabled and selected by Auto CTS (EFR bit-7). Auto CTS flow control allows starting and stopping of local data transmissions based on the modem CTS# signal. A logic 1 on the CTS# pin will stop UART transmitter as soon as the current character has finished transmission, and a logic 0 will resume data transmission. Normally MSR bit-4 bit is the compliment of the CTS# input. However in the loopback mode, this bit is equivalent to the RTS# bit in the MCR register. The CTS# input may be used as a general purpose input when the modem interface is not used.

MSR[5]: DSR Input Status

DSR# (active high, logical 1). Normally this bit is the compliment of the DSR# input. In the loopback mode, this bit is equivalent to the DTR# bit in the MCR register. The DSR# input may be used as a general purpose input when the modem interface is not used.

MSR[6]: RI Input Status

RI# (active high, logical 1). Normally this bit is the compliment of the RI# input. In the loopback mode this bit is equivalent to bit-2 in the MCR register. The RI# input may be used as a general purpose input when the modem interface is not used.

MSR[7]: CD Input Status

CD# (active high, logical 1). Normally this bit is the compliment of the CD# input. In the loopback mode this bit is equivalent to bit-3 in the MCR register. The CD# input may be used as a general purpose input when the modem interface is not used.

6.11 Infrared Transmit Pulse Width Control Register (IRPW) - Write Only

The IRPW register allows the user to program the the encoder's pulse width. This cuts the LED on-time, hence, reducing power consumption.

IRPW [7:0]: Pulse width control.

A 0x00 value (default) will set the pulse width to normal width of 3/16 of the data bit rate. The programmable infrared pulse width can be calculated using the following equation:

Infrared pulse width (PW) = Crystal clock period x 'N', where 'N' is the value in IRPW from 1 to 255.

Examples:

Crystal frequency = 14.7456MHz (clock period of 67.82ns)

PW = 67.82 x 'N' or ranges from 67.82ns to 17.29ms

Caution: Never allow PW to exceed the operating data rate bit period, else the encoder stops.

6.12 Scratch Pad Register (SPR)

This is a 8-bit general purpose register for the user to store temporary data. The content of this register is preserved during sleep mode but becomes 0xFF (default) after a reset or a power off-on cycle.

6.13 Baud Rate Generator Registers (DLL and DLM)

The concatenation of the contents of DLM and DLL gives the 16-bit divisor value which is used to calculate the baud rate:

- Baud Rate = (Clock Frequency / 16) / Divisor

See MCR bit-7 and the baud rate table also.

6.14 Device Identification Register (DVID) - Read Only

This register contains the device ID (0x04 for XR16L651). Prior to reading this register, DLL and DLM should be set to 0x00.

6.15 Device Revision Register (DREV) - Read Only

This register contains the device revision information. For example, 0x01 means revision A. Prior to reading this register, DLL and DLM should be set to 0x00.

6.16 Enhanced Feature Register (EFR)

Enhanced features are enabled or disabled using this register. Bit 0-3 provide single or dual consecutive character software flow control selection (see Table 12). When the Xon1 and Xon2 and Xoff1 and Xoff2 modes are selected, the double 8-bit words are concatenated into two sequential characters. Caution: note that whenever changing the TX or RX flow control bits, always reset all bits back to logic 0 (disable) before programming a new setting.

EFR BIT 0-3: Software Flow Control Select

Combinations of software flow control can be selected by programming these bits.

Table 12: Software Flow Control Functions

EFR bit-3 Cont-3	EFR bit-2 Cont-2	EFR bit-1 Cont-1	EFR bit-0 Cont-0	Transmit and Receive Software Flow Control
0	0	0	0	No TX and RX flow control (default and reset)
0	0	X	X	No transmit flow control
1	0	X	X	Transmit Xon1/Xoff1
0	1	X	X	Transmit Xon2/Xoff2
1	1	X	X	Transmit Xon1 and Xon2/Xoff1 and Xoff2
X	X	0	0	No receive flow control
X	X	1	0	Receiver compares Xon1/Xoff1
X	X	0	1	Receiver compares Xon2/Xoff2
1	0	1	1	Transmit Xon1/ Xoff1, Receiver compares Xon1 or Xon2, Xoff1 or Xoff2
0	1	1	1	Transmit Xon2/Xoff2, Receiver compares Xon1 or Xon2, Xoff1 or Xoff2
1	1	1	1	Transmit Xon1 and Xon2/Xoff1 and Xoff2, Receiver compares Xon1 and Xon2/Xoff1 and Xoff2
0	0	1	1	No transmit flow control, Receiver compares Xon1 and Xon2/Xoff1 and Xoff2

EFR[4]: Enhanced Function Bits Enable

Enhanced function control bit. This bit enables IER bits 4-7, ISR bits 4-5, FCR bits 4-5, MCR bits 5-7, XFR bits 0-7 and IRPW bits 0-7 to be modified. After modifying any enhanced bits, EFR bit-4 can be set to a logic 0 to latch the new values. This feature prevents legacy software from altering or overwriting the enhanced functions once set. Normally, it is recommended to leave it enabled, logic 1.

- Logic 0 = modification disable/latch enhanced features. IER bits 4-7, ISR bits 4-5, FCR bits 4-5, MCR bits 5-7, XFR bits 0-7 and IRPW bits 0-7 are saved to retain the user settings. After a reset, the IER bits 4-7, ISR bits 4-5, FCR bits 4-5, MCR bits 5-7, XFR bits 0-7 and IRPW bits 0-7 are set to a logic 0 to be compatible with ST16C554 mode. (default).
- Logic 1 = Enables the above-mentioned register bits to be modified by the user.

EFR[5]: Special Character Detect Enable

- Logic 0 = Special Character Detect Disabled. (default)
- Logic 1 = Special Character Detect Enabled. The UART compares each incoming receive character

with data in Xoff-2 register. If a match exists, the received data will be transferred to FIFO and ISR bit-4 will be set to indicate detection of the special character. Bit-0 corresponds with the LSB bit for the receive character. If flow control is set for comparing Xon1, Xoff1 (EFR [1:0]=10) then flow control and special character work normally. However, if flow control is set for comparing Xon2, Xoff2 (EFR[1:0]=01) then flow control works normally, but Xoff2 will not go to the FIFO, and will generate an Xoff interupt and a special character interrupt.

EFR[6]: Auto RTS Flow Control Enable

RTS# output may be used for hardware flow control by setting EFR bit-6 to logic 1. When Auto RTS is selected, an interrupt will be generated when the receive FIFO is filled to the programmed trigger level and RTS de-asserts to a logic 1 at the next upper trigger level. RTS# will return to a logic 0 when FIFO data falls below the next lower trigger level. The RTS# output must be asserted (logic 0) before the auto RTS can take effect. RTS# pin will function as a general purpose output when hardware flow control is disabled.

- Logic 0 = Automatic RTS flow control is disabled. (default)
- Logic 1 = Enable Automatic RTS flow control.

EFR[7]: Auto CTS Flow Control Enable

Automatic CTS Flow Control.

- Logic 0 = Automatic CTS flow control is disabled. (default)
- Logic 1 = Enable Automatic CTS flow control. Data transmission stops when CTS# input de-asserts to logic 1. Data transmission resumes when CTS# input returns to a logic 0.

TABLE 13: UART RESET CONDITIONS

REGISTERS	RESET STATE
DLL	Bits 7-0 = 0xXX
DLM	Bits 7-0 = 0xXX
RHR	Bits 7-0 = 0xXX
THR	Bits 7-0 = 0xXX
IER	Bits 7-0 = 0x00
FCR	Bits 7-0 = 0x00
ISR	Bits 7-0 = 0x01
LCR	Bits 7-0 = 0x00
MCR	Bits 7-0 = 0x00
LSR	Bits 7-0 = 0x60
XFR	Bits 7-0 = 0x00
MSR	Bits 3-0 = logic 0 Bits 7-4 = logic levels of the inputs
IRPW	Bits 7-0 = 0x00
SPR	Bits 7-0 = 0xFF
EFR	Bits 7-0 = 0x00
XON1	Bits 7-0 = 0x00
XON2	Bits 7-0 = 0x00
XOFF1	Bits 7-0 = 0x00
XOFF2	Bits 7-0 = 0x00
I/O SIGNALS	**RESET STATE**
TX	Normal = logic 1 Infrared = logic 0
RTS#	Logic 1
DTR#	Logic 1

ABSOLUTE MAXIMUM RATINGS

Power Supply Range	7 Volts
Voltage at Any Pin	-0.5 to 7V
Operating Temperature	-40^{o} to +85^{o}C
Storage Temperature	-65^{o} to +150^{o}C
Package Dissipation	500 mW
Thermal Resistance (7x7x1.4mm 48-TQFP)	theta-ja = 59^{o}C/W, theta-jc = 16^{o}C/W

ELECTRICAL CHARACTERISTICS (PRELIMINARY)

DC ELECTRICAL CHARACTERISTICS FOR 2.5V SIGNALING

UNLESS OTHERWISE NOTED: TA=0^{O} TO 70^{O}C (-40^{O} TO +85^{O}C FOR INDUSTRIAL GRADE PACKAGE), VCC IS 2.5 +/- 10%

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITION	NOTES
V_{IL}	Input Low Voltage	-0.3	0.6	V		
V_{IH}	Input High Voltage	2.0	6.0	V		
V_{OL}	Output Low Voltage		TBD	V		
V_{OH}	Output High Voltage	TBD		V		
I_{IL}	Input Low Leakage Current		+/-10	uA		
I_{IH}	Input High Leakage Current		+/-10	uA		
C_{IN}	Input Pin Capacitance		5	pF		
I_{CC}	Power Supply Current		1.0	mA	Crystal or external clock of 12MHz	
I_{SLEEP}	Sleep Current		100	uA	UART at asleep. A2-A0 at GND, all inputs at VCC or GND	

AC ELECTRICAL CHARACTERISTICS FOR 2.5V SIGNALLING

UNLESS OTHERWISE NOTED: TA=0^{O} TO 70^{O}C (-40^{O} TO +85^{O}C FOR INDUSTRIAL GRADE PACKAGE), VCC IS 2.5V +/- 10%

SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTES
OSC	Crystal Oscillator		16	MHz	
CLK	External Clock		24	MHz	
TAS	Address Valid to CS# Asserted	15		ns	
TAH	CS# De-asserted to Address Invalid	10		ns	
TDLY	Delay between CS# Active Cycles (16 Mode)	50		ns	
TRD	Read Strobe Width (16 Mode)	50		ns	
TWR	Write Strobe Width (16 Mode)	50		ns	
TDA	Read/Write Asserted to Data Valid		50	ns	
TDH	Read/Write De-asserted to Data Invalid	50		ns	
TRWS	R/W# Valid to CS# Valid (68 Mode)	TBD		ns	
TRWH	CS# De-asserted to R/W# De-asserted (68 Mode)	TBD		ns	
TCSL	CS# Active Width	TBD		ns	
TCSH	CS# Inactive Width	TBD		ns	
T17D	Delay from IOW# to output		50	ns	
T18D	Delay to set Interrupt from Modem Input		50	ns	
T19D	Delay to reset Interrupt from IOR#		50	ns	

DC ELECTRICAL CHARACTERISTICS FOR 3.3V SIGNALING

UNLESS OTHERWISE NOTED: TA=0^{O} TO 70^{O}C (-40^{O} TO +85^{O}C FOR INDUSTRIAL GRADE PACKAGE), VCC IS 3.3V +/- 10%

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITION	NOTES
V_{IL}	Input Low Voltage	-0.3	0.8	V		
V_{IH}	Input High Voltage	2.0	6.0	V		
V_{OL}	Output Low Voltage		TBD	V		
V_{OH}	Output High Voltage	TBD		V		
I_{IL}	Input Low Leakage Current		+/-10	uA		
I_{IH}	Input High Leakage Current		+/-10	uA		
C_{IN}	Input Pin Capacitance		5	pF		
I_{CC}	Power Supply Current		1.0	mA	Crystal or external clock of 16MHz	
I_{SLEEP}	Sleep Current		100	uA	UART at asleep. A2-A0 at GND, all inputs at VCC or GND	

AC ELECTRICAL CHARACTERISTICS FOR 3.3V SIGNALING

UNLESS OTHERWISE NOTED: TA=0^{O} TO 70^{O}C (-40^{O} TO +85^{O}C FOR INDUSTRIAL GRADE PACKAGE), VCC IS 3.3V +/- 10%

SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTES
OSC	Crystal Oscillator		20	MHz	
CLK	External Clock		33	MHz	
TAS	Address Valid to CS# Asserted	15		ns	
TAH	CS# De-asserted to Address Invalid	10		ns	
TDLY	Delay between CS# Active Cycles (16 Mode)	50		ns	
TRD	Read Strobe Width (16 Mode)	50		ns	
TWR	Write Strobe Width (16 Mode)	50		ns	
TDA	Read/Write Asserted to Data Valid		50	ns	
TDH	Read/Write De-asserted to Data Invalid	50		ns	
TRWS	R/W# Asserted to CS# Asserted (68 Mode)	TBD		ns	
TRWH	CS# De-asserted to R/W# De-asserted (68 Mode)	TBD		ns	
TCSL	CS# Active Width	TBD		ns	
TCSH	CS# Inactive Width	TBD		ns	
T17d	Delay from IOW# to output		50	ns	
T18d	Delay to set Interrupt from Modem Input		50	ns	
T19d	Delay to reset Interrupt from IOR#		50	ns	

DC ELECTRICAL CHARACTERISTICS FOR 5.0V SIGNALING

UNLESS OTHERWISE NOTED: TA=0^{O} TO 70^{O}C (-40^{O} TO +85^{O}C FOR INDUSTRIAL GRADE PACKAGE), VCC IS 5.0V +/- 10%

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITION	NOTES
V_{IL}	Input Low Voltage	-0.5	0.8	V		
V_{IH}	Input High Voltage	2.0	6.0	V		
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 6 mA	
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -6 mA	
I_{IL}	Input Low Leakage Current		+/-10	uA		
I_{IH}	Input High Leakage Current		+/-10	uA		
C_{IN}	Input Pin Capacitance		5	pF		
I_{CC}	Power Supply Current		1.3	mA	Crystal or external clock of 24MHz	
I_{SLEEP}	Sleep Current		100	uA	UART at asleep. A2-A0 at GND, all inputs at VCC or GND	

AC ELECTRICAL CHARACTERISTICS FOR 5.0V SIGNALING

UNLESS OTHERWISE NOTED: TA=0^{O} TO 70^{O}C (-40^{O} TO +85^{O}C FOR INDUSTRIAL GRADE PACKAGE), VCC IS 5.0V +/- 10%

SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTES
OSC	Crystal Oscillator		24	MHz	
CLK	External Clock		50	MHz	
TAS	Address Valid to CS# Asserted	15		ns	
TAH	CS# De-asserted to Address Invalid	10		ns	
TDLY	Delay between CS# Active Cycles (16 Mode)	50		ns	
TRD	Read Strobe Width (16 Mode)	50		ns	
TWR	Write Strobe Width (16 Mode)	50		ns	
TDA	Read/Write Asserted to Data Valid		50	ns	
TDH	Read/Write De-asserted to Data Invalid	50		ns	
TRWS	R/W# Asserted to CS# Asserted (68 Mode)	TBD		ns	
TRWH	CS# De-asserted to R/W# De-asserted (68 Mode)	TBD		ns	
TCSL	CS# Active Width	TBD		ns	
TCSH	CS# Inactive Width	TBD		ns	
T17d	Delay from IOW# to output		50	ns	
T18d	Delay to set Interrupt from Modem Input		50	ns	
T19d	Delay to reset Interrupt from IOR#		50	ns	

FIGURE 16. INTEL DATA BUS READ AND WRITE TIMING

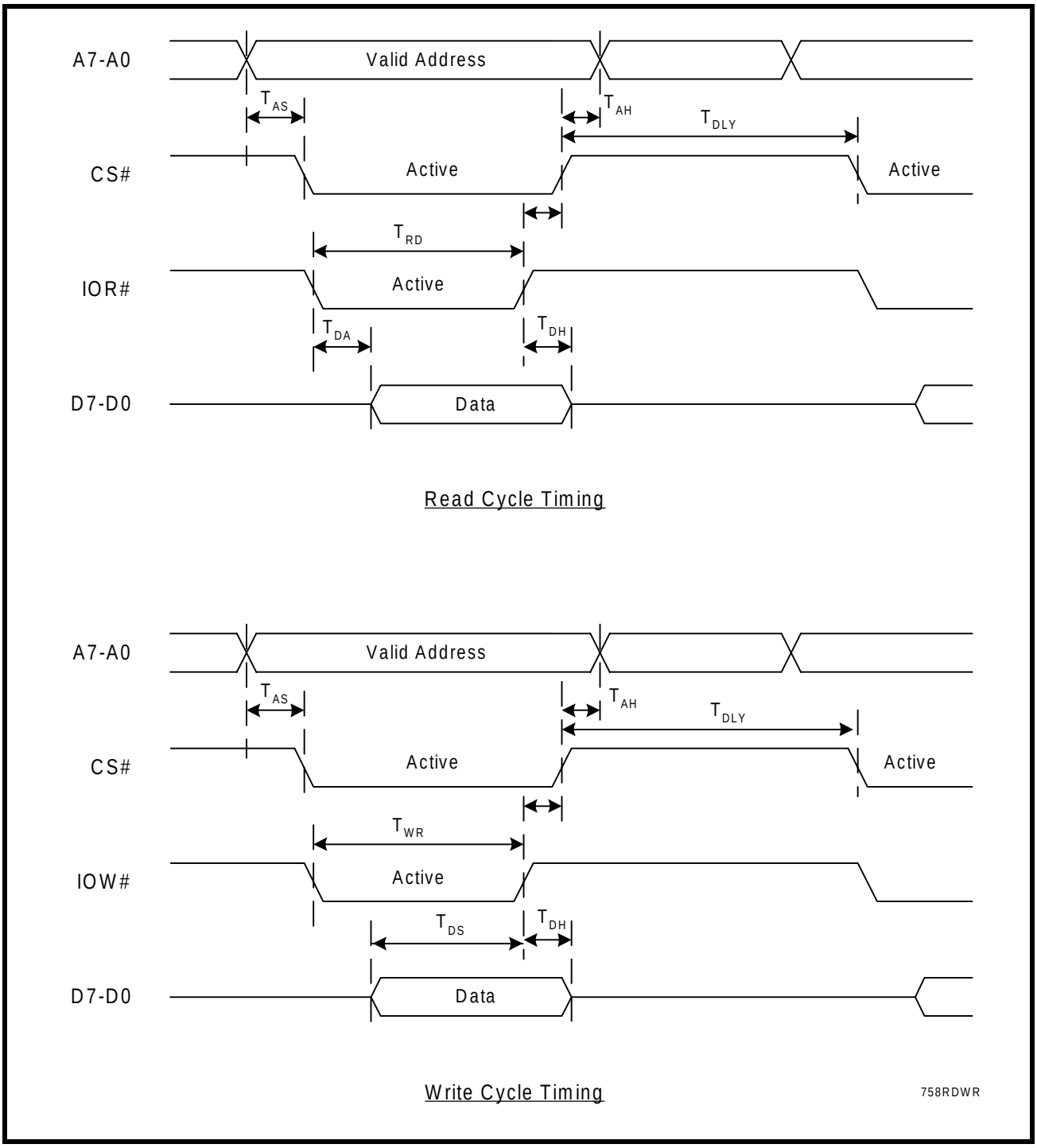
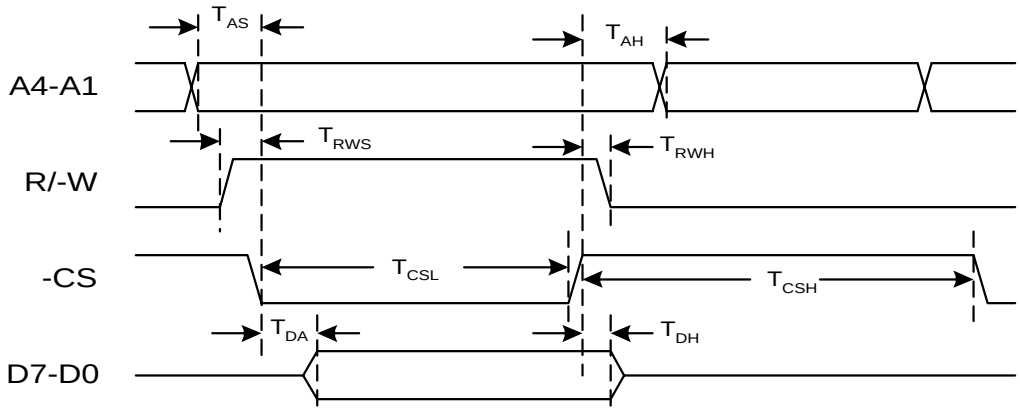
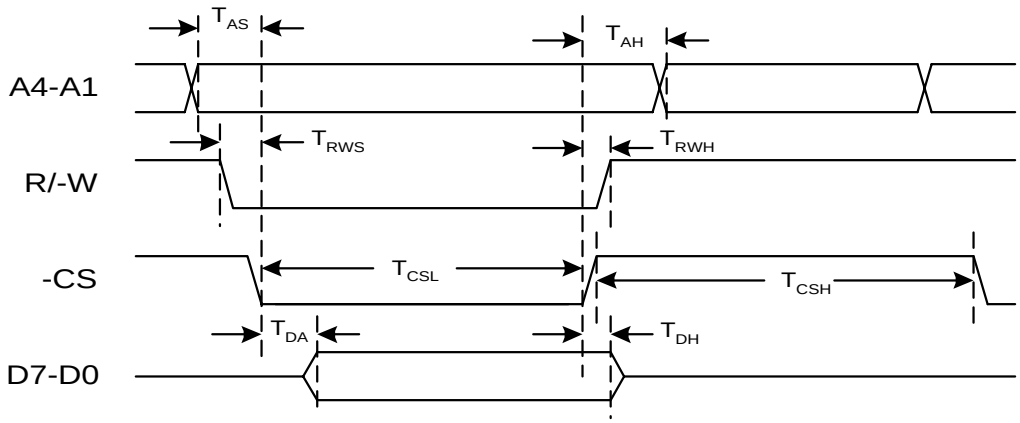


FIGURE 17. MOTOROLA DATA BUS READ AND WRITE TIMING



Read Cycle Timing



Write Cycle Timing

FIGURE 18. MODEM INPUT/OUTPUT PORT DELAY

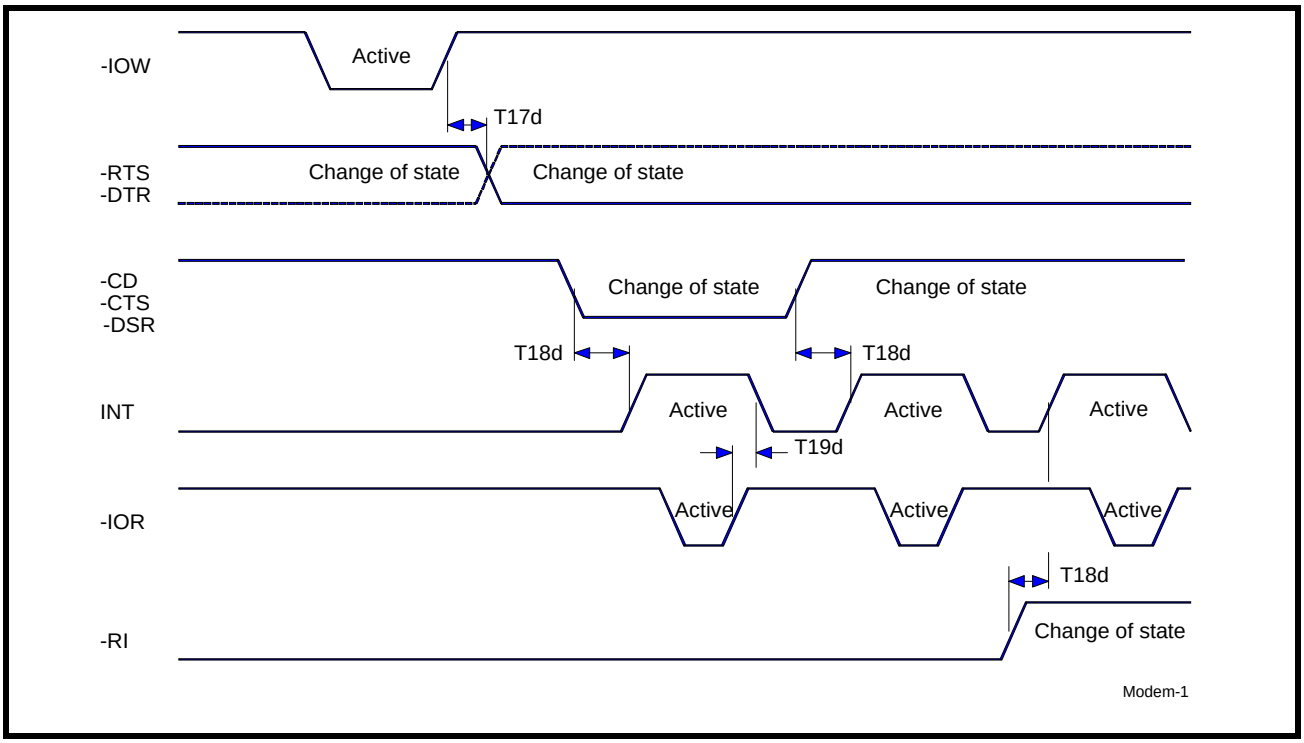


FIGURE 19. TRANSMIT DATA INTERRUPT AT TRIGGER LEVEL

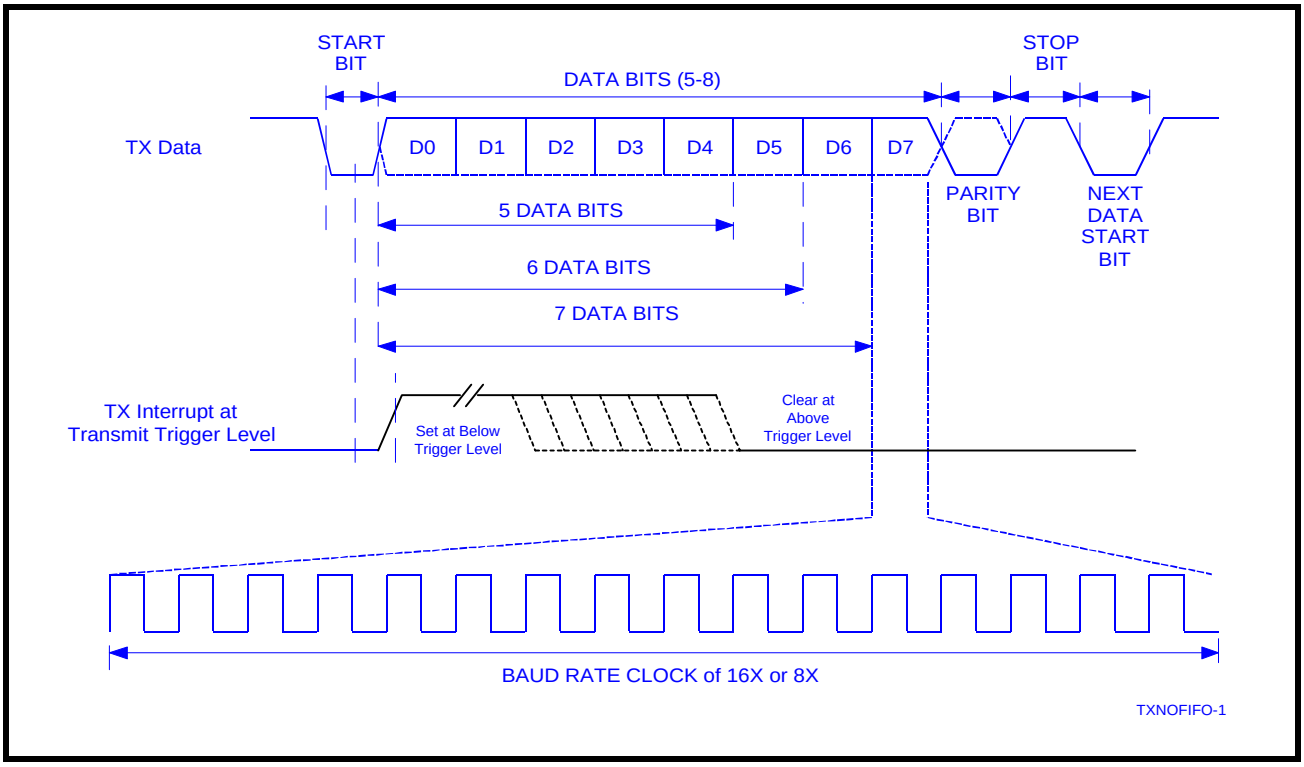
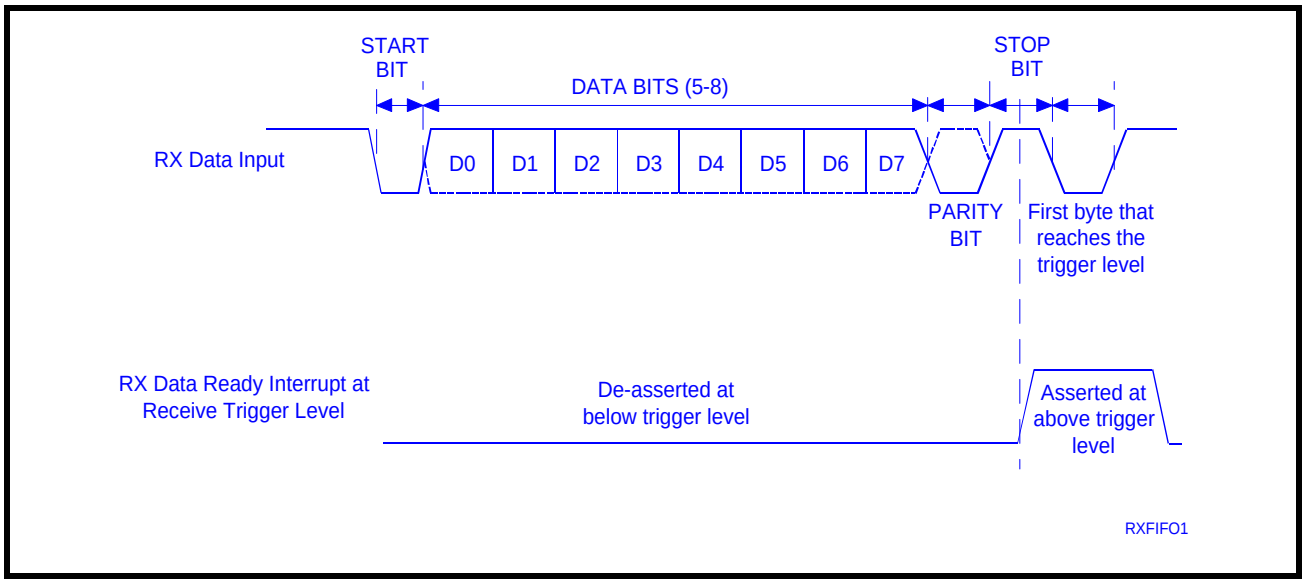
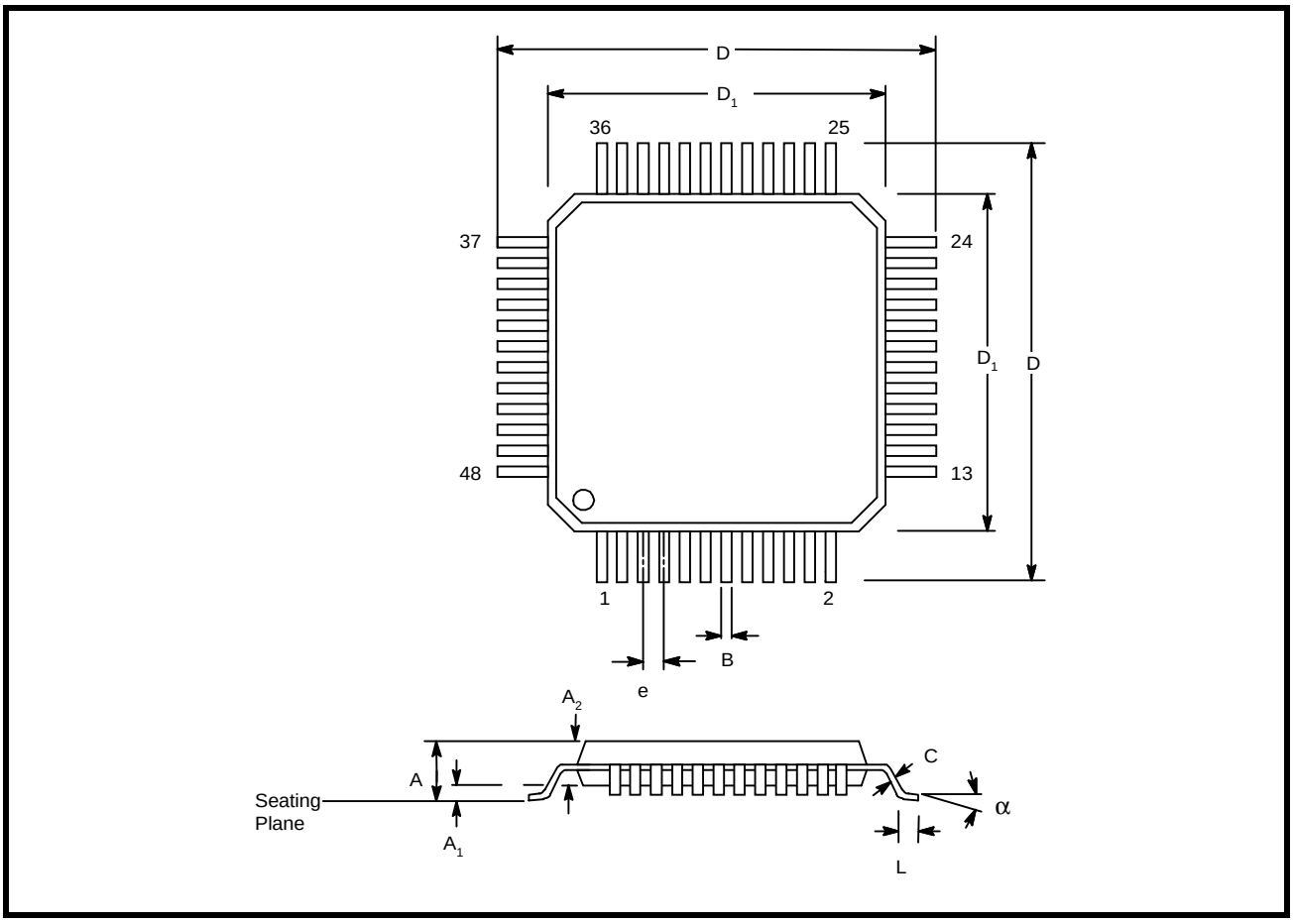


FIGURE 20. RECEIVE DATA READY INTERRUPT AT TRIGGER LEVEL



PACKAGE DIMENSIONS (48 PIN TQFP - 7 X 7 X 1 mm)



Note: The control dimension is the millimeter column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.055	0.063	1.40	1.60
A_1	0.002	0.006	0.05	0.15
A_2	0.053	0.057	1.35	1.45
B	0.007	0.011	0.17	0.27
C	0.004	0.008	0.09	0.20
D	0.346	0.362	8.80	9.20
D_1	0.272	0.280	6.90	7.10
e	0.020 BSC		0.50 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°

TABLE 14: EXPLANATION OF DATA SHEET REVISIONS

FROM	TO	CHANGES	DATE
-	P1.0.0	Initiate Data sheet	January 2001

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