Semiconductor Corporation

# CS61544

## *T1 Line Interface*

### Features

- Provides Analog T1 Line Interface
- Fully Compatible with CB119, Publication 43802, & TR-TSY-000009
- Programmable Pulse-Shaping Line Driver
- Performs Data and Timing Recovery
- Implements ISDN Primary Rate and DMI Interface
- Diagnostic and Performance Monitoring Features
- Selectable B8ZS Encode/Decode
- Jitter Attenuator
- 3 Micron CMOS for High Reliability

### General Description

The CS61544 combines the analog transmit and receive line interface functions for a T1 system interface in one 28 pin device. The T1 line interface operates from a single 5V supply, is transparent to the T1 framing format, and can work with ABAM and other cable types.

Crystal's SMART *Analog*™ circuitry shapes the transmit pulse internally, providing the appropriate pulse shape at the DSX-1 cross-connect for the line lengths ranging from 0 to 655 feet. Maximum range is greater than 1500 feet. The transmitter uses an elastic store to remove jitter from the outgoing data prior to transmission.

3

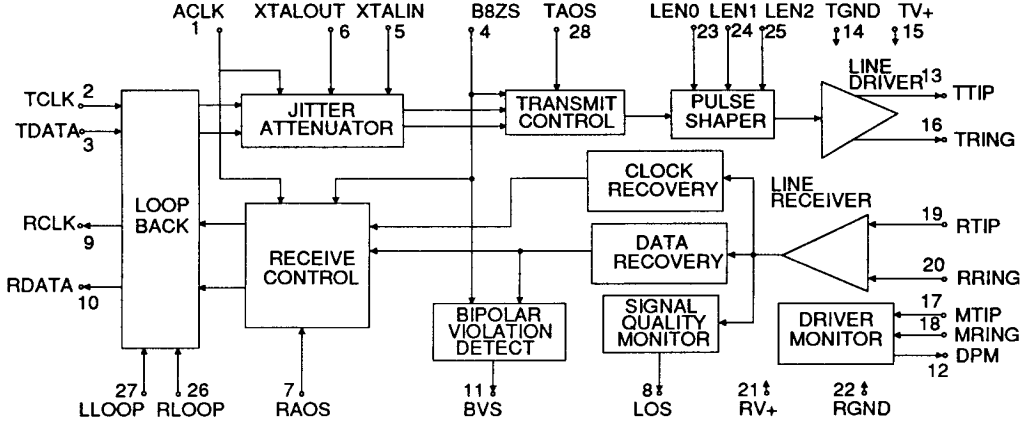
### Applications

- Interfacing Networking Equipment such as M13 Multiplexers to a DSX-1 Cross Connect.
- Interfacing fiber optic transmission equipment to T1 lines.

**ORDERING INFORMATION**

| | | |
|---|---|---|
| CS61544-IP | - | 28 Pin Plastic DIP |
| CS61544-ID | - | 28 Pin Cerdip |
| CS61544-IL | - | 28 Pin PLCC (j-leads) |

### Block Diagram

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## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Min | Max | Units |
|---|---|---|---|---|
| DC Supply (referenced to GND) | RV+, TV+ | - | 6.0 | V |
| Input Voltage, Any Pin (Note 1) | $V_{in}$ | RGND-0.3 | RV+ + 0.3 | V |
| Input Current, Any Pin (Note 1 & 2) | $I_{in}$ | - | 10 | mA |
| Ambient Operating Temperature | $T_A$ | -40 | 85 | °C |
| Storage Temperature | $T_{stg}$ | -65 | 150 | °C |

Notes: 1. Excluding RTIP and RRING.
2. Transient currents of up to 100 mA will not cause SCR latch-up.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

## RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| DC Supply (Note 3) | RV+, TV+ | 4.75 | 5.0 | 5.25 | V |
| Ambient Operating Temperature | $T_A$ | -40 | 25 | 85 | °C |
| Total Power Dissipation (Note 4)<br>100% ones density & max. line length @ 5.25 V | $P_D$ | - | - | 760 | mW |

Notes: 3. TV+ must not exceed RV+ by more than 0.3V.
4. Power dissipation while driving 25Ω load, over operating temperature range. Includes CS61544 and load.

## DIGITAL CHARACTERISTICS ($T_A$ = -40 °C to 85 °C; V+ = 5.0V ± 5%; GND = 0V)

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| High-Level Input Voltage Pins 1-5, 7, 23 - 28 | $V_{IH}$ | 2.0 | - | - | V |
| Low-Level Input Voltage Pins 1-5, 7, 23 - 28 | $V_{IL}$ | - | - | 0.8 | V |
| High-Level Output Voltage (Note 5)<br>$I_{OUT}$=-40 uA Pins 6, 8 - 12 | $V_{OH}$ | 2.4 | - | - | V |
| Low-Level Output Voltage (Note 5)<br>$I_{OUT}$= 1.6 mA Pins 6, 8 - 12 | $V_{OL}$ | - | - | 0.4 | V |
| Input Leakage Current | | - | - | ±10 | uA |

Note: 5. Output drivers will output CMOS logic levels into a CMOS load.

Specifications are subject to change without notice.

## ANALOG CHARACTERISTICS ($T_A$ = -40°C to +85°C; V+ = 5.0V ±5%; GND = 0V)

| Parameter | | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| AMI Output Pulse Amplitudes | Measured at the DSX | 2.4 | 3.0 | 3.6 | $V_{0-p}$ |
| Load Presented to Transmitter Output | (Note 6) | - | 25 | - | ohms |
| Power in 2kHz band about 772kHz | (Note 7) | 12.6 | 15 | 17.9 | dBm |
| Power in 2kHz band about 1.554MHz (referenced to power at 772kHz) | (Note 7) | -29 | -38 | - | dB |
| Positive to Negative Pulse Imbalance | (Note 7) | - | 0.2 | 0.5 | dB |
| Input Jitter Tolerance-Transmitter | | 7.0 | - | - | U.I. |
| Jitter Attenuation Curve Corner Frequency | (Note 8) | - | - | 50 | Hz |
| Loss of Signal Threshold | | - | 0.5 | - | V |
| Receiver Sensitivity Below DSX-1 | (2.4V) | -10 | - | - | dB |
| Receiver Jitter Tolerance | (Note 9) | | | | |
| 8kHz - 40kHz | | 0.1 | - | - | U.I. |
| 10Hz - 500Hz | | 5 | - | - | U.I. |

Notes:
6. On the CS61544 side of the 2:1 transformer, with a 100Ω impedance line attached to the secondary.
7. Typical performance with 0.47 µF capacitor in series with primary of transmitter output transformer. Not production tested. Parameters guaranteed by design and characterization.
8. Crystal pull range: ± 200 ppm. Five unit intervals of input jitter. Slope above corner frequency is -20dB/decade. See Figure 5.
9. For CERDIP ICs, assumes IC is operated within -70° to +70° C of reset temperature. For Plastic ICs, assumes is operated within -25° to +40° C of reset temperature (meets Bellcore central office specification: TR-EOP-000063 NEBS). For all packages, assumes IC is operated within 0.1 V of reset V+. Input data pattern is quasi-random: (2↑20) - 1 with 1-in-15. Between 500 Hz and 8 kHz the jitter tolerance will be better than the AT&T 43802 line shown in Figure 7.

## SWITCHING CHARACTERISTICS ($T_A$ = -40°C to +85°C; V+ = 5.0V ±5%; GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+)

| Parameter | | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Crystal Frequency | (Note 10) | $f_c$ | - | 6.176000 | - | MHz |
| TCLK Frequency | | $f_{in}$ | - | 1.544 | - | MHz |
| ACLK Frequency | (Note 11) | $f_{out}$ | - | 1.544 | - | MHz |
| RCLK Pulse Width | | $t_{pwh}$ | - | 324 | - | ns |
| | (Note 12) | $t_{pwl}$ | - | 324 | - | ns |
| Duty Cycle | (Note 13) | | - | 50 | - | % |
| Rise Time, All Digital Outputs | (Note 14) | $t_r$ | - | - | 100 | ns |
| Fall Time, All Digital Outputs | (Note 14) | $t_f$ | - | - | 100 | ns |
| TDATA to TCLK Falling Setup Time | | $t_{su}$ | 25 | - | - | ns |
| TCLK Falling to TDATA Hold Time | | $t_h$ | 25 | - | - | ns |
| RDATA to RCLK Rising Setup Time | | $t_{su}$ | - | 274 | - | ns |
| RCLK Rising to RDATA Hold Time | | $t_h$ | - | 274 | - | ns |
| Reset Pulse Duration | | | 0.2 | - | 2000 | us |

Notes: 10. Crystal must meet specifications described in CXT6176 data sheet.
11. ACLK provided by an external source or TCLK.
12. The sum of the pulse widths must always meet the frequency specifications.
13. Duty cycle is $(t_{pwh} / (t_{pwh}+t_{pwl}))*100\%$.
14. At maximum load of 1.6mA and 50pF.

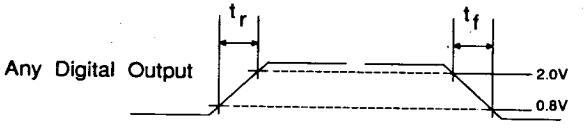



**Figure 1 - Signal Rise and Fall Characteristics**

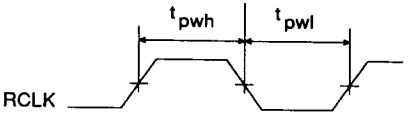



**Figure 2 - Clock Signal Quality**


**Figure 3 - Switching Characteristics**

Note that when externally looping RCLK back into TCLK, RCLK must be inverted.

## THEORY OF OPERATION

### *Transmitter*

The transmitter takes binary (unipolar) data from a T1 terminal and produces alternate bipolar pulses of appropriate shape. The transmit clock and transmit data (TCLK, TDATA) are supplied synchronously. Data is sampled on the falling edge of the input clock.

Line lengths from 0 to 655 feet (as measured from the CS61544 to the DSX-1 cross connect) are selectable. Pulse shaping and signal level are determined by "line length select" inputs and require no external circuitry. Pulse shaping is accomplished with a slew-rate-controlled fast digital-to-analog converter. Alternate mark inversion operation is implemented by driving the line in a true differential manner. In order to achieve the necessary line voltages, which exceed the 5 volt supply, a two-to-one, step-up transformer is required. The line driver drives a 25Ω equivalent load.

To place the device in a low power dissipation mode (i.e., to disable the drive), the B8ZS and TDATA should be held low while TCLK continues to be input. When any transmit control pin (TAOS, LEN0, LEN1, LEN2, LLOOP, or RLOOP) is toggled, the transmitter stabilizes within 16 bit periods.

B8ZS coding can be inserted into the data stream using the B8ZS select feature. This feature replaces every string of eight consecutive zeros with a pulse train containing bipolar violations. The violations can then be decoded at the receive end and the original data recovered.

### *Transmit Line Length Selection*

Line length selection can be controlled by an intelligent controller or hard-wired with a switch which is set at the time of installation. The line length selection supports both a three-partition arrangement for ICOT and MAT cable, and a five-partition arrangement for ABAM cable as shown in Table 1. For each line length selected, the CS61544 modifies the output pulse to meet the requirements of Compatibility Bulletin 119 and TR-TSY-000009. A typical output pulse is shown in Figure 4.

| LEN2 | LEN1 | LEN0 | LINE LENGTH SELECTED (FEET) | CABLE TYPE |
|---|---|---|---|---|
| 0 | 0 | 0 | 0-220 | MAT and ICOT |
| 0 | 0 | 1 | 220-440 | |
| 0 | 1 | 0 | 440-655 | |
| 0 | 1 | 1 | 0-133 | ABAM (AT&T 600B & 600C series) |
| 1 | 0 | 0 | 133-266 | |
| 1 | 0 | 1 | 266-399 | |
| 1 | 1 | 0 | 399-533 | |
| 1 | 1 | 1 | 533-655 | |

**Table 1 - Line Length Selection**

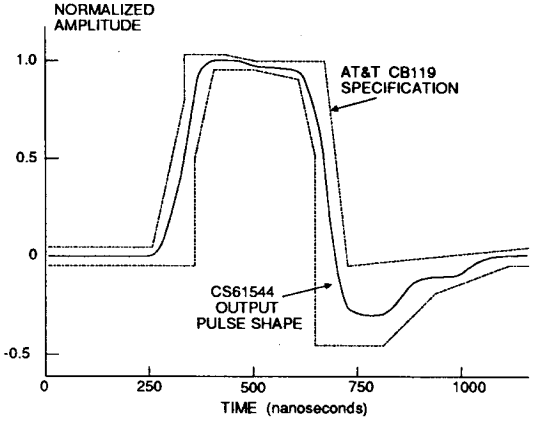



**Figure 4 - Typical Pulse Shape at DSX-1 Cross Connect**

### *Transmit Jitter Attenuator*

The 61544 will tolerate and attenuate at least seven unit intervals of jitter (peak-to-peak) from a T1 signal. Figure 5 shows a family of curves which show the jitter attenuation achieved by the 61544. Each curve shows the jitter attenuation for a signal with constant jitter amplitude over a range of jitter frequencies. The more jitter a signal has, the more the jitter is attenuated. The jitter attenuator on the transmitter side meets the jitter attenuation and input tolerance specifications of AT&T Publication 43802, as shown in Figures 6 and 7.

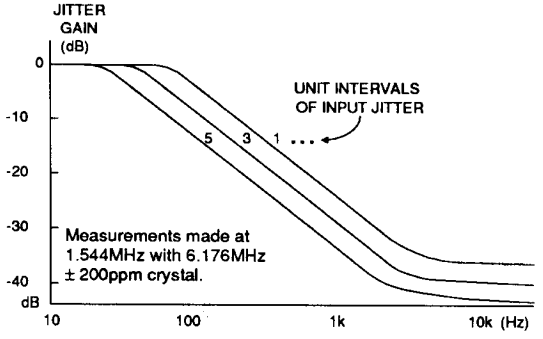



**Figure 5 - CS61544 Jitter Attenuation Curves**

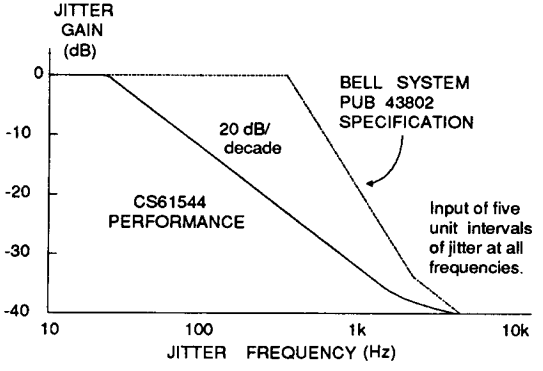



**Figure 6 - Jitter Attenuation Characteristics**

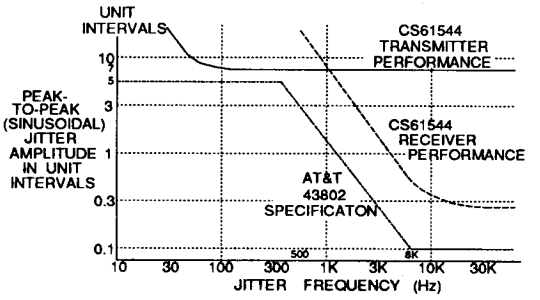



**Figure 7 - Typical Input Jitter Tolerance of Transmitter and Receiver**

The external reference crystal used by the jitter attenuator should have a nominal frequency of 6.176 MHz, and have a pull range, in the oscillator circuit, that is sufficient to meet the frequency tolerance requirements specified for the system. Furthermore, the frequency tolerance must be met over all operating temperatures. The jitter attenuator can be disabled by driving XTALIN with a clock which is exactly four times the TCLK frequency. Remote loopback should not be used if the jitter attenuator is disabled.

### *Transmit All Ones Select*

The transmitter provides for all ones insertion at the frequency of the alternate clock input, ACLK. (The transmit clock can be used as the alternate clock by connecting pins 1 and 2 together). Transmit all ones is selected when TAOS goes high, and causes continuous ones to be transmitted on the line (TTIP and TRING) using the alternate clock. The TDATA and TCLK inputs are ignored. If Remote Loopback is in effect, any TAOS request will be ignored.

### *Receiver*

The receiver extracts data and clock from an AMI (Alternate Mark Inversion) coded signal and outputs clock and synchronized data. The receiver is sensitive to signals over the entire range of cable lengths and requires no equalization or ALBO (Automatic Line Build Out) circuits. The signal is received on both ends of a center-tapped, center-grounded transformer. The transformer is center tapped on the CS61544 side. Data on RDATA is stable and may be sampled on the rising edge of the recovered clock, RCLK. The clock and data recovery circuit meets or exceeds the jitter tolerance specifications of Publication 43802.

The two leads of the receiver transformer have opposite polarity and drive the receiver inputs RTIP and RRING differentially. Comparators detect pulses on RTIP and RRING. The comparator thresholds are dynamically established by peak detectors.

Clock recovery is achieved through a frequency and phase lock loop (FPLL). Upon power up and reset of the CS61544, and prior to the start of clock acquisition, the FPLL has its center frequency trained. A current controlled oscillator (ICO) is trained relative to the crystal oscillator frequency reference. The current is adjusted until the ICO frequency is near the reference frequency. This current is then held constant. The FPLL has small signal control from the output of the phase detector and loop filter, which takes the form of a current. This is added to the fixed current to modulate the ICO about the center frequency and close the loop. The FPLL is insensitive to variations in temperature and slight variations in power supply voltage as shown in the Analog Specifications table, but fairly large changes in power supply voltage will change the control current in the FPLL, reducing its effectiveness. Resetting the CS61544 will optimize receiver performance for the operating power supply and temperature.

The received signal is monitored to detect bipolar violations. If a bipolar violation is detected, a positive strobe (BVS) is output with a width of one half the clock period.

The receiver has the capability to decode signals which have been transmitted with B8ZS bipolar violations. This feature is enabled when B8ZS (pin 4) goes high. Recovered data is processed by B8ZS decode (if enabled) and sent to the output. The bipolar violation detection algorithm is also modified to not detect the B8ZS encoded violation as an error.

### *Loss of Signal*

The receiver reports loss of the received signal on the Loss of Signal pin, LOS. The threshold for loss of signal is 0.5 volts. A loss of signal will be indicated within 200 bit periods if an active signal falls below the threshold. In the event that the input signal drops to zero volts, the loss of signal will be indicated within 31 bit periods. When a loss of signal is detected, RDATA is not valid, but the receiver will continue to try to recover data. LOS will return to a low state when a valid signal returns to RTIP and RRING. RCLK is always output, but may drift up to ± 6% from 1.544 MHz.

### *Receive All Ones Select*

Receive all ones is selected when RAOS goes high. If receive all ones is selected when the local loopback is not in effect, continuous ones are sent to RDATA using the alternate clock, ACLK, for timing. The alternate clock, ACLK, is sent to RCLK. (The transmit clock, TCLK, can be used as the alternate clock by connecting pins 1 and 2 together.) If it is desirable to have all ones automatically replace recovered data (at RDATA) upon loss of signal, then RAOS and LOS should be tied together (pins 7 and 8).

### *Local Loopback*

The local loopback mode bypasses the receive circuit and routes the digital transmit clock and data to the receive clock and data pins. A local loopback occurs in response to LLOOP going high. Any RAOS request is overridden (see Table 2). The transmit clock and data signals, TCLK and TDATA are sent out on the line through TTIP and TRING unless transmit all ones, TAOS, is selected, in which case continuous ones are transmitted on the line at the rate determined by ACLK.

| LLOOP Input Signal | RAOS Input Signal | Source of Data for RDATA | Source of Clock for RCLOCK |
|---|---|---|---|
| 0 | 0 | RTIP & RRING | RTIP & RRING |
| 0 | 1 | all 1s | ACLK |
| 1 | X | TDATA | TCLK |

**Table 2 - Interaction of LLOOP and RAOS**

### *Remote Loopback*

In remote loopback, the recovered clock and data input on RTIP and RRING are sent through the elastic store to remove jitter, and back out on the line via TTIP and TRING. Selecting remote loopback overrides any TAOS request (see Table 3). The recovered incoming signals are also sent to RCLK and RDATA unless receive all ones (RAOS) is selected, in which case continuous ones and an alternate clock are sent to RDATA and RCLK. Remote loopback occurs in response to RLOOP going high. Simultaneous selection of local and remote loopback modes is not valid (see *Reset*).

| RLOOP Input Signal | TAOS Input Signal | Source of Data for TTIP & TRING | Source of Clock for TTIP & TRING |
|---|---|---|---|
| 0 | 0 | TDATA | TCLK |
| 0 | 1 | all 1s | ACLK |
| 1 | X | RTIP & RRING | RTIP & RRING |

Notes:
1. X - Don't care. The identified All Ones Select input is ignored when the indicated loopback is in effect.
2. Logic 1 indicated that Loopback or All Ones option is selected.

**Table 3 - Interaction of RLOOP and TAOS**

### *Driver Performance Monitor*

To aid in early detection and easy isolation of nonfunctioning T1 links, the CS61544 is able to monitor transmit drive performance and report when the driver is no longer operational. This feature can be used to monitor either the device's performance or the performance of a neighboring CS61544. The driver performance monitor indicator is normally at a low (zero) logic level, and goes to high level upon detecting driver failure.

The driver performance monitor consists of a receiver that monitors the transmitted signal on input pins, MTIP and MRING. If no signal is present on MTIP and MRING for between 15 to 31 clock cycles, the DPM pin goes high.

To provide immunity from spurious DPM reports, the following application procedure is recommended: If the controller on the T1 line card detects that DPM has hone high before taking actions to respond to the driver failure. The intent of the reconfirmation is to screen out events where DPM goes high for a few bit periods, erroneously indicating a driver problem. This situation can occur only when ones density is very low.

Whenever more than one CS61544 reside on the same circuit board, the effectiveness of the driver performance monitor can be maximized by having each CS61544 monitor performance of a neighboring CS61544 device, rather than having it monitor its own performance.

*Reset*

The CS61544 initiates internal reset procedures either upon power up or in response to a reset request. After initial power up, the device will delay for approximately 10 ms before initiating the training proceedure for the FPLL. It is advisable to issue a reset request after the power supply has stabilized and signals have been applied to the device to insure that conditions on the chip are stable before FPLL training takes place. Training the FPLL takes at most 43 ms, but typically requires less than half that amount of time. These conditions should also be adhered to if temporary loss of power supply occurs.

A reset request is made by simultaneously setting both RLOOP and LLOOP high for a period not to exceed 2 ms. Reset will be completed within 53 ms after the falling edge of the reset request (falling edge of RLOOP and LLOOP).

During the reset procedure, the loss of signal indicator is high. Once the reset procedures are completed, the loss of signal indicator goes low, signifying that normal operation of the device has begun.

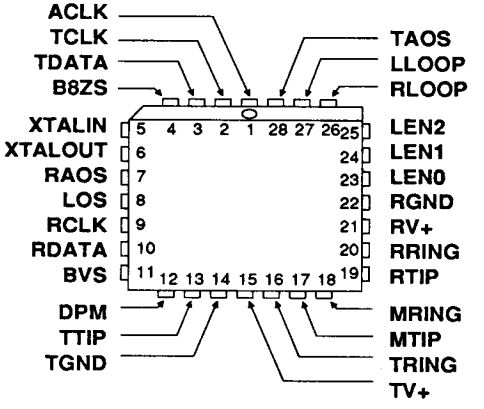
*Power Supply*

The device operates from a single 5 volt supply. Separate pins for transmit and receive supplies provide internal isolation. However these pins may be connected externally with no impact on device performance, provided the power supply pins are decoupled to their respective grounds. These capacitors should be located physically close to the device. TV+ must not exceed RV+ by more than 0.3V.

Decoupling and filtering of the power supplies is crucial for the proper operation of the analog circuits in both the transmit and receive paths. The best way to configure the power supplies is to tie TV+ to RV+ at the chip. A 1.0 µF capacitor should be connected between TV+ and TGND, and a 0.1 µF capacitor should be connected between RV+ and RGND. Use mylar or ceramic capacitors and place them as closely as possible to their respective power supply pins. A 68 µF tantalum capacitor should be added close to the RV+/RGND supply. If TV+ and RV+ are supplied by different traces, 68 µF capacitors should be used on both supplies. Wire wrap breadboarding of the CS61544 is not recommended because lead resistance and inductance serve to defeat the function of the decoupling capacitors.

## PIN DESCRIPTIONS

| | | | | | |
|---|---|---|---|---|---|
| ALTERNATE EXTERNAL CLOCK | ACLK | 1 | 28 | TAOS | TRANSMIT ALL ONES SELECT |
| TRANSMIT CLOCK | TCLK | 2 | 27 | LLOOP | LOCAL LOOPBACK |
| TRANSMIT DATA | TDATA | 3 | 26 | RLOOP | REMOTE LOOPBACK |
| B8ZS ENABLE | B8ZS | 4 | 25 | LEN2 | BIT 2 OF LINE LENGTH SELECT |
| CRYSTAL INPUT 2 | XTALIN | 5 | 24 | LEN1 | BIT 1 OF LINE LENGTH SELECT |
| CRYSTAL INPUT 1 | XTALOUT | 6 | 23 | LEN0 | BIT 0 OF LINE LENGTH SELECT |
| RECEIVE ALL ONES SELECT | RAOS | 7 | 22 | RGND | RECEIVE GROUND |
| LOSS OF SIGNAL | LOS | 8 | 21 | RV+ | RECEIVE V+ (+5V DC) |
| RECOVERED CLOCK | RCLK | 9 | 20 | RRING | RECEIVE RING |
| RECEIVE DATA | RDATA | 10 | 19 | RTIP | RECEIVE TIP |
| BIPOLAR VIOLATION STROBE | BVS | 11 | 18 | MRING | MONITORED RING |
| DRIVER PERFORMANCE MONITOR | DPM | 12 | 17 | MTIP | MONITORED TIP |
| TRANSMIT TIP | TTIP | 13 | 16 | TRING | TRANSMIT RING |
| TRANSMIT GROUND | TGND | 14 | 15 | TV+ | TRANSMIT V+ (+5V DC) |




### *Power Supplies*

**TV+ - Positive Power Supply, Transmit Drivers, Pin 15.**
Positive power supply for the transmit drivers; typically +5 volts. TV+ must not exceed RV+ by more than 0.3V.

**TGND - Ground, Transmit Drivers, Pin 14.**
Power supply ground for the transmit drivers; typically 0 volts.

**RV+ - Positive Power Supply, Pin 21.**
Positive power supply for the device, except transmit drivers; typically +5 volts.

**RGND - Ground, Pin 22.**
Power supply ground for the device, except transmit drivers; typically 0 volts.

*Oscillator*

**XTALIN, XTALOUT - Crystal Inputs, Pins 5 and 6.**
A 6.176 MHz crystal should be connected across these pins. An externally generated 6.176 MHz clock signal may be put into the XTALIN pin, disabling the jitter attenuator. This clock must be *exactly* four times the frequency at TCLK. See the CXT6176 data sheet for more information on crystals.

*Control*

**B8ZS - B8ZS Encoding Enable, Pin 4.**
Setting B8ZS to a logic 1 enables B8ZS encoding of the transmit data and B8ZS decoding of the receive data.

3

**RAOS - Receive All Ones Select, Pin 7.**
Setting RAOS to a logic 1 causes continuous ones to be sent to RDATA at the frequency determined by ACLK.

**TAOS - Transmit All Ones Select, Pin 28.**
Setting TAOS to a logic 1 causes continuous ones to be transmitted at the frequency determined by ACLK.

**LLOOP - Local Loopback, Pin 27.**
Setting LLOOP to a logic 1 routes the transmit clock and data to the receive clock and data pins, bypassing the receive circuit. Any RAOS request is ignored. TCLK and TDATA are still transmitted unless overridden by a TAOS request.

**RLOOP - Remote Loopback, Pin 26.**
Setting RLOOP to a logic 1 causes the recovered clock and data to be sent through the jitter attenuator and through the driver back to the line. The recovered signal is also sent to RCLK and RDATA unless overridden by a RAOS request. Any TAOS request is ignored. If the oscillator is being driven with a 4X clock, the remote loopback function is not possible.

Simultaneously taking RLOOP and LLOOP high for less than 2 ms initiates a device reset.

**LEN0, LEN1, LEN2 - Line Length Selection, Pins 23, 24 and 25.**
Determines the shape and amplitude of the transmitted pulse to accomodate several cable types and lengths. See Table 1 for information on line length selection.

*Inputs*

**ACLK - Alternate External Clock, Pin 1.**
This input should be tied to TCLK or some other externally generated 1.544 MHz clock. The frequency of ACLK determines the rate at which TAOS and RAOS are output.

**TCLK, TDATA - Transmit Clock, Transmit Data, Pins 2 and 3.**

Inputs for clock and data to be transmitted. Signal jitter is attenuated and the signal is driven on to the line through TTIP and TRING. TDATA is sampled on the falling edge of TCLK.

**RTIP, RRING - Receive Tip, Receive Ring, Pins 19 and 20.**

The receive AMI signal is input to these pins. A center-tapped, center-grounded, 2:1, step-up transformer is required on these inputs, as shown in Figure A3. Data and clock are recovered and output on RDATA and RCLK.

**MTIP, MRING - Monitored Tip, Monitored Ring, Pins 17 and 18.**

These pins are normally connected to TTIP and TRING and monitor the output of a CS61544. If the monitors are not used, tying MTIP low and MRING high through a resistor will reduce power consumption slightly.

*Outputs*

**RCLK, RDATA - Recovered Clock, Receive Data, Pins 9 and 10.**

Data and clock are recovered from the RTIP and RRING inputs and output at these pins. RDATA is valid on the rising edge of RCLK.

**TTIP, TRING - Transmit Tip, Transmit Ring, Pins 13 and 16.**

The AMI, T1 signal is driven to the line through these pins. This output is designed to drive a 25Ω load. A 2:1 step-up transformer is required to drive the line as shown in Figure A1.

*Status*

**LOS - Loss of Signal, Pin 8.**

LOS goes to a logic 1 when the received signal falls below a 0.5 volt threshold, or after 31 clock cycles with out a detected one. LOS returns to logic 0 when the signal returns.

**BVS - Bipolar Violation Strobe, Pin 11.**

BVS goes to a logic 1 when a bipolar violation is detected in the received signal. The strobe is approximatly 324 ns wide and aligned with the rising edge of RCLK. The strobe will occur concurrently with the RDATA output for which the violation was detected. The bipolar violation detection algorithm is modified when B8ZS is selected to accept B8ZS encoded data.

**DPM - Driver Performance Monitor, Pin 12.**

If no signal is present on MTIP and MRING for between 15 to 31 clock cycles, DPM goes to a logic 1 until the first detected signal.

## APPLICATIONS

### *Selecting an Oscillator Crystal*

Specific crystal parameters are required for proper operation of the CS61544. It is recommended that the Crystal Semiconductor CXT6176 be used with the CS61544.

### *General Applications*

Figure A1 shows the typical configuration for the CS61544, including transmit and receive transformers. The receiver transformer is center tapped and center grounded with 200Ω resistors between the center tap and each leg on the CS61544 side. These resistors provide the 100Ω termination for the T1 line. Line Length Select pins are shown in a manual switching configuration. These inputs can be controlled by logic circuitry if desired.

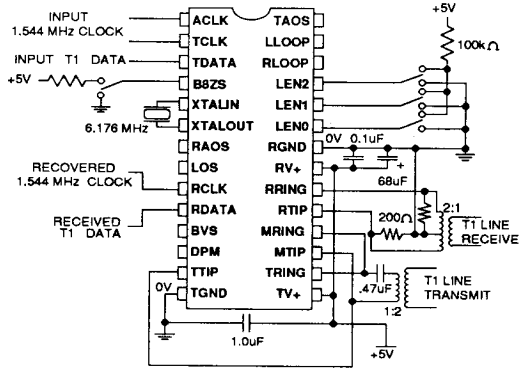



**Figure A1. Typical Configuration Showing Line Interface**

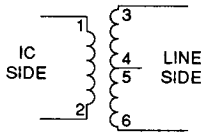
### *Transformers*

Transformers listed in Table A1 have been found to be suitable for use with the CS61544. Figure A2 shows the connections for some of the transformers mentioned in the Table A1. The transformers should be placed physically close to the CS61544.

| Manufacturer | Part # |
|---|---|
| Pulse Engineering | PE-64931 |
| Pulse Engineering | PE-64951 (dual) |
| Schott Corp. | 67115100 & 67124670 |
| Schott Corp. | 68115090 (dual) |
| Bell Fuse | 0553-5006-IC |
| Nova Magnetics | 6500-07-0001 |
| Midcom | 671-5832. |

Note: The Pulse Eng. 1682x and 5764 are still acceptable, but the above Pulse Engineering transformers are preferred. The Schott 67112060 is still acceptable, but the above Schott transformers are preferred.

**Table A1. Suitable Transformers**




Bell Fuse 0553-5006-IC
Schott Corp. 67115100
Pulse Engineering 5764 & PE-64931

**Figure A2. Transmitter Transformer Configuration**

Key transmit transformer specifications are:

Turns ratio: 1:2 (or 1:1:1)±5%

Primary inductance: 600 µH min measured at 772 khz

Leakage inductance: 1.3 µH max at 772 kHz with secondary shorted

Secondary leakage inductance: 0.4 µH max at 772 kHz.

Interwinding capacitance: 23 pF max, primary to secondary

ET-Constant: 16 V-µs min for T1;

To save on power consumption under normal operating conditions, the output drivers are powered down during the transmission of a space (zero) on to the line. Approximately one quarter cycle prior to transmitting a mark (one), the drivers are enabled. The transformer, interacting with the driver, can cause a slight voltage dif-

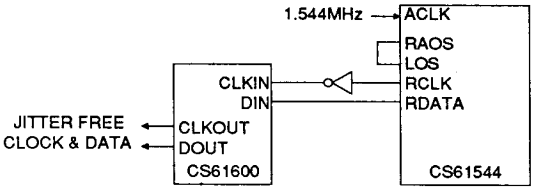



**Figure A3. Receiver Jitter Attenuation**

ference (<200 mV) between the driven zero and the non-driven zero. We recommend that this effect be eliminated by inserting a 0.47 µF non-polarized capacitor in series with the primary of the transformer.

### *Receive Side Jitter Attenuation*

In some applications it is desirable to attenuate jitter from the received signal. A CS61600 PCM jitter attenuator can be used to remove at least seven unit intervals of jitter from the recovered clock and data as shown in Figure A3.

### *Maintaining Recovered Clock*

Figure A3 also shows how the recovered clock, RCLK, can be maintained within desired specifications in the event that the received AMI signal is lost. This design requires a locally generated 1.544 MHz clock whose frequency is within the required system specifications. This clock is input to the ACLK input of the CS61544. The loss of signal output, LOS, is connected to the receive all ones select input, RAOS.

If the AMI signal is lost, the LOS signal goes high, taking RAOS high, directing the CS61544 to output all ones at RDATA at the frequency determined by ACLK (i.e. RCLK = ACLK). The CS61600 will buffer any instantaneous phase or frequency change at the RCLK and RDATA pins, retaining clock integrity. This type of circuit is necessary since the frequency/phase lock loop in the CS61544 may drift when the AMI signal is lost.

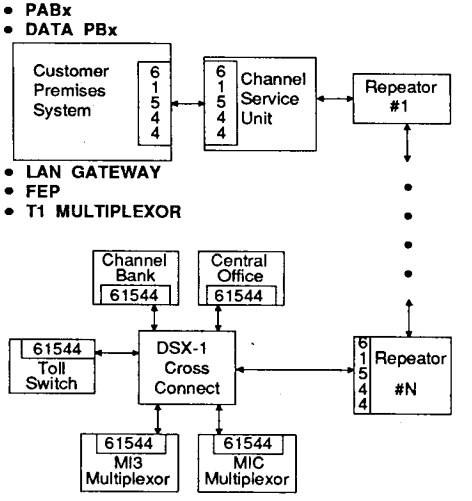



**Figure A4. Applicable Types of Connection**

If the receiver input returns, LOS goes low, deselecting RAOS, and returning the circuit to its normal operating status. It is important to note that LOS will go low as soon as a valid pulse is detected, which is before the receiver has locked onto the incoming signal. It is advisable to delay the transition from RAOS to the receiver output for a few milliseconds after LOS indicates receipt of signal.

### *Applicable Systems*

Figure A4 shows a T1 span from a customer premises location through a TELCO DSX-1 cross connect. As shown in Figure A4, the CS61544 is applicable in customer premises systems that interconnect to a channel service unit (CSU), and is applicable in network equipment that connects to a DSX-1 cross connect.

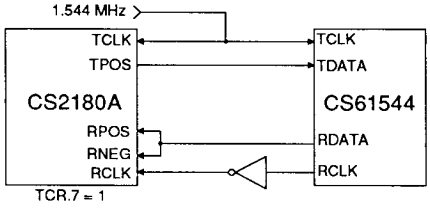



**Figure A5. Interfacing CS61544 with CS2180A**

### *Interfacing The CS61544 With T1 Digital Transceivers*

To interface with the CS2180A, connect the devices as shown in Figure A5. When RPOS is tied to RNEG, B8ZS encoding/decoding and bipolar violation detection functions are performed by the CS61544.

### *Test and Evaluation of the CS61544*

When connecting the receive clock and data, RCLK and RDATA, to the transmit clock and data, TCLK and TDATA, of the CS16544, be sure to invert the clock signal.

### *Transmitter or Receiver Function Only*

If the CS61544 is used for transmit only, tie RTIP and RRING high through a resistor, ground RAOS, RLOOP, and LLOOP, and float the outputs. To configure the device for receive only, float TTIP, TRING, TV+ and TGND, ground TAOS, TCLK, TDATA, RLOOP, LLOOP and LEN0/1/2 .